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April 1st, 2010
Renesas Electronics Corporation

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M16C/Tiny Series

Operation of Serial I/O (Reception in Clock-Synchronous Serial I/O Mode)

1. Abstract

In receiving data in clock-synchronous serial I/O mode, choose functions from those listed in Table1. Operations of the checked items are described below.

Table 1. Choosed Functions

Item	Set-up		Item	Set-up	
Transfer clock source		Internal clock (f_1/f_2/f_8/f_{32})	Continuous receive mode	Yes	Disabled
	Yes	External clock (CLKi pin)			Enabled
$\overline{\text{RTS}}$ function	Yes	$\overline{\text{RTS}}$ function enabled	Output transfer clock to multiple pins (Note 1)	Yes	Not selected
		$\overline{\text{RTS}}$ function disabled			Selected
CLK polarity	Yes	Input reception data at the rising edge of the transfer clock	Data logic select (Note 2)	Yes	No reverse
					Reverse
		Input reception data at the falling edge of the transfer clock	TxD, RxD I/O polarity reverse function (Note 2)	Yes	No reverse
					Reverse
Transfer format	Yes	LSB first	UART1 pin remapping function (Note 3)	Yes	UART1 pins assigned to $P6_7$ to $P6_4$
		MSB first			UART1 pins assigned to $P7_3$ to $P7_0$

Note 1: This can be selected only when UART1 is used in combination with the internal clock. When this function is selected, UART1 $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function can not be utilized. Set the UART1 $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ disable bit to "1".

Note 2: UART2 only

Note 3: It is possible to select it only with M16C/26A, M16C/28, and M16C/29.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M16C/26, M16C/26A, M16C/28, M16C/29 Group

This program can also be used when operating other microcomputers within the M16C family, provided they have the same SFR (Special Function Registers) as the M16C/26, M16C/26A, M16C/28, M16C/29 microcomputers. However, some functions may have been modified.
Refer to the User's Manual for details. Use functions covered in this Application Note only after careful evaluation.

3. Operation of Serial I/O

(1) Writing dummy data to the UARTi transmit buffer register, setting the receive enable bit to “1”, and the transmit enable bit to “1”, makes the data receivable status ready. At this time, the output from the $\overline{\text{RTSi}}$ pin goes to “L” level, which informs the transmission side that the data receivable status is ready (output the transfer clock from the IC on the transmission side after checking that the $\overline{\text{RTS}}$ output has gone to “L” level).

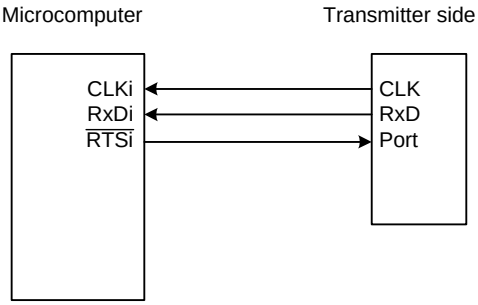
(2) In synchronization with the first falling edge of the transfer clock, the $\overline{\text{RTSi}}$ output goes to “H”, and in synchronization with the first rising edge of the transfer clock, the input signal to the RxDi pin is stored in the highest bit of the UARTi receive register. Then, data is taken in by shifting right the content of the UARTi reception data in synchronization with the rising edges of the transfer clock.

(3) When 1-byte data lines up in the UARTi receive register, the content of the UARTi receive register is transmitted to the UARTi receive buffer register. The transfer clock stops at “H” level. At this time, the receive complete flag and the UARTi receive interrupt request bit goes to “1”.

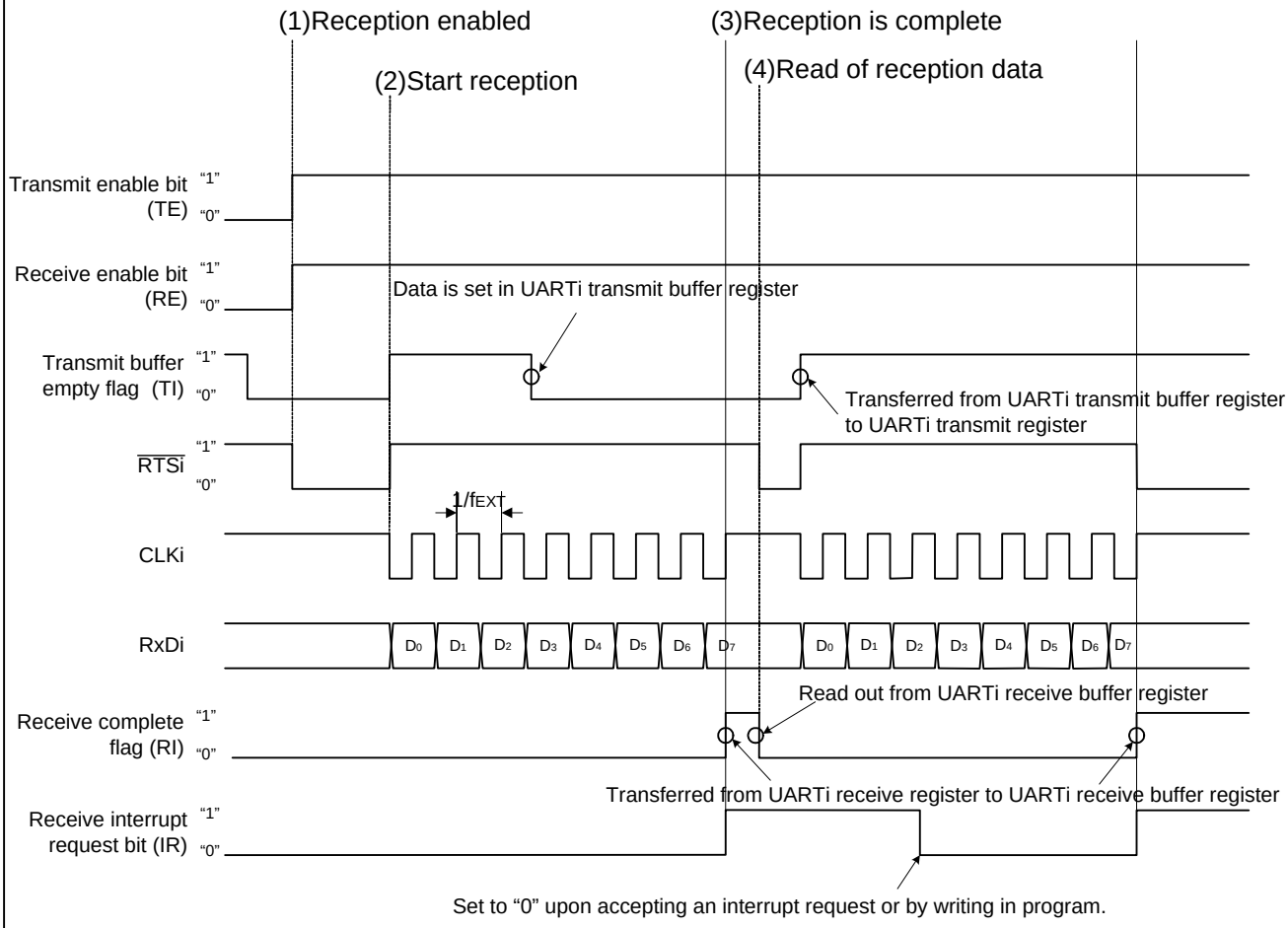
(4) The receive complete flag goes to “0” when the lower-order byte of the UARTi buffer register is read. At this time, The $\overline{\text{RTSi}}$ output goes to “L”.

Figure 1 shows the operation timing.

Example of wiring



Example of operation



i = 0 to 2

Shown in ( ) are bit symbols.

The above timing applies to the following settings:
- External clock is selected.
- $\overline{\text{RTS}}$ function is selected.
- CLK polarity select bit = "0".

f_{EXT} : frequency of external clock

Make sure that the following conditions are met when the CLKi pin input ="H" before data reception

- Transmit enable bit → "1"
- Receive enable bit → "1"
- Dummy data write to UARTi transmit buffer register

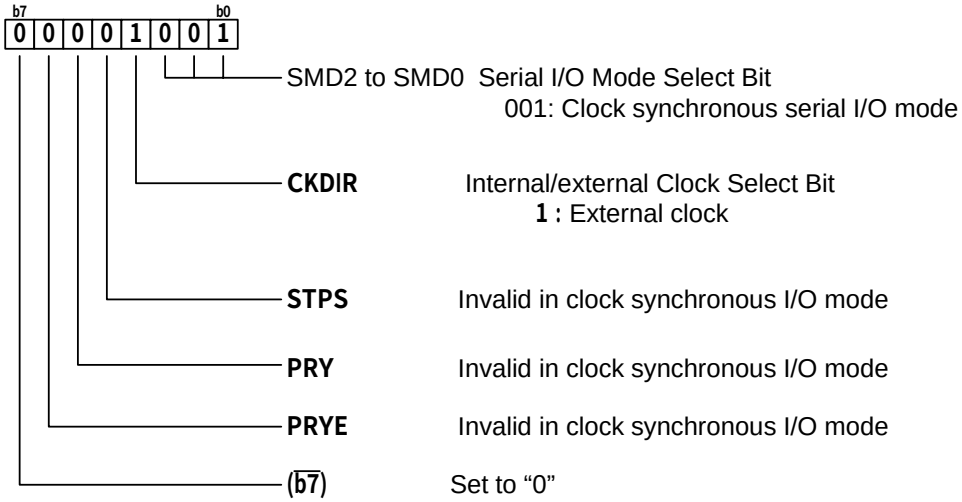
Figure 1. Operation Timing of Reception in Clock-Synchronous Serial I/O Mode

3.1 Register Setting

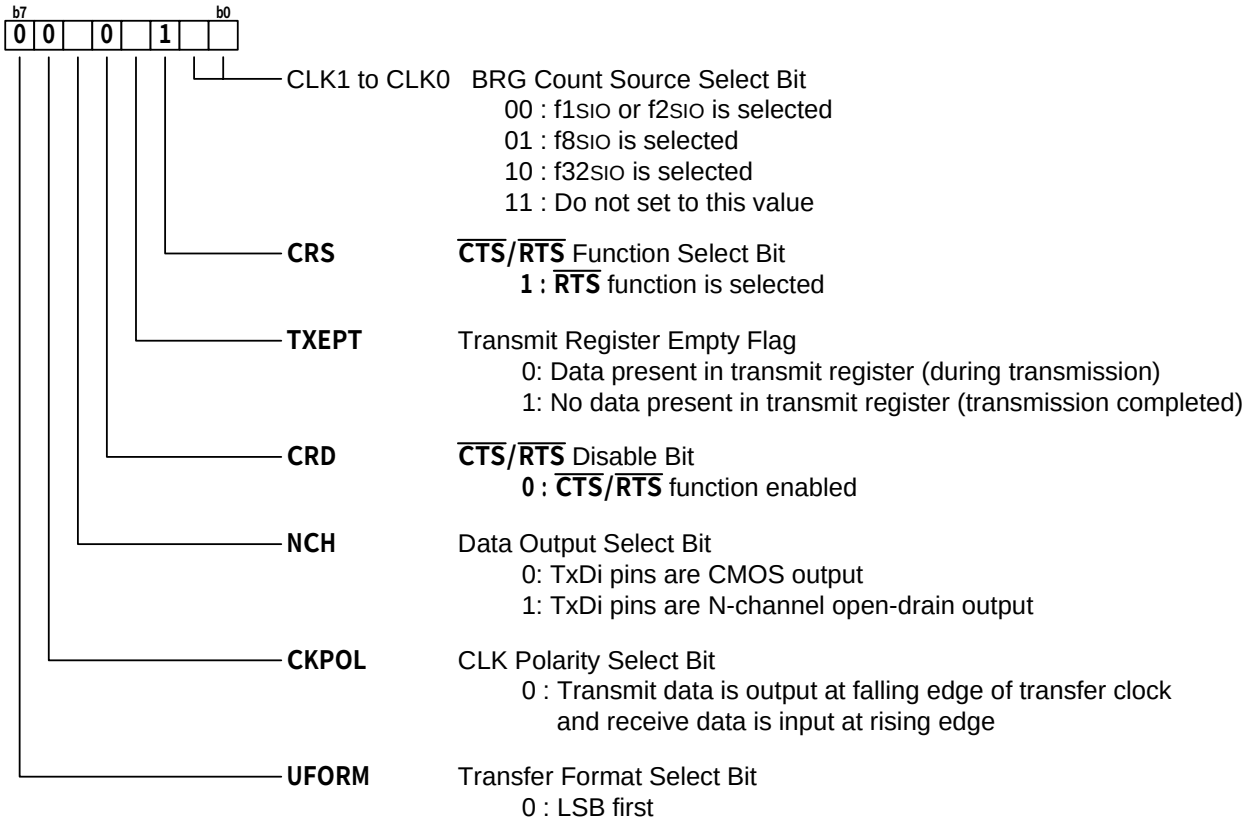
To enable the operation defined in “Section 3. Operation of timer A”, the following register settings must be taken place step by step. For detail configuration of each register, please refer to M16C/26 Group hardware manual, M16C/26A Group hardware manual, M16C/28 Group hardware manual, M16C/29 Group hardware manual.

3.1.1 UART0, 1

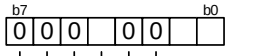
(1) Setting UARTi transmit/receive mode register (i=0, 1)



(2) Setting UARTi transmit/receive control register 0 (i=0,1)



(3) Setting UART transmit/receive control register 2



U0RRM — UART0 Continuous Receive Mode Enable Bit
0 : Continuous receive mode disabled

U1RRM — UART1 Continuous Receive Mode Enable Bit
0 : Continuous receive mode disabled

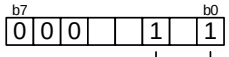
CLKMD0 — UART1 CLK/CLKS Select Bit 0
Effective when CLKMD1 = "1"

CLKMD1 — UART1 CLK/CLKS Select Bit 1
0 : CLK output is only CLK1

RCSP — Separate UART0 $\overline{CTS}/\overline{RTS}$ Bit
0 : $\overline{CTS}/\overline{RTS}$ shared pin
1 : $\overline{CTS}/\overline{RTS}$ separated ($\overline{CTS}_0$ supplied from the $P6_4$ pin)

($\overline{b7}$) — Set to "0"

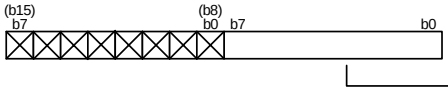
(4) Reception enabled (UARTi transmit/receive control register 1) (i=0,1))



TE — Transmit Enable Bit
1 : Transmission enabled

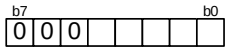
RE — Receive Enable Bit
1 : Reception enabled

(5) Writing dummy data (UARTi transmit buffer register (i=0,1))



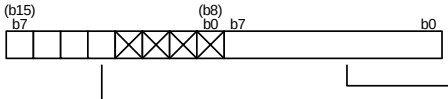
Setting dummy data

(6) Checking the status of UARTi receive buffer register (i=0,1)



RI — Receive Complete Flag
0 : No data present in UiRB register
1 : Data present in UiRB register

(7) Reading out reception data and checking error (Read UARTi reception buffer register (i=0,1))

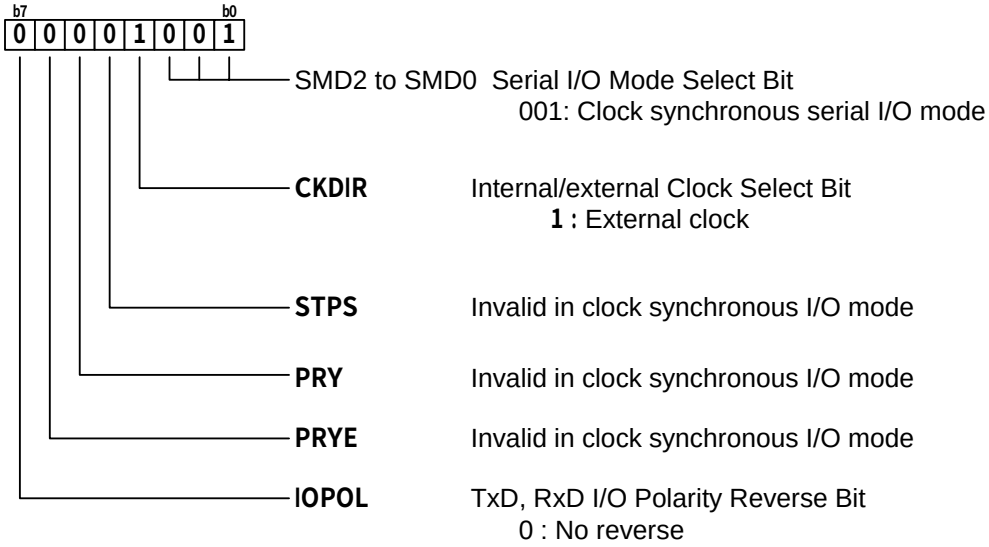


Reception data

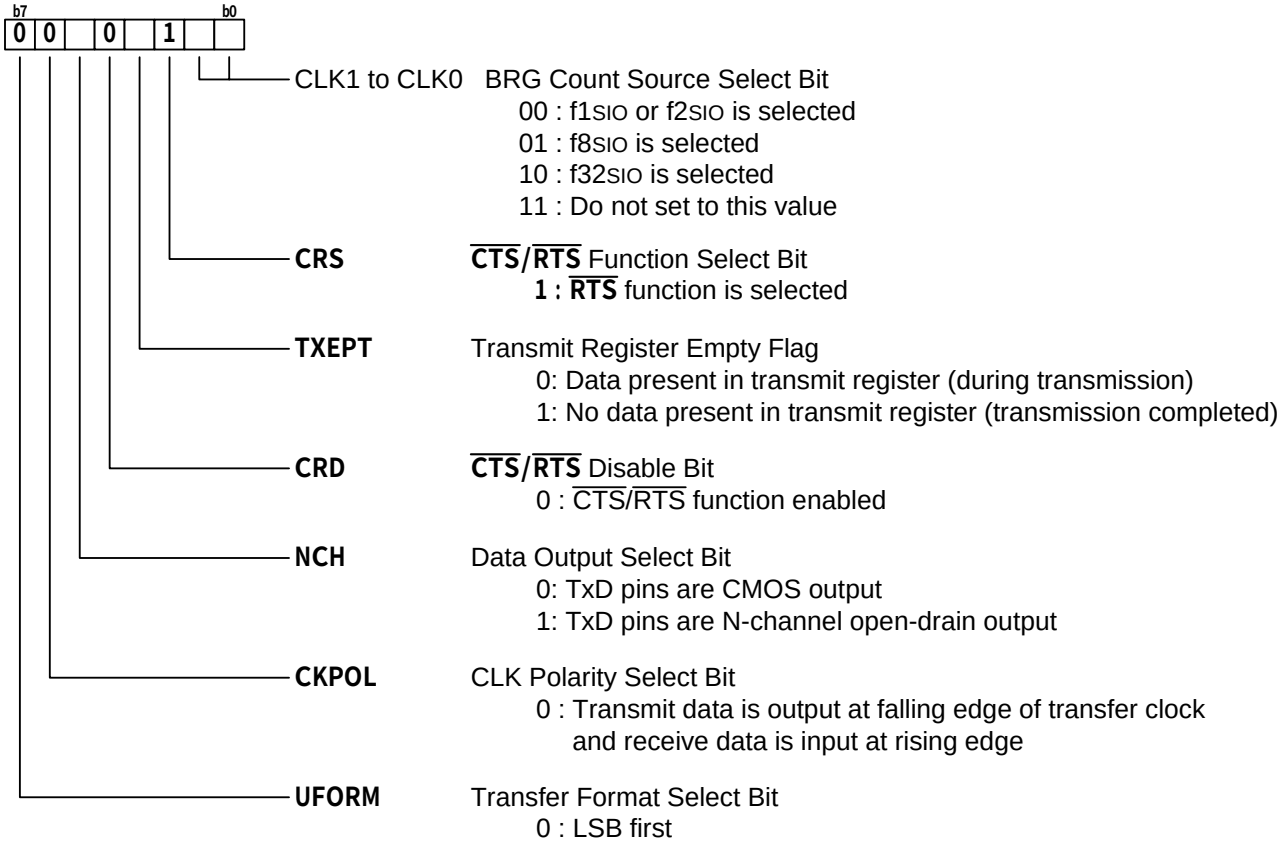
OER — Overrun Error Flag
0 : No overrun error
1 : Overrun error found

3.1.2 UART2

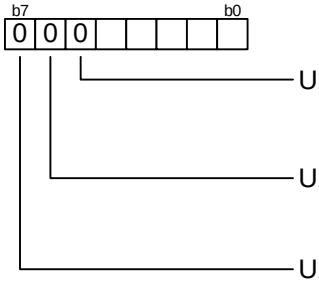
(1) Setting UART2 transmit/receive mode register



(2) Setting UART2 transmit/receive control register 0



(3) Setting UART2 transmit/receive control register 1

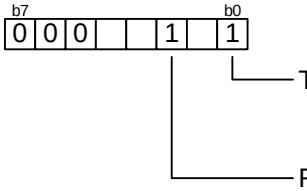


UART2 Continuous Receive Mode Enable Bit
0 : Continuous receive mode disable

Data Logic Select Bit
0 : No reverse

Error Signal Output Enable Bit
Set to “0” in clock synchronous serial I/O mode

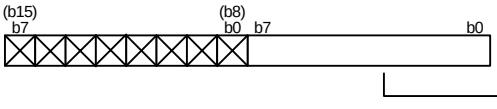
(4) Reception enabled (UART2 transmit/receive control register 1)



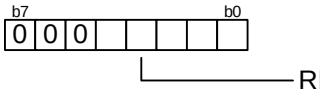
Transmit Enable Bit
1 : Transmission enabled

Receive Enable Bit
1 : Reception enabled

(5) Writing dummy data (UART2 transmit buffer register)

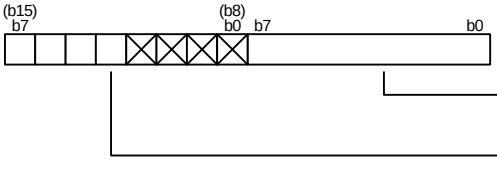


(6) Checking the status of UART2 receive buffer register



eceive Complete Flag
0 : No data present in U2RB register
1 : Data present in U2RB register

(7) Reading out reception data and checking error (Read UART2 reception buffer register)



Overrun Error Flag
0 : No overrun error
1 : Overrun error found

4. Sample Program

4.1 UART0

```
/************************************************************
 *                                                          *
 *   FILE NAME :                                            *
 *   CPU       : M16C/Tiny series                           *
 *   Function  : Operation of UART0                         *
 *                (Clock synchronous serial I/O receive)    *
 *   Version   : 1.00                                       *
 *                                                          *
 *   Copyright (C)2004, Renesas Technology Corp.            *
 *   Copyright (C)2004, Renesas Solutions Corp.             *
 *                                                          *
 ************************************************************/
/*************************
 *   include file        *
 *************************/
#include "sfr28.h"

/*************************
 *   Function Definition *
 *************************/

/*************************
 *   main                *
 *************************/
    unsigned short   receive_data;

void main(void) {

    unsigned short   dummy_data = 0;

    u0mr = 0x09; /* UART0 transmint/receive mode register setting
                 Clock synchronous serial I/O mode
                 External clokc select
            */

    u0c0 = 0x04; /* UART0 transmint/receive control register 0 setting
                 ~RTS function select
                 ~CTS/~RTS function enabled
                 TxD0 pin is CMOS output
                 Transmission data is output at falling edge of transfer
                 clock and reception data is input at rising edge
                 LSB first
            */

    ucon = 0x00; /* UART transmint/receive control register 2 setting
                 UART0 tansmit interrupt cause is selected to "Transmit buffer empty(TI=1)"
                 ~CTS/~RTS shared pin
            */

    u0c1 = 0x05; /* UART transmint/receive control register 1 setting
                 Transmit enabled
                 Receive enabled
            */

    while (1) {

        while (!p6_1) {      /* Wait until CLK0 "H" */
        }

        u0tb = dummy_data;   /* Writing dummy data */

        while (!ri_u0c1) {   /* Check & wait the status of UART0 receive complete flag */
        }

        receive_data = u0rb; /* Receive data read */

    }
}
```

4.1.1 UART2

```
/************************************************************
 *                                                          *
 *   FILE NAME :                                            *
 *   CPU       : M16C/Tiny series                           *
 *   Function  : Operation of UART2                         *
 *               (Clock synchronous serial I/O receive)     *
 *   Version   : 1.00                                       *
 *                                                          *
 *   Copyright (C)2004, Renesas Technology Corp.            *
 *   Copyright (C)2004, Renesas Solutions Corp.             *
 *                                                          *
 ************************************************************/
/***************************
 *   include file          *
 ***************************/
#include "sfr28.h"

/***************************
 *   Function Definition   *
 ***************************/

/***************************
 *   main                  *
 ***************************/
    unsigned short   receive_data;

void main(void) {

    unsigned short   dummy_data = 0;

    u2mr = 0x09; /* UART2 transmint/receive mode register setting
                 Clock synchronous serial I/O mode
                 External clokc select
            */

    u2c0 = 0x04; /* UART2 transmint/receive control register 0 setting
                 ~RTS function select
                 ~CTS/~RTS function enabled
                 TxD0 pin is CMOS output
                 Transmission data is output at falling edge of transfer
                 clock and reception data is input at rising edge
                 LSB first
            */

    u2c1 = 0x05; /* UART2 transmint/receive control register 1 setting
                 Transmit enabled
                 Receive enabled
            */

    while (1) {

        while (!p7_2) {      /* Wait until CLK2 "H" */
        }

        u2tb = dummy_data;       /* Writing dummy data */

        while (!ri_u2c1) {       /* Check & wait the status of UART2 receive complete flag */
        }

        receive_data = u2rb;     /* Receive data read */

    }
}
```

5. Reference

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Hardware Manual

M16C/26, M16C/26A, M16C/28, M16C/29 Group Hardware Manual
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