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# M16C/Tiny Series

# Operation of DMAC (Repeat Transfer Mode)

#### 1. Abstract

In repeat transfer mode of DMAC, choose functions from those listed in Table 1. Operations of the checked items are described below.

#### Table 1. Choosed Functions

ltem	Set-up			
Transfer space	From any address in the 1M bytes space to a fixed address			
	Yes	From a fixed address to any address in the 1M bytes space		
		From a fixed address to a fixed address		
Unit of transfer	t of transfer 8 bits			
	Yes	16 bits		

#### 2. Introduction

The explanation of this issue is applied to the following condition: Applicable MCU: M16C/26, M16C/26A, M16C/28, M16C/29 Group

This program can be used for the other M16C Families which have the same SFR (Special Function Register) as the one in the M16C/26, M16C/26A, M16C/28, M16C/29 However, since some functions may be modified such as added functions, check it in a manual. Execute sufficient evaluation when using this application note.



#### 3. Operation of DMAC

- (1) When software trigger is selected, setting software DMA request bit to "1" generates a DMA transfer request signal.
- (2) If DMAC is active, data transfer starts, and the contents of the address indicated by the DMAi source pointer are transferred to the address indicated by the DMAi forward-direction address pointer. When data transfer starts directly after DMAC becomes active, the value of the DMAi transfer counter reload register is reloaded to the DMAi transfer counter, and the value of the DMAi destination pointer is reloaded by the DMAi forward-direction address pointer. Each time a DMA transfer request signal is generated, 2 byte of data is transferred. The DMAi transfer counter is down counted, and the DMAi forward-direction address pointer is up counted.
- (3) Though DMAi transfer counter is underflowed, DMA enable bit is still "1". The DMA interrupt request bit changes to "1" simultaneously.
- (4) After DMAi transfer counter is underflowed, when the next DMA request is generated, DMA transfer is repeated from (1).

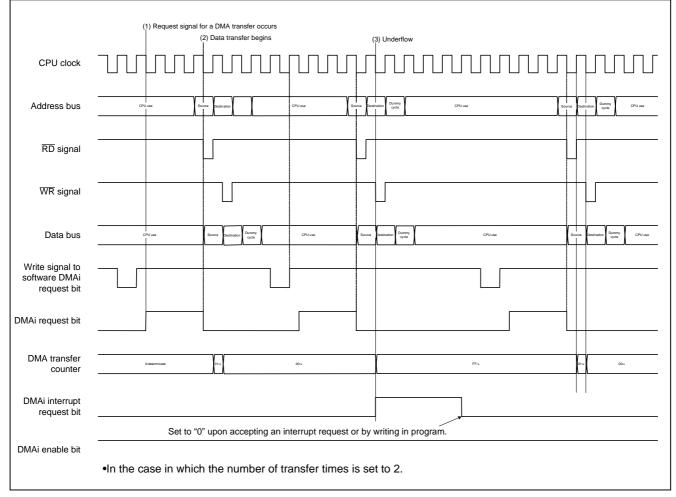


Figure 1 shows the operation timing.

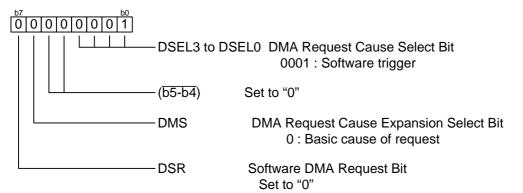
Figure 1. Operation Timing of Repeat Transfer Mode



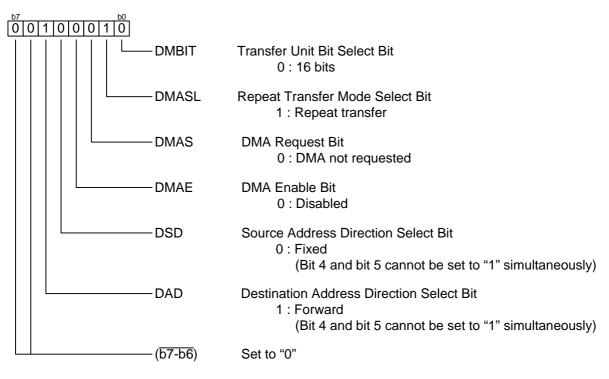
## 3.1 Register Setting

To enable the operation defined in "Section 3. Operation of A/D Converter", the following register settings must be taken place step by step. For detail configuration of each register, please refer to M16C/26 Group hardware manual, M16C/26A Group hardware manual, M16C/28 Group hardware manual, M16C/29 Group hardware manual

(1) Setting DMAi request cause select register

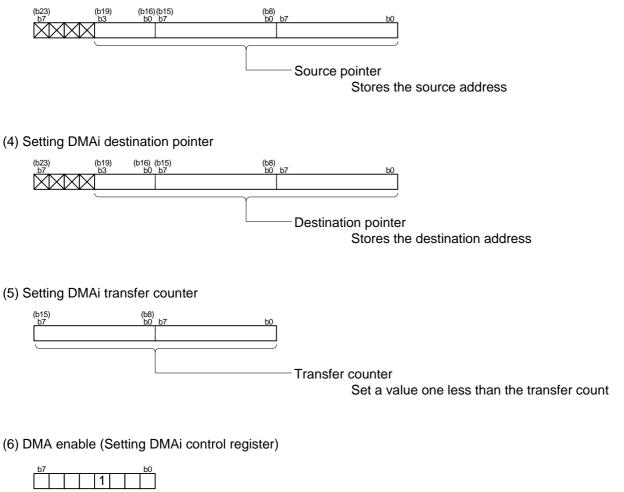


(2) Setting DMAi control register





#### (3) Setting DMAi source pointer



DMAE

DMA Enable Bit 1 : Enabled

(7) When software DMA request bit = "1", start DMA transmission



#### 4. Sample Program

```
*
    FILE NAME :
   CPU : M16C/Tiny series
Function : Operation of DMAC
 *
 *
*
              (repeated transfer mode)
*
    Version
           : 1.00
 *
   Copyright (C)2004, Renesas Technology Corp.
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****
/*******
 * include file
 ************************************
#include "sfr28.h"
/*******
 * Function Definition *
 *********************************
* Global variable declaration
const static unsigned short src_data = 0x55AA;
unsigned short dst_data [8];
/******
* main
*********************************
void main(void) {
   dm0ic = 0;
   dmOsl = 0x01; /* Setting DMA0 request cause select register
             DMA request cause select bit is selected to software trigger
   dm0con = 0x22;
                /* Setting DMA0 control register
                     Transfer unit bit select bit is selected to 16 bit
                     Repeat transfer mode select bit is selected to repeat transfer
                     DMA request bit is set to DMA not request
                     DMA enable bit is set to disable
                     Source address direction select bit is set to fixed
                     Destination address direction select bit is set to forward
                  * /
   sar0_addr.byte.low = (char)(&src_data); /*
sar0_addr.byte.mid = (char)((unsigned long)(&src_data) >> 8 );
                                                         /* Setting DMA0 source pointer */
   sar0_addr.byte.high = (char)((unsigned long)(&src_data) >> 16 );
   /* Setting DMA0 destination pointer */
   dar0_addr.byte.high = (char)((unsigned long)(&dst_data) >> 16 );
                /* Setting DMA0 transfer counter */
   tcr0 = 7;
   dmae_dm0con = 1; /* DMA enabled */
   while (1) {
       while ( !ir_dm0ic )
       {
          dsr_dm0sl = 1;
                           /* Software DMA request bit is set to "1" */
       ir_dm0ic = 0;
                           /* Interrupt request bit is set to "0" */
   }
}
```



## 5. Reference

Renesas Technology Corporation Home Page http://www.renesas.com/

E-mail Support E-mail: csc@renesas.com

Hardware Manual M16C/26, M16C/26A, M16C/28, M16C/29 Group Hardware Manual (Use the latest version on the home page: http://www.renesas.com)

TECHNICAL UPDATE/TECHNICAL NEWS (Use the latest information on the home page: http://www.renesas.com)



## **REVISION HISTORY**

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		Page	Summary		
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