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April 1st, 2010
Renesas Electronics Corporation

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M16C/80 Group

Operation of A-D Converter (in repeat sweep mode 0)

1.0 Abstract

In repeat sweep mode 0, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Choosed functions

Item	Set-up		Item	Set-up	
Operation clock f_{AD}	O	Divided-by-4 f_{AD} / divided-by-2 f_{AD} / f_{AD}	Trigger for starting A-D conversion	O	Software trigger
					Trigger by $\overline{ADTRG}$
Resolution	O	8-bit / 10-bit	Expanded analog input pin	O	Not used
Analog input pin	O	AN_0 and AN_1 (2 pins) / AN_0 to AN_3 (4 pins) / AN_0 to AN_5 (6 pins) / AN_0 to AN_7 (8 pins)			External ope-amp connection mode
			Sample & Hold		Not activated
				O	Activated

2.0 Introduction

Operation (1) Setting the A-D conversion start flag to “1” causes the A-D converter to start the conversion on voltage input to the AN_0 pin.

(2) After the A-D conversion of voltage input to the AN_0 pin is completed, the content of the successive comparison register (conversion result) is transmitted to A-D register 0.

(3) The A-D converter converts all pins selected by the user. The conversion result is transmitted to A-D register i corresponding to each pin every time A-D conversion on the pin is completed. The A-D conversion interrupt request bit does not change.

(4) The A-D converter continues operating until the A-D conversion start flag is set to “0” by software.

Note • In repeat sweep mode 0, the A-D conversion interrupt request bit does not change. By using Timer, it is possible to make it synchronize with the timing which A-D conversion completes, and to read conversion results repeatedly.

Figure 1 shows the operation timing

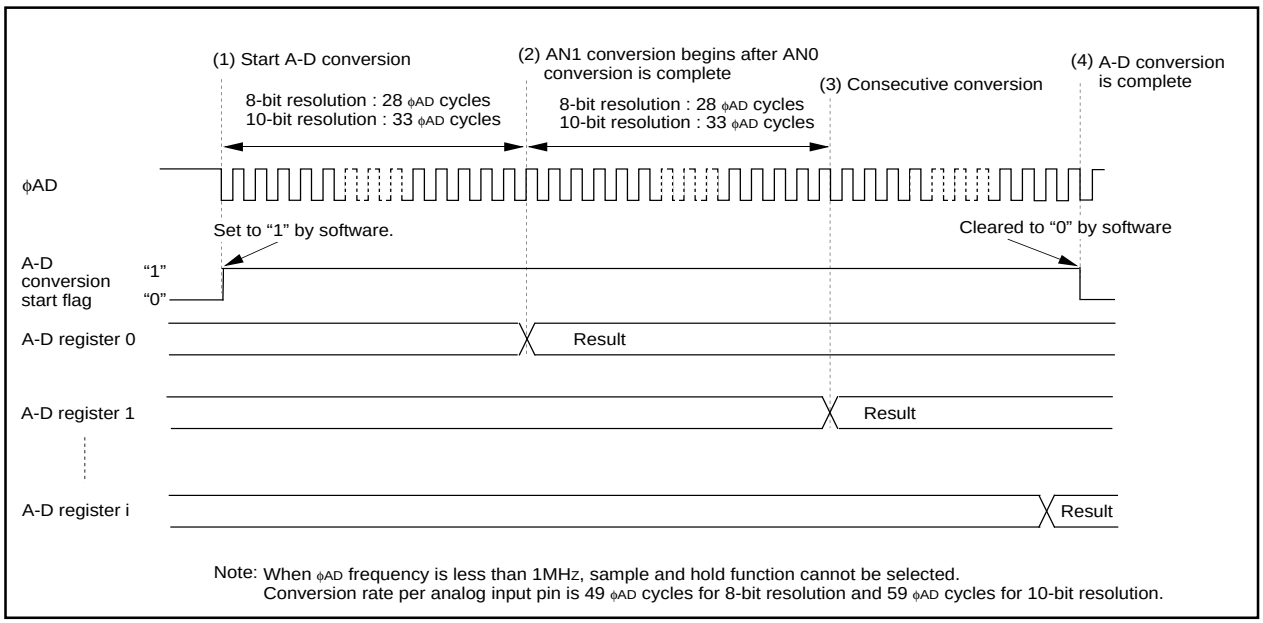
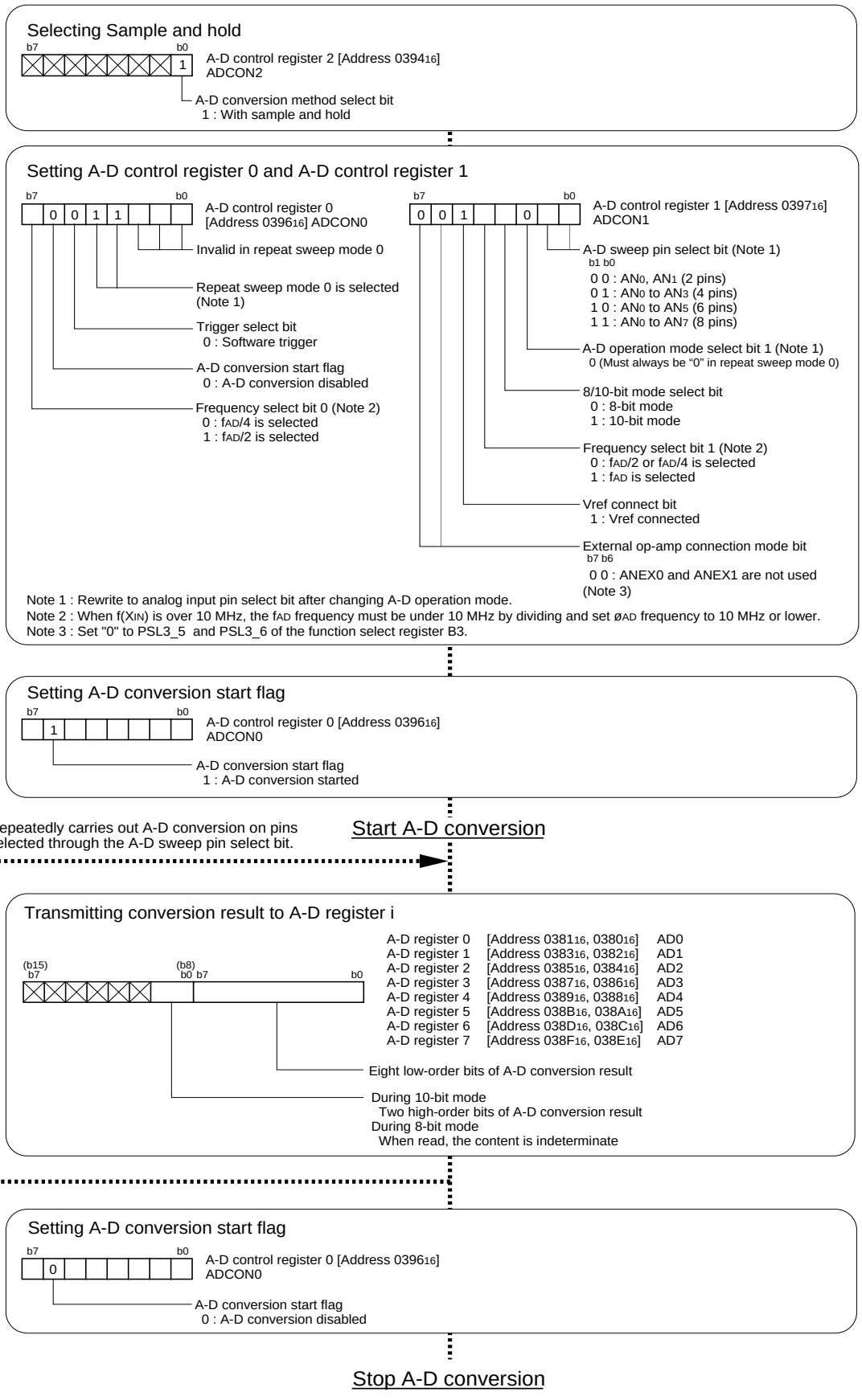


Figure 1. Operation timing of repeat sweep mode 0

3.0 Set-up procedure



4.0 Programming Code

```
;***************************************************************************************
;
;   M16C/80 Program Collection
;
;   FILE NAME : rjj05b0481_src.a30
;   CPU       : M16C/80 Group
;   FUNCTION  : Operation of A-D Converter
;               (in repeat sweep mode 0)
;   HISTORY   : 2004.02.02  Ver 1.00
;
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;
;***************************************************************************************
;***************************************************************************************
;       Include
;***************************************************************************************
        .LIST       OFF             ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr80100.inc    ;Reads the file that defined SFR
        .LIST       ON              ;Starts outputting lines to the assembler list file
;
;***************************************************************************************
;       Symbol definition
;***************************************************************************************
RAM_TOP          .EQU    000400H    ;Start address of RAM
RAM_END          .EQU    002BFFH    ;End address of RAM
ROM_TOP          .EQU    0FFC000H   ;Start address of ROM
FIXED_VECT_TOP   .EQU    0FFFFDCH   ;Start address of fixed vector
;
;
;***************************************************************************************
;       Program area
;***************************************************************************************
;=======================================================================
;       Start up
;=======================================================================
        .SECTION    PROGRAM, CODE  ;Declares section name and section type
        .ORG        ROM_TOP        ;Declares start address
RESET:
        LDC      #RAM_END+1, ISP   ;Sets initial value in stack pointer
        ; Sets Processor mode, System clock and Main clock division
        MOV.B    #03H, prcr        ;Removes protect
        MOV.B    #10000000B, pm0   ; Single-chip mode
        MOV.B    #11000000B, pm1   ; Flash memory version
        MOV.B    #00001000B, cm0   ; Xcin-Xcout High
        MOV.B    #00100000B, cm1   ; Xin-Xout High
        MOV.B    #00010010B, mcd   ; No division mode
        MOV.B    #00H, prcr        ;Protects all registers
;
```

```
;===============================================================================
;       A-D Converter (in repeat sweep mode 0)
;===============================================================================
        ; Selecting sample and hold
        MOV.B    #00000001B, adcon2
;                       +---------;A-D conversion method select bit
;                                  (1:With sample and hold)
        ; Setting A-D control register 0 and A-D control register 1
        MOV.B    #10011000B, adcon0
;                |||||+++---------;Invalid in repeat sweep mode 0
;                |||++------------;Repeat sweep mode 0 is selected
;                ||+--------------;Trigger select bit (0:Software trigger)
;                |+---------------;A-D conversion start flag (0:A-D conversion disabled)
;                +----------------;Frequency select bit 0 (1:fAD/2 is selected)
        MOV.B    #00101011B, adcon1
;                ||||||++---------;A-D sweep pin select bit (11:AN0 to AN7 (8pins))
;                |||||+-----------;A-D operation mode select bit1
;                |||||             (Must always be "0" in repeat sweep mode 0)
;                ||||+------------;8/10-bit mode select bit (1:10-bit mode)
;                |||+-------------;Frequency select bit 1 (0:fAD/2 or fAD/4 is selected)
;                ||+--------------;Vref connect bit (1:Vref connected) (Note)
;                ++---------------;External op-amp connection mode bit
;                                  (00:ANEX0 and ANEX1 are not used) (Note)
        ; Setting the direction register of the relevant port to input
        MOV.B    #00H, pd10        ;AN0-AN7(P100-P107):Analog input pin
        ; (Note) Setting function select register B3 (ANEX0 & ANEX1 are not used)
        BCLR     psl3_5            ;P95:Input peripheral function enabled
        BCLR     psl3_6            ;P96:Input peripheral function enabled
;
;-------------------------------------------------------------------------------
;       Start A-D conversion
;-------------------------------------------------------------------------------
        ; (Note) When the Vref connection bit is changed from 0 to 1,
        ;        start A-D conversion after an elapsing of 1 us or longer.
        MOV.W    #10, R0           ; 10 * 2cy = 20cy = 1 us or longer (@20MHz)
PRE_START:
        NOP
        NOP
        ADJNZ.W  #-1, R0, PRE_START
;
START_AD:
        BSET     adst              ; Setting A-D conversion start flag
;
REPEAT_AD_CNV:
        ;
        ; Processing of reading A-D conversion result
        ; depending on the application program.
        ;
        JMP      REPEAT_AD_CNV
;
;-------------------------------------------------------------------------------
;       Stop A-D conversion
;-------------------------------------------------------------------------------
STOP_AD:
        BCLR     adst              ; A-D conversion stop
;
STOPPED_AD:
        JMP      STOPPED_AD
;
```

```
;===============================================================================
;       Dummy interrupt processing program
;===============================================================================
dummy:
        REIT
;
;*******************************************************************************
;       Setting of fixed vector
;*******************************************************************************
        .SECTION    F_VECT, ROMDATA
        .ORG        FIXED_VECT_TOP
;
        .LWORD    dummy    ;Undefined instruction
        .LWORD    dummy    ;Overflow
        .LWORD    dummy    ;BRK instruction execution
        .LWORD    dummy    ;Address match
        .LWORD    dummy    ;
        .LWORD    dummy    ;Watchdog timer
        .LWORD    dummy    ;
        .LWORD    dummy    ;NMI
        .LWORD    RESET    ;Reset
;
        .END
```

5.0 Reference

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Data Sheet

M16C/80 group Rev. E3

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