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April 1st, 2010
Renesas Electronics Corporation

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M16C/62A Group

Operation of A-D Converter (one-shot mode)

1.0 Abstract

In one-shot mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Chosen functions

Item	Set-up	Item	Set-up
Operation clock ϕ_{AD}	<input type="radio"/> Divided-by-4 f_{AD} / divided-by-2 f_{AD} / f_{AD}	Expanded analog input pin	<input type="radio"/> Not used
Resolution	<input type="radio"/> 8-bit / 10-bit		Either ANEX0 pin or ANEX1 pin
Analog input pin	<input type="radio"/> One of AN0 pin to AN7 pin		External operation amplifier connection mode
Trigger for starting A-D conversion	<input type="radio"/> Software trigger	Sample & Hold	Not activated
	Trigger by \overline{ADTRG}		<input type="radio"/> Activated

2.0 Introduction

Operation (1) Setting the A-D conversion start flag to "1" causes the A-D converter to begin operating.

(2) After A-D conversion is completed, the content of the successive comparison register (conversion result) is transmitted to A-D register i. At this time, the A-D conversion interrupt request bit goes to "1". Also, the A-D conversion start flag goes to "0", and the A-D converter stops operating.

Figure 1 shows the operation timing

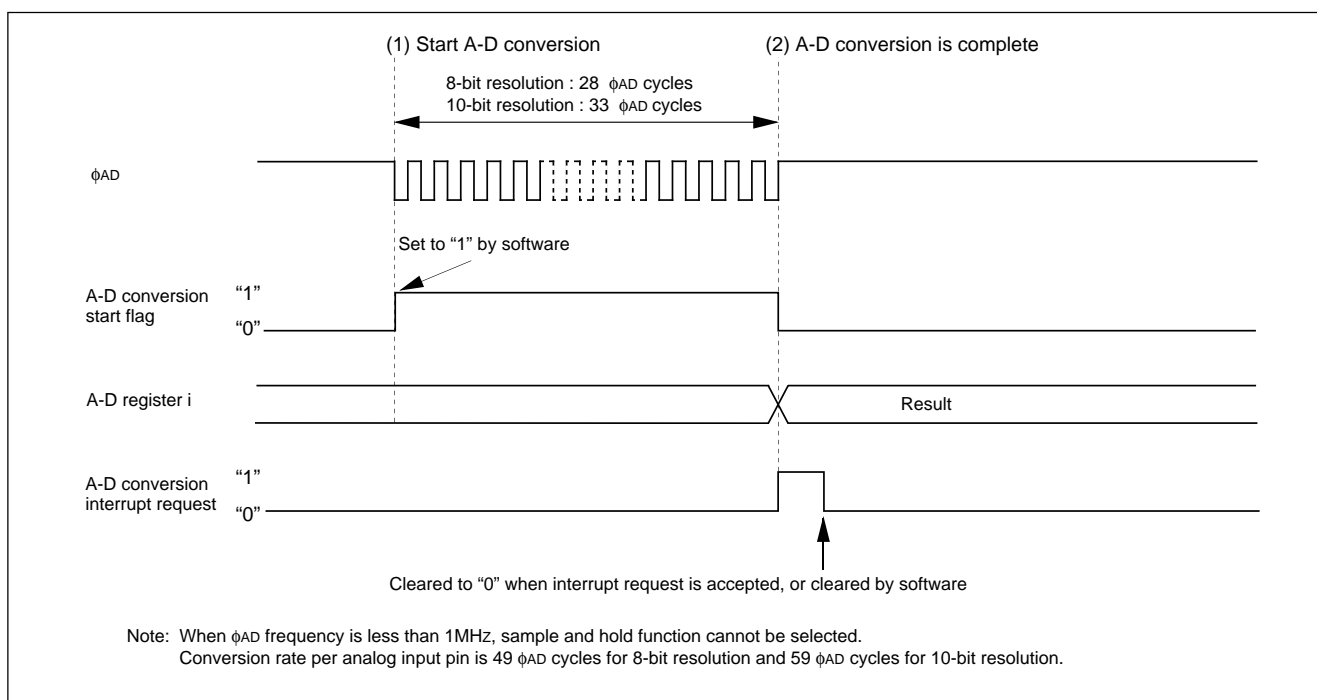
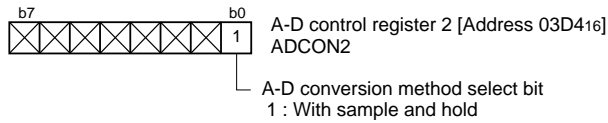


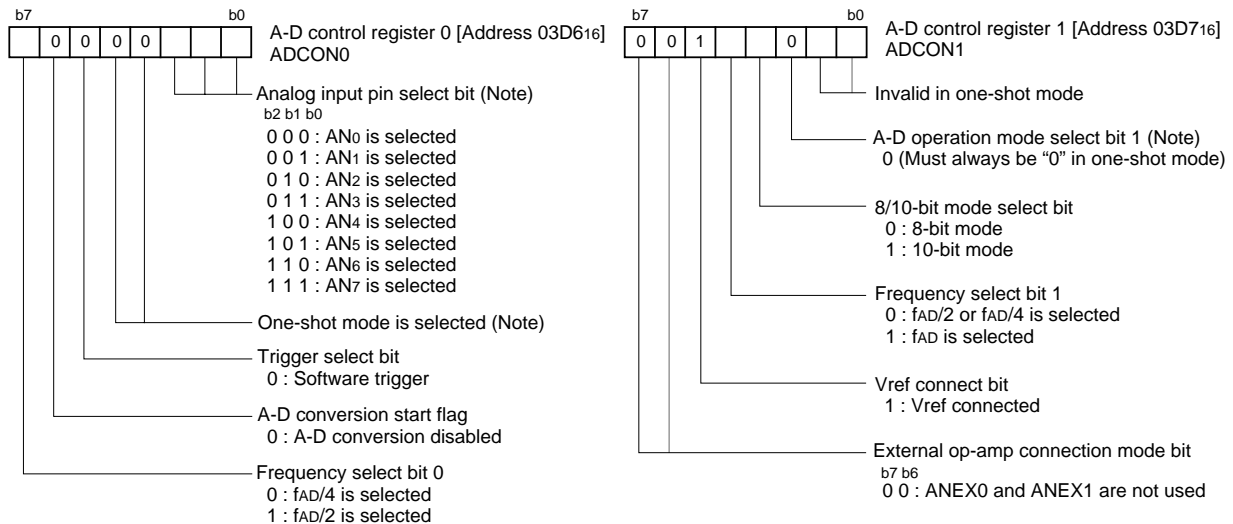
Figure 1. Operation timing of one-shot mode

3.0 Set-up procedure

Selecting Sample and hold

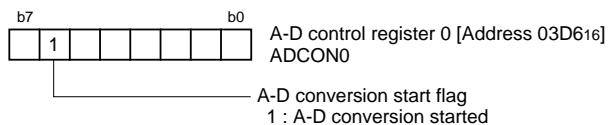


Setting A-D control register 0 and A-D control register 1



Note: Rewrite to analogue input pin select bit after changing A-D operation mode.

Setting A-D conversion start flag



Start A-D conversion

Stop A-D conversion

Reading conversion result



4.0 Programming Code

```

;*****
;
;   M16C/62A Program Collection
;
;   FILE NAME : rjj05b0053_src.a30
;   CPU       : M16C/62A Group
;   FUNCTION  : Operation of A-D Converter
;               (one-shot mode)
;   HISTORY   : 2003.05.16 Ver 1.00
;
;   Copyright(C)2003, Renesas Technology Corp.
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;
;*****
;*****
;   Include
;*****
;*****
;   .LIST      OFF           ;Stops outputting lines to the assembler list file
;   .INCLUDE   sfr62a.inc    ;Reads the file that defined SFR
;   .LIST      ON           ;Starts outputting lines to the assembler list file
;
;*****
;   Symbol definition
;*****
RAM_TOP      .EQU    00400H    ;Start address of RAM
RAM_END      .EQU    00FFFH    ;End address of RAM
ROM_TOP      .EQU    0F8000H   ;Start address of ROM
FIXED_VECT_TOP .EQU    0FFFDCH  ;Start address of fixed vector
;
;*****
;   Allocation of work RAM area
;*****
;*****
;   .SECTION    WORKRAM, DATA
;   .ORG        RAM_TOP
WORKRAM_TOP:
v_AD_result: .BLKW    1        ;A-D conversion result store area
WORKRAM_END:
;
;*****
;   Program area
;*****
;*****
;=====
;   Start up
;=====
;*****
;*****
;   .SECTION    PROGRAM, CODE ;Declares section name and section type
;   .ORG        ROM_TOP      ;Declares start address
RESET:
MOV.B    #03H, prcr          ;Removes protect
;                               ;Set processor mode registers 0 and 1
MOV.B    #00000000B, pm0     ; Single-chip mode
MOV.B    #00000000B, pm1     ; No expansion, No wait
;                               ;Set system clock control registers 0 and 1
MOV.B    #00001000B, cm0     ; Xcin-Xcout High
MOV.B    #00100000B, cm1     ; Xin-Xout High, Main clock is No divison
MOV.B    #00H, prcr          ;Protects all registers
;

```

```

MOV.W    #0, v_AD_result    ;Clear A-D result store area
;=====
;    A-D Converter (one-shot mode)
;=====
MOV.B    #00h, adic          ;Disabled A-D conversion interrupt and
                              ;clear interrupt request bit to "0"
;
MOV.B    #00000001B, adcon2   ;Selecting Sample and hold
                              ;-----+-----;A-D conversion method select bit
                              ;(1:With sample and hold)
MOV.B    #10000000B, adcon0   ;Setting A-D control register 0
;    |||++-----;Analog input pin select bit (000:AN0 is selected)
;    ||+-----;One-shot mode is selected
;    |+-----;Trigger select bit (0:Software trigger)
;    +-----;A-D conversion start flag (0:A-D conversion disabled)
;    +-----;Frequency select bit 0 (1:fAD/2 is selected)
MOV.B    #00101000B, adcon1   ;Setting A-D control register 1
;    |||++-----;Invalid in one-shot mode
;    |||+-----;Must always be "0" in one-shot mode
;    ||+-----;8/10-bit mode select bit (1:10-bit mode)
;    |+-----;Frequency select bit 1 (0:fAD/2 or fAD/4 is selected)
;    +-----;Vref connect bit (1:Vref connected)
;    +-----;External op-amp connection mode bit
;    (00:ANEX0 and ANEX1 are not used)
BCLR     pd10_0               ;Set the direction register of the relevant port to input
                              ;(AN0:Analog input pin)
;
;-----
;    Start A-D conversion
;-----
START_AD:
    BSET     adst              ;Setting A-D conversion start flag
;
WAIT_AD_CNV:
    BTST     ir_adic
    JNC      WAIT_AD_CNV
    BCLR     ir_adic           ;Clear to "0" A-D conversion interrupt request
;
COMPLETE_CNV:
    ; Reading conversion result
    MOV.W    ad0, v_AD_result  ;Read conversion result
    AND.W    #03FFH, v_AD_result ;Mask 10 bits result
;
STOPPED_AD:
    JMP      STOPPED_AD
;

```

```

=====
;      Dummy interrupt processing program
=====
dummy:
    REIT
;
;*****
;      Setting of fixed vector
;*****
    .SECTION    F_VECT, ROMDATA
    .ORG        FIXED_VECT_TOP
;
    .LWORD     dummy    ;Undefined instruction interrupt vector
    .LWORD     dummy    ;Overflow (INT0 instruction) interrupt vector
    .LWORD     dummy    ;BRK instruction interrupt vector
    .LWORD     dummy    ;Address match interrupt vector
    .LWORD     dummy    ;Single-step interrupt vector
    .LWORD     dummy    ;Watchdog timer interrupt vector
    .LWORD     dummy    ;DBC interrupt vector
    .LWORD     dummy    ;NMI interrupt vector
    .LWORD     RESET    ;Sets reset vector
;
    .END

```

5.0 Reference

Renesas Technology Corporation Semiconductor Home page
<http://www.renesas.com/>

Technical Support

E-mail: support_apl@renesas.com

Data Sheet

M16C/62A group Rev. C.1
(Use the latest version on the Home page: <http://www.renesas.com/>)

User's Manual

M16C/62A group Rev. 1.0
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