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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics Corporation

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## M16C/62A Group Memory to Memory DMA Transfer

### 1.0 Abstract

The following are steps for changing both source address and destination address to transfer data from memory to another. The DMA transfer utilizes the workings that assign a higher priority to the DMA0 transfer if transfer requests simultaneously occur in two DMA channels.

Use the following peripheral function:

- Timer mode of timer A
- Two DMAC channels
- One-byte temporary RAM (address 0800<sub>16</sub>)

### 2.0 Introduction

Specifications (1) Transfer the content of memory extending over 128 bytes from address A0000<sub>16</sub> to a 128-byte area starting from address C0000<sub>16</sub>. Transfer the content every time a timer A0 interrupt request occurs.

- (2) Use DMA0 for a transfer from the source to built-in memory, and DMA1 for a transfer from built-in memory to the destination.

#### Operation

- (1) A timer A interrupt request occurs. Though both a DMA0 transfer request and a DMA1 transfer request occur simultaneously, the former is executed first.
- (2) DMA0 receives a transfer request and transfers data from the source to the built-in memory. At this time, the source address is incremented.
- (3) Next, DMA1 receives a transfer request and transfers data involved from built-in memory to the destination. At this time, the destination address is incremented.

Figure 1. shows the operation timing

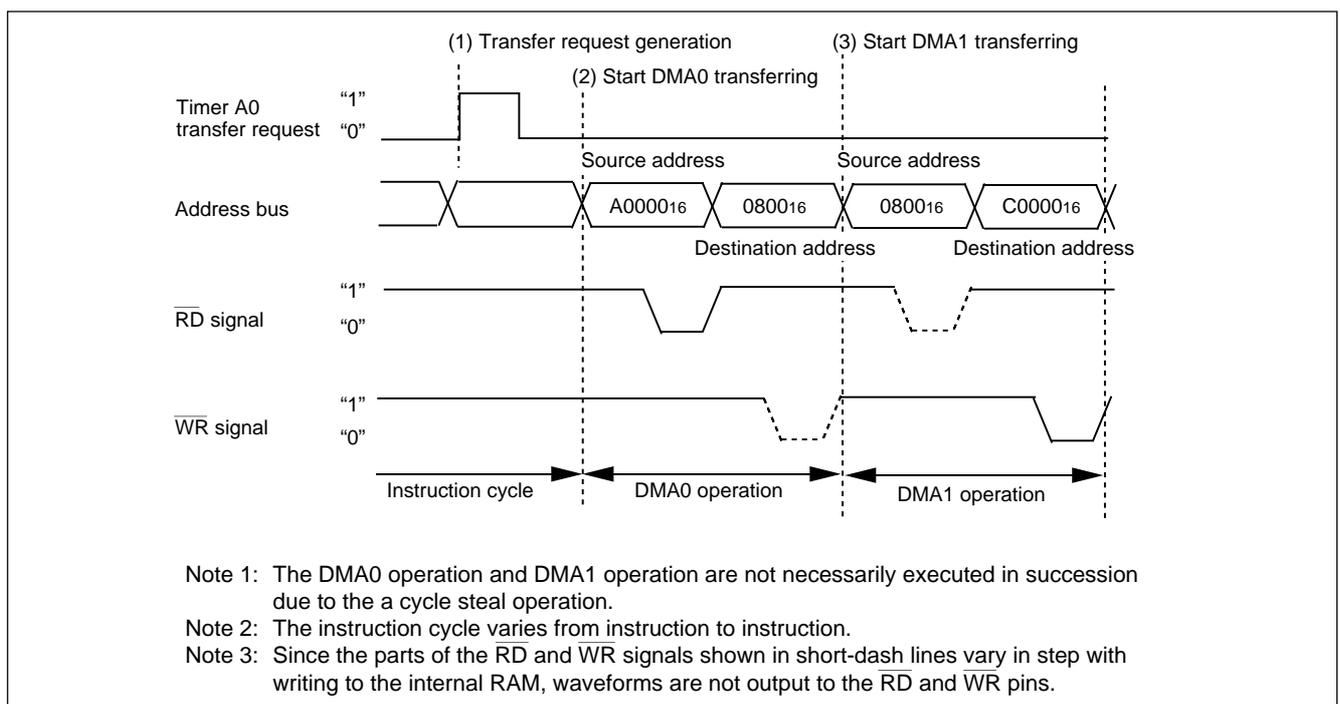
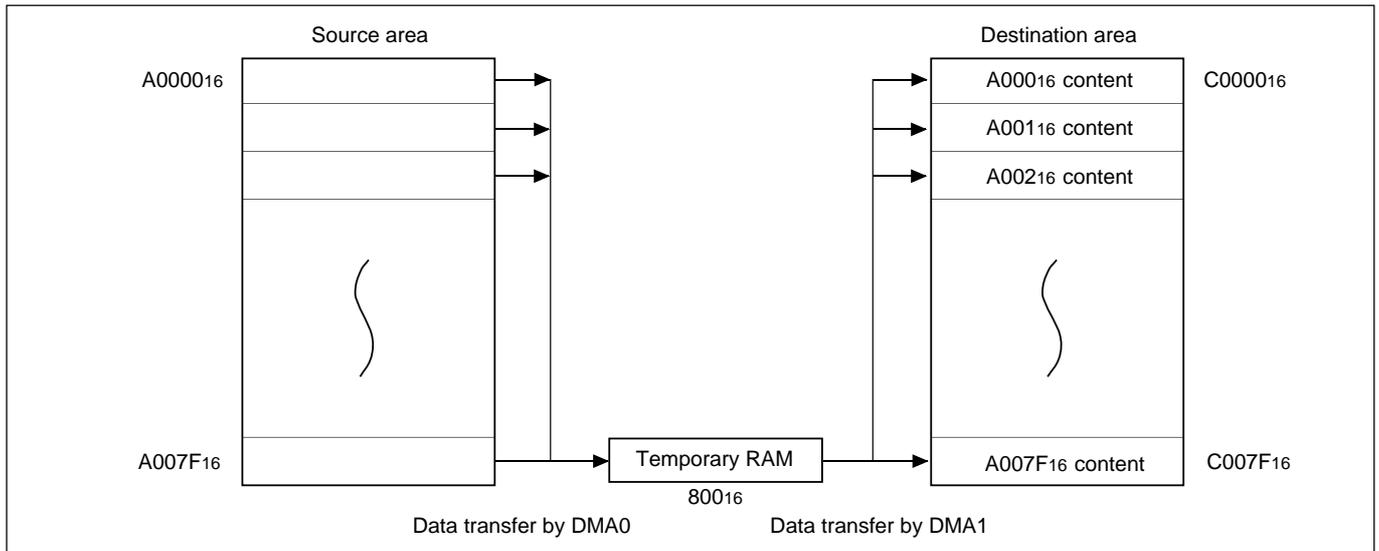


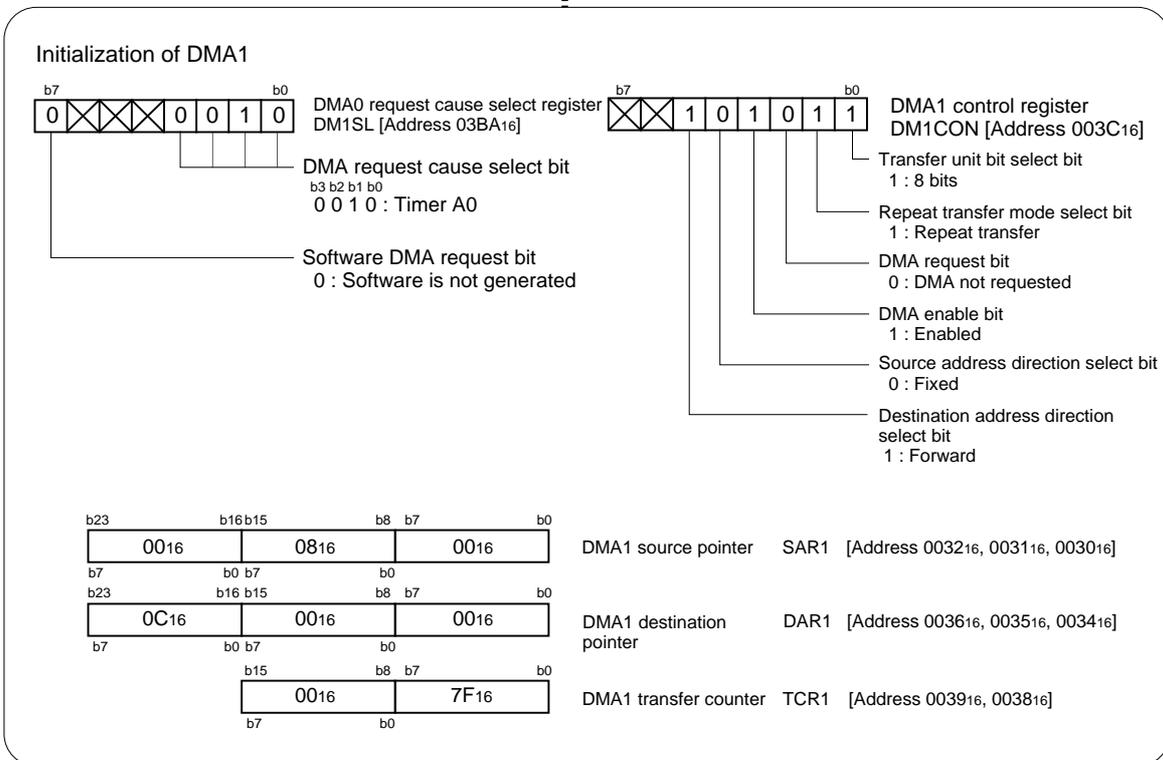
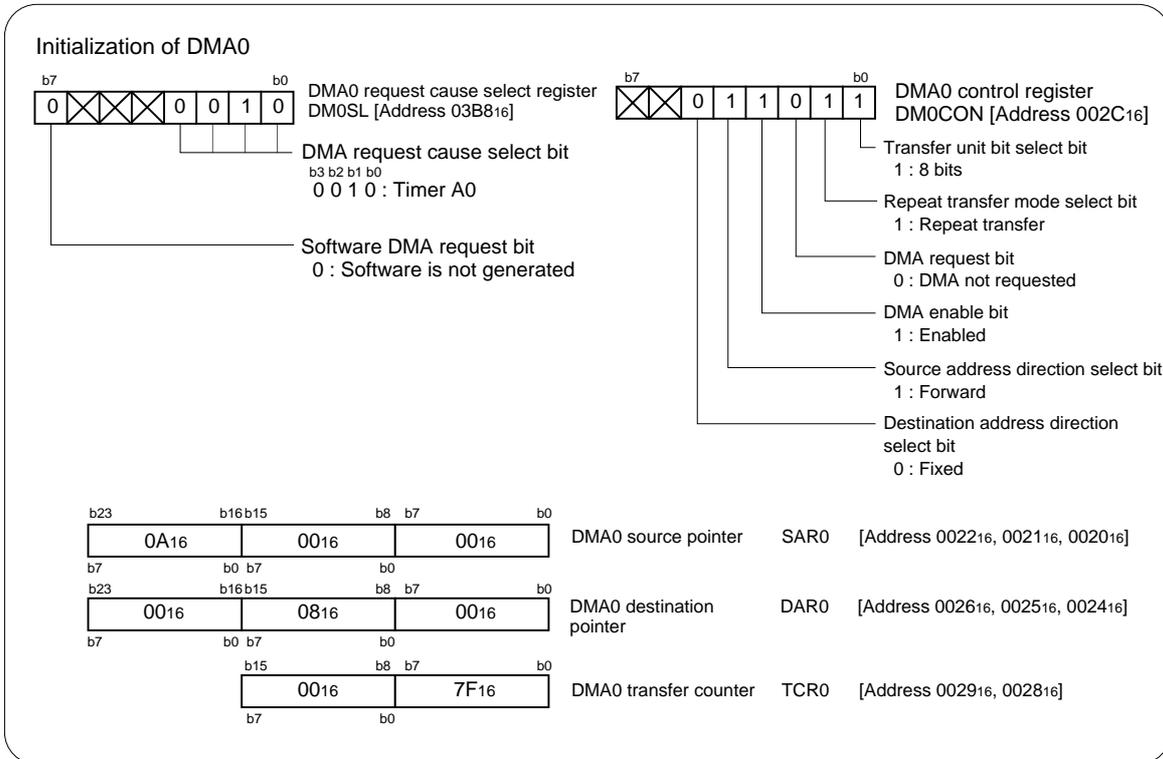
Figure 1. Operation timing of memory to memory DMA transfer

Figure 2 shows the block diagram



**Figure 2. Block diagram of memory to memory DMA transfer**

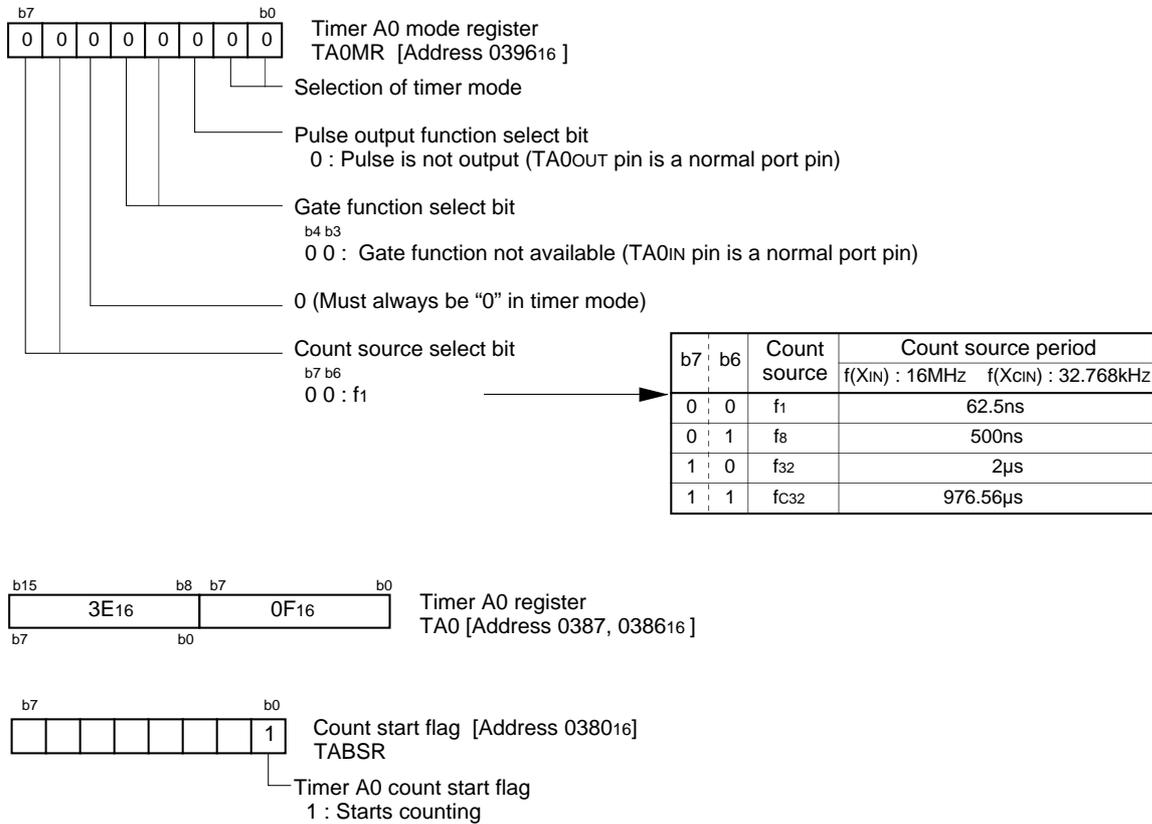
### 3.0 Set-up procedure



Continued to the next page

Continued from the previous page

### Initialization of timer A0



### 4.0 Programming Code

```

;*****
;
; M16C/62A Program Collection
;
; FILE NAME : rjj05b0074_src.a30
; CPU      : M16C/62A Group
; FUNCTION  : DMAC Applications
;            (Memory to Memory DMA Transfer)
; HISTORY  : 2003.05.16 Ver 1.00
;
; Copyright(C)2003, Renesas Technology Corp.
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; All rights reserved.
;
;*****
;*****
; Include
;*****
        .LIST      OFF          ;Stops outputting lines to the assembler list file
        .INCLUDE   sfr62a.inc   ;Reads the file that defined SFR
        .LIST      ON          ;Starts outputting lines to the assembler list file
;
;*****
; Symbol definition
;*****
RAM_TOP      .EQU    00400H    ;Start address of RAM
RAM_END      .EQU    00FFFH    ;End address of RAM
ROM_TOP      .EQU    0F8000H   ;Start address of ROM
FIXED_VECT_TOP .EQU    0FFFDCH  ;Start address of fixed vector
;
A_SRC_MEM    .EQU    0A0000H   ;Top address of source area
A_TMP_MEM    .EQU    00800H    ;Address of temporary area
A_DST_MEM    .EQU    0C0000H   ;Top address of destination area
C_CNT_DMA    .EQU    128       ;DMA transfer counter
;
;*****
; Allocation of work RAM area
;*****
        .SECTION   WORKRAM, DATA
        .ORG       RAM_TOP
;
        .ORG       A_TMP_MEM    ;Temporary RAM area
v_Tmp_mem:   .BLKB   1
;
        .SECTION   DMA_DST, DATA ;Destination area
        .ORG       A_DST_MEM
v_Dst_mem:   .BLKB   (C_CNT_DMA*1)
;

```

```

;*****
;      Program area
;*****
;=====
;      Start up
;=====
      .SECTION    PROGRAM, CODE ;Declares section name and section type
      .ORG        ROM_TOP      ;Declares start address
RESET:
      MOV.B      #03H, prcr     ;Removes protect
                                   ;Set processor mode registers 0 and 1
      MOV.B      #00000001B, pm0 ; Memory expansion mode
      MOV.B      #00000000B, pm1 ; No expansion, No wait
                                   ;Set system clock control registers 0 and 1
      MOV.B      #00001000B, cm0 ; Xcin-Xcout High
      MOV.B      #00100000B, cm1 ; Xin-Xout High, Main clock is No divison
      MOV.B      #00H, prcr     ;Protects all registers
;
      MOV.B      #00001111B, csr ;Set chip select control register
;
;      |||||+-----;CS0 output enable bit (1:Chip select output enabled)
;      |||||+-----;CS1 output enable bit (1:Chip select output enabled)
;      |||||+-----;CS2 output enable bit (1:Chip select output enabled)
;      ||||+-----;CS3 output enable bit (1:Chip select output enabled)
;      ++++-----;CS0 - CS3 are No wait state
;
;

```

```

;=====
;   DMAC
;=====
;-----DMAC0-----
MOV.B   #00010011B, dm0con   ;DMA0 control register
;       |||||+-----;Transfer unit bit select bit (1:8bit)
;       |||||+-----;Repeat transfer mode select bit (1:Repeat transfer)
;       |||||+-----;DMA request bit (0:DMA not requested)
;       |||+-----;DMA enable bit (0:Disabled)
;       |+-----;Source address direction select bit (1:Forward)
;       +-----;Destination address direction select bit (0:Fixed)
MOV.B   #00000010B, dm0sl    ;DMA0 request cause select register
;       |  ++++-----;DMA request cause select bit (0010:TimerA0)
;       +-----;software DMA request bit (0:Software is not generated)
;
MOV.W   #(A_SRC_MEM & 0FFFFh), sar0   ;Set DMA0 source pointer M,L
MOV.B   #(A_SRC_MEM >> 16),   sar0h   ;Set DMA0 source pointer H
;
MOV.W   #(v_Tmp_mem & 0FFFFh), dar0   ;Set DMA0 destination pointer M,L
MOV.B   #(v_Tmp_mem >> 16),   dar0h   ;Set DMA0 destination pointer H
;
MOV.B   #(C_CNT_DMA-1), tcr0          ;DMA0 transfer counter
;
;-----DMAC1-----
MOV.B   #00100011B, dmlcon   ;DMA1 control register
;       |||||+-----;Transfer unit bit select bit (1:8bit)
;       |||||+-----;Repeat transfer mode select bit (1:Repeat transfer)
;       |||||+-----;DMA request bit (0:DMA not requested)
;       |||+-----;DMA enable bit (0:Disabled)
;       |+-----;Source address direction select bit (0:Fixed)
;       +-----;Destination address direction select bit (1:Forward)
MOV.B   #00000010B, dmlsl    ;DMA1 request cause select register
;       |  ++++-----;DMA request cause select bit (0010:TimerA0)
;       +-----;Software DMA request bit (0:Software is not generated)
;
MOV.W   #(v_Tmp_mem & 0FFFFh), sar1   ;Set DMA1 source pointer M,L
MOV.B   #(v_Tmp_mem >> 16),   sar1h   ;Set DMA1 source pointer H
;
MOV.W   #(A_DST_MEM & 0FFFFh), dar1   ;Set DMA1 destination pointer M,L
MOV.B   #(A_DST_MEM >> 16),   dar1h   ;Set DMA1 destination pointer H
;
MOV.B   #(C_CNT_DMA-1), tcrl          ;DMA1 transfer counter
;
;-----TimerA0-----
MOV.B   #00000000B, ta0mr     ;TimerA0 mode register
;       |||||+-----;Selection of timer mode
;       |||||+-----;Pulse is not output (TA0OUT pin is a normal port pin)
;       |||+-----;Gate function not available (TA0OUT pin is a normal port pin)
;       ||+-----;Must always be "0" in timer mode
;       ++-----;Count source f1
MOV.W   #3E0FH, ta0          ;TimerA0 register (993u @16MHz, f1)
;
;-----Enable DMAC0 & DMAC1-----
MOV.B   #00011011B, dm0con
;       |-----;Clear DMA request bit simultaneously
;       +-----;DMA enable bit (1:Enabled)
MOV.B   #00101011B, dmlcon
;       |-----;Clear DMA request bit simultaneously
;       +-----;DMA enable bit (1:Enabled)
MOV.B   #00000001B, tabsr     ;Count start flag
;       +-----;TimerA0 count start flag (1:Starts counting)
;
MAIN:
JMP     MAIN

```

```

;
;=====
;   Dummy interrupt processing program
;=====
dummy:
    REIT
;
;*****
;   DMA source area ( ROM area )
;*****
    .SECTION    SRC_DMA, ROMDATA
    .ORG        A_SRC_MEM
; DMA transmission data
    .BYTE  01h,  02h,  03h,  04h,  05h,  06h,  07h,  08h
    .BYTE  09h,  0Ah,  0Bh,  0Ch,  0Dh,  0Eh,  0Fh,  10h
    .BYTE  11h,  12h,  13h,  14h,  15h,  16h,  17h,  18h
    .BYTE  19h,  1Ah,  1Bh,  1Ch,  1Dh,  1Eh,  1Fh,  20h
    .BYTE  21h,  22h,  23h,  24h,  25h,  26h,  27h,  28h
    .BYTE  29h,  2Ah,  2Bh,  2Ch,  2Dh,  2Eh,  2Fh,  30h
    .BYTE  31h,  32h,  33h,  34h,  35h,  36h,  37h,  38h
    .BYTE  39h,  3Ah,  3Bh,  3Ch,  3Dh,  3Eh,  3Fh,  40h
    .BYTE  41h,  42h,  43h,  44h,  45h,  46h,  47h,  48h
    .BYTE  49h,  4Ah,  4Bh,  4Ch,  4Dh,  4Eh,  4Fh,  50h
    .BYTE  51h,  52h,  53h,  54h,  55h,  56h,  57h,  58h
    .BYTE  59h,  5Ah,  5Bh,  5Ch,  5Dh,  5Eh,  5Fh,  60h
    .BYTE  61h,  62h,  63h,  64h,  65h,  66h,  67h,  68h
    .BYTE  69h,  6Ah,  6Bh,  6Ch,  6Dh,  6Eh,  6Fh,  70h
    .BYTE  71h,  72h,  73h,  74h,  75h,  76h,  77h,  78h
    .BYTE  79h,  7Ah,  7Bh,  7Ch,  7Dh,  7Eh,  7Fh,  80h
;
;*****
;   Setting of fixed vector
;*****
    .SECTION    F_VECT, ROMDATA
    .ORG        FIXED_VECT_TOP
;
    .LWORD  dummy      ;Undefined instruction interrupt vector
    .LWORD  dummy      ;Overflow (INT0 instruction) interrupt vector
    .LWORD  dummy      ;BRK instruction interrupt vector
    .LWORD  dummy      ;Address match interrupt vector
    .LWORD  dummy      ;Single-step interrupt vector
    .LWORD  dummy      ;Watchdog timer interrupt vector
    .LWORD  dummy      ;DBC interrupt vector
    .LWORD  dummy      ;NMI interrupt vector
    .LWORD  RESET      ;Sets reset vector
;
    .END

```

## 5.0 Reference

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### Data Sheet

M16C/62A group Rev. C.1  
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M16C/62A group Rev. 1.0  
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