Renesas RA Family

Flash Memory Programming

Introduction

This application note details the process of programming flash memory in Renesas RA MCUs. Note the following convention in this document:

Target Devices

Renesas RA MCUs use two kinds of flash memory, MF3 and RV40.

MF3 Code Flash double access type Two Code Flash are controlled at the same time. (64-bit I/O)	RA2A1, RA4M1, RA4W1
RV40F Phase 2	RA6M1, RA6M2, RA6M3, RA6T1

Contents

1. MF3 Type Flash

MF3 type flash memory is found in Renesas RA Family products such as RA2A1, RA4M1 and RA4W1.

1.1 Overview

Table 1 describes the specifications of the MF3 flash memory.

Table 1. MF3 Flash Memory Specifications

Item	Description
Memory space	• User area: Up to 1 MB • Data area: Up to 16 KB
Block Size	User area: 2 KB, Data area: 1 KB
Program/Erase unit	Program: User area: 64 bits, Data area: 8 bits Erase: User area 2 KB, Data area: 1 KB
Software commands	• The following describes the commands of the boot mode or the self-programming mode: — Blank check — Block erase — Chip erase — Program — Consecutive read — Access window information program — Start-up area information and security program — OCDID program • Checksum can be also executed in boot mode. — Suspend/resume of the block erase command can be also executed during the self-programming mode.
On-board programming	Boot mode (SCI) • Channel 9 of the serial communications interface (SCI9) is used for asynchronous serial communication. • The user area and data area are rewritable. Boot mode (USB interface) [Except RA2A1] • Channel 0 of the USB 2.0 function (USB0) module is used. • The user area and data area are rewritable. • The flash memory can be rewritable in self-powered or bus-powered mode. • A personal computer can be connected using only a USB cable. Self-programming mode
Off-board programming	The user area and data area are rewritable using a flash programmer compatible with this MCU.
Debug IF	JTAG/SWD [Except RA2A1] SWD (depending on the product's specification) [RA2A1]
ID code protect	The software commands are protected by the ID code.
Start-up program protection	The boot area (16 KB) can be swapped in 8-KB units.
Area protection	The area protection by the access window is possible in the boot mode and the self-programming mode.
Background Operation (BGO)	Reading the code flash while the programming the data flash

1.1.1 Block Configuration of the Code Flash

[RA2A1]

The maximum size of the code flash is 256 KB. The sector size is 1 KB. Figure 1 shows the block configuration of the code flash.

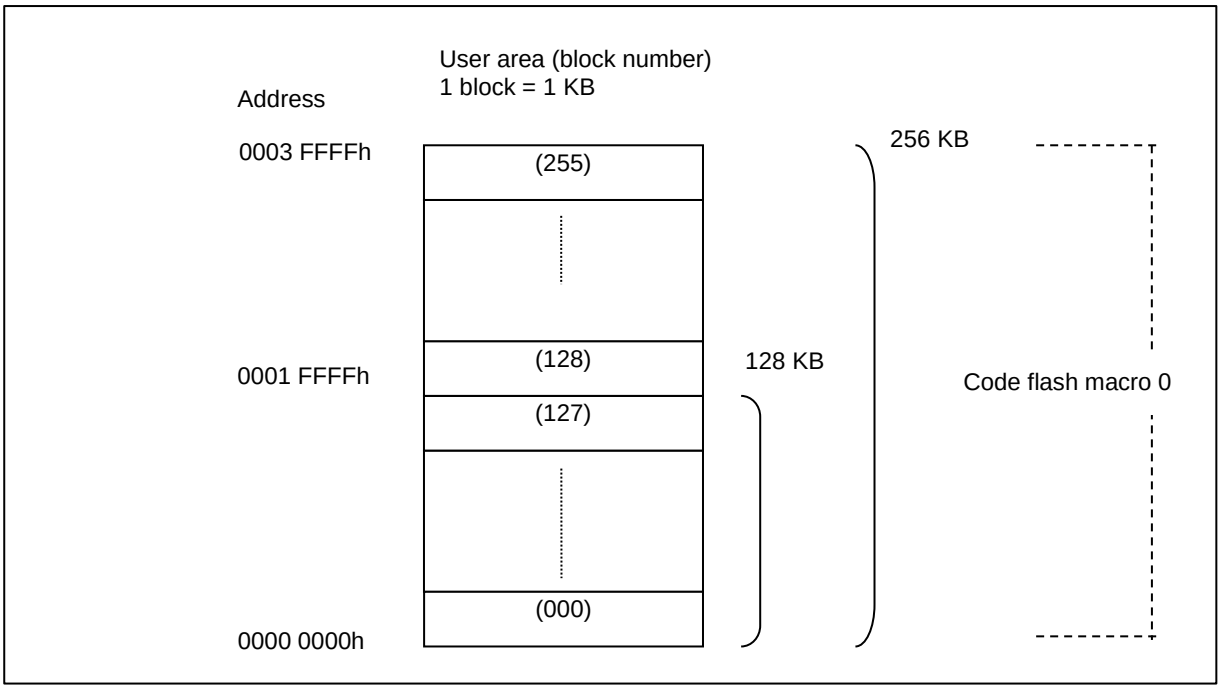


Figure 1. Block Configuration of Code Flash (max 256 KB, depending on the product's specification)

Table 2. Correspondence between the Size of the Code Flash and the Address

Size of the Code Flash	CPU (Read) Address	P/E Address *1	Number of Blocks
256 KB	0000 0000h - 0003 FFFFh	0000 0000h - 0003 FFFFh	0 - 255
128 KB	0000 0000h - 0001 FFFFh	0000 0000h - 0001 FFFFh	0 - 127
64 KB	0000 0000h - 0000 FFFFh	0000 0000h - 0000 FFFFh	0 - 63
32 KB	0000 0000h - 0000 7FFFh	0000 0000h - 0000 7FFFh	0 - 31

Note: 1. The code flash hard macrocell consists of one macrocell of 128 KB. In executing the blank check, block erase, and consecutive read command, the start and end address must be set in each code flash macrocell.

[Products except RA2A1]

The maximum size of the code flash is 1 MB. The sector size is 2 KB. Figure 2 shows the block configuration of the code flash.

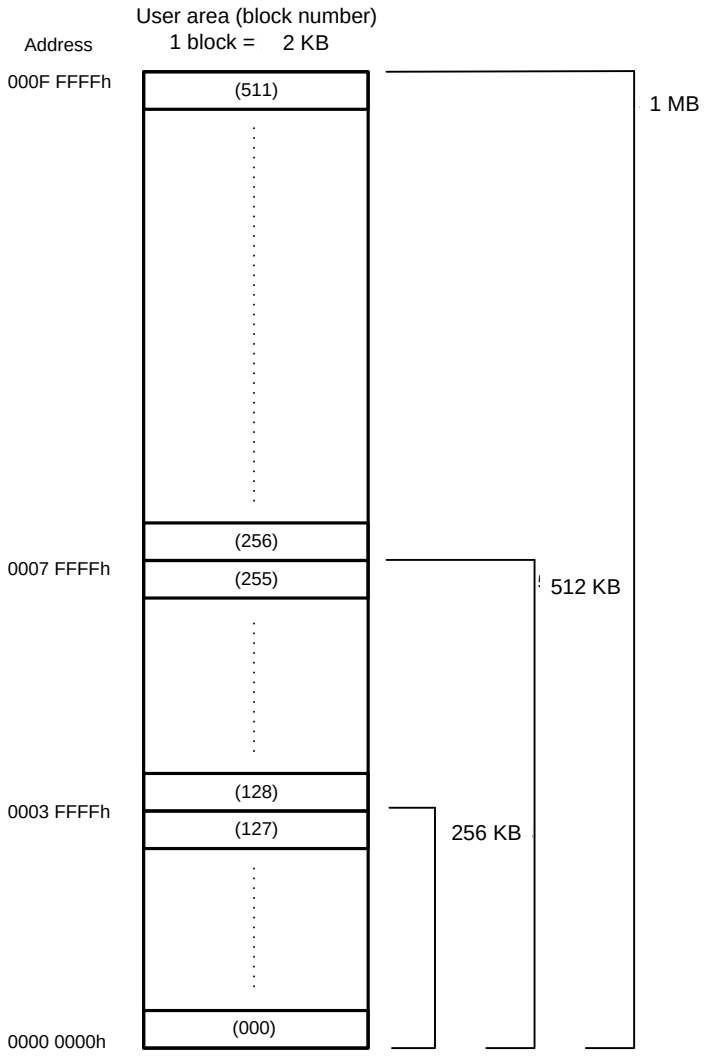


Figure 2. Block Configuration of Code Flash (max 1 MB, depending on the product's specification)

Table 3. Correspondence between the Size of the Code Flash and the Address

Size of the Code Flash	CPU (Read) Address	P/E address *1	Number of Blocks
1 MB	0000 0000h - 000F FFFFh	0000 0000h - 000F FFFFh	0 - 511
512 KB	0000 0000h - 0007 FFFFh	0000 0000h - 0007 FFFFh	0 - 255
256 KB	0000 0000h - 0003 FFFFh	0000 0000h - 0003 FFFFh	0 - 127

Note: 1. In case of the 1-MB product, the code flash hard macrocell consists of two macrocells of 512 KB. In executing the blank check, block erase, and consecutive read command, the start and end address must be set in each code flash macrocell.

1.1.2 Block Configuration of the Data Flash

1.1.2.1 Products with 1 Data Flash Macrocell [RA2A1]

The maximum size of the data flash is 8 KB. The sector size is 1 KB. Figure 3 shows the block configuration of the data flash.

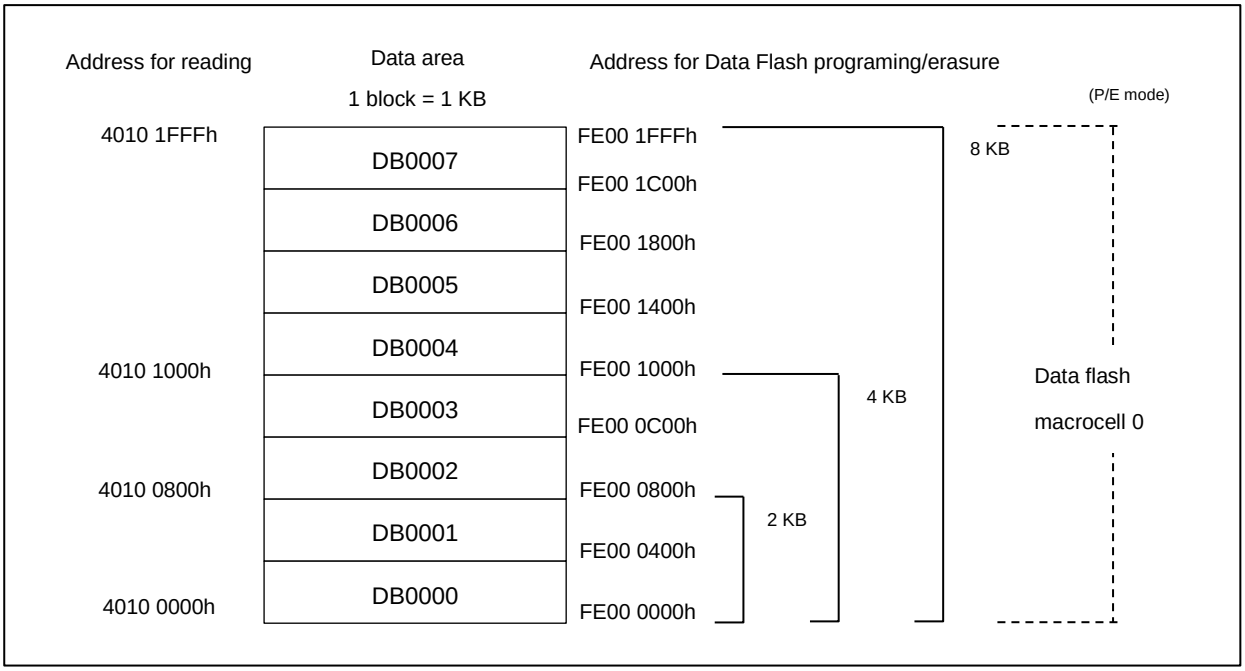


Figure 3. Block Configuration of the Data Flash (Example of 8 KB)

Table 4. Correspondence between the Size of the Data Flash and the Address

Size of the Data Flash	CPU (Read) Address	P/E Address *1	Number of Blocks
8 KB	4010 0000 – 4010 1FFFh	FE00 0000h – FE00 1FFFh	0 - 7
4 KB	4010 0000h – 4010 0FFFh	FE00 0000h – FE00 0FFFh	0 - 3
2 KB	4010 0000h – 4010 07FFh	FE00 0000h – FE00 07FFh	0 -1

Note: 1. The data flash hard macrocell consists of one macrocell of 4 KB. In executing the blank check, block erase, and consecutive read command, the start and end address must be set in each code flash macrocell.

1.1.2.2 Products with 2 Data Flash Macrocells [Products except RA2A1]

The maximum size of the data flash is 16 KB. The sector size is 1 KB. Figure 4 shows the block configuration of the data flash.

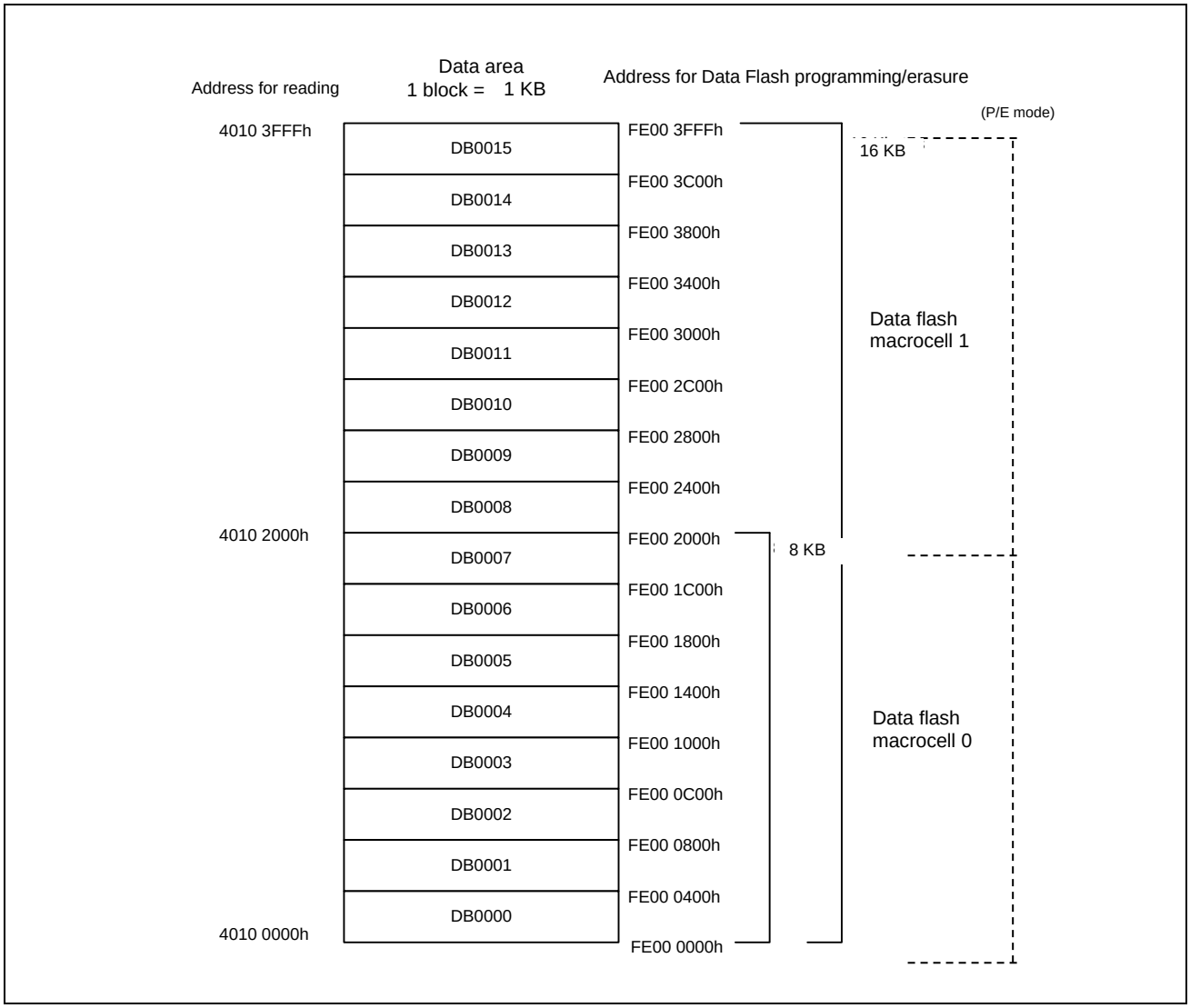


Figure 4. Block Configuration of Data Flash (Example of 16 KB)

Table 5. Correspondence between the Size of the Data Flash and the Address

Size of the data flash	CPU (Read) address	P/E Address *1	Number of Blocks
16 KB	4010 0000h – 4010 3FFFh	FE00 0000h – FE00 3FFFh	0 - 15
8 KB	4010 0000h – 4010 1FFFh	FE00 0000h – FE00 1FFFh	0 - 7

Note: 1. The data flash hard macrocell consists of two macrocells of 8 KB. In executing the blank check, block erase, and consecutive read command, the start and end address must be set in each code flash macrocell.

1.2 Register Descriptions

Table 6. List of Registers

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Reference Page
407E C090h	FLASH	Data Flash Control Register	DFLCTL	8	8	10
407E FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	10
407E C180h	FLASH	Protection Unlock Register	FPR	8	8	11

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Reference Page
407E C184h	FLASH	Protection Unlock Status Register	FPSR	8	8	12
407E C100h	FLASH	Flash P/E Mode Control Register	FPMCR	8	8	12
407E C1D8h	FLASH	Flash Initial Setting Register	FISR	8	8	14
407E C124h	FLASH	Flash Reset Register	FRESETR	8	8	15
407E C104h	FLASH	Flash Area Select Register	FASR	8	8	16
407E C114h	FLASH	Flash Control Register	FCR	8	8	16
407E C1DCh	FLASH	Flash Extra Area Control Register	FEXCR	8	8	18
407E C110h	FLASH	Flash Processing Start Address Register H	FSARH	16	16	20
407E C108h	FLASH	Flash Processing Start Address Register L	FSARL	16	16	21
407E C120h	FLASH	Flash Processing End Address Register H	FEARH	16	16	21
407E C118h	FLASH	Flash Processing End Address Register L	FEARL	16	16	22
407E C130h	FLASH	Flash Write Buffer Register L0	FWBL0	16	16	22
407E C138h	FLASH	Flash Write Buffer Register H0	FWBH0	16	16	23
407E C140h	FLASH	Flash Write Buffer Register L1 [Products except RA2A1]	FWBL1	16	16	23
407E C144h	FLASH	Flash Write Buffer Register H1 [Products except RA2A1]	FWBH1	16	16	23
407E C188h	FLASH	Flash Read Buffer Register L0	FRBL0	16	16	24
407E C190h	FLASH	Flash Read Buffer Register H0	FRBH0	16	16	24
407E C148h	FLASH	Flash Read Buffer Register L1 [Products except RA2A1]	FRBL1	16	16	25
407E C14Ch	FLASH	Flash Read Buffer Register H1 [Products except RA2A1]	FRBH1	16	16	25
407E C128h	FLASH	Flash Status Register00	FSTATR00	16	16	25
407E C13Ch	FLASH	Flash Status Register01	FSTATR01	16	16	27
407E C1F0h	FLASH	Flash Status Register02	FSTATR2	16	16	28
407E C12Ch	FLASH	Flash Status Register1	FSTATR1	8	8	29
407E C1E8h	FLASH	Flash Error Address Monitor Register H	FEAMH	16	16	29
407E C1E0h	FLASH	Flash Error Address Monitor Register L	FEAML	16	16	30
407E C1C0h	FLASH	Flash Start-Up Setting Monitor Register	FSCMR	16	16	30
407E C1C8h	FLASH	Flash Access Window Start Address Monitor Register	FAWSMR	16	16	31
407E C1D0h	FLASH	Flash Access Window End Address Monitor Register	FAWEMR	16	16	31
407E FFC0h	FLASH	Flash Wait Cycle Register [RA2A1]	FLWAITR	8	8	32

1.2.1 Data Flash Control Register (DFLCTL)

Address(es) 407E_C090h

	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	-	-	DFLEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DFLEN	data flash Access Enable	0: Access to the data flash is disabled (*1) 1: Access to the data flash is enabled (*1)	R/W
b7-b1	-	Reserved	Read data is 0.	R

The DFLCTL register enables or disables access (reading, programming, and erasing) to the data flash. After setting the DFLCTL.DFLEN bit, Data Flash STOP recovery time (tDSTOP) is necessary before reading the data flash or entering the data flash P/E mode.

(*1) It is necessary that DFLCTL.DFLEN bit is set to 1 before issuing the Start-up area information and security program, Access window information program, and OCDID program command.

1.2.2 Flash P/E Mode Entry Register (FENTRYR)

Address(es) 407E_FFB2h

	b15	b14	b13	b12	b11	b10	b9	b8
	FEKEY[7:0]							
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
	FENTRYD	0	0	0	0	0	0	FENTRY0
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FENTRY0	Code Flash P/E Mode Entry 0	0: The code flash is the read mode. 1: The code flash is the P/E mode	R/W
b6-b1	—	Reserved	Read data is 0.	R
b7	FENTRYD	Data flash P/E Mode Entry	0: The data flash is the read mode. 1: The data flash is the P/E mode.	R/W
b15-b8	FEKEY[7:0]	Key Code	The FEKEY [7:0] bits protect from unauthorized setting of FENTRY0 bit or FENTRYD bit. Setting AAh to FEKEY [7:0] allows setting the FENTRY0 bit or the FENTRYD bit. The FEKEY [7:0] bits are read as 00h.	R/W

To program the code flash or the data flash, either the FENTRYD or FENTRY0 bit are set to 1 to enter the P/E mode. Clearing the FENTRY0 bit or the FENTRYD bit allow the code flash or the data flash to the read mode, but it is necessary to confirm the read value of these bits before reading.

Refer to section 1.5.1, Sequencer Modes, for details on P/E mode and read mode.

Set/Clear condition of the FENTRY0 bit

[Setting condition]

- Set AA01h to the FENTRYR register when the FENTRYR register is 0000h.

[Clearing conditions]

- Data is written by byte access.
- Data other than AAh is set to the FEKEY[7:0] bits and data is written to the FENTRYR register.
- Set AA00h to the FENTRYR register.
- Data is written to the FENTRYR register while the FENTRYR register is a value other than 0000h.

Set/Clear condition of the FENTRYD bit

[Setting condition]

- Set AA80h to the FENTRYR register when the FENTRYR register is 0000h.

[Clearing conditions]

- Data is written by byte access.
- Some data other than AAh is set to the FEKEY [7:0] bits and data is written to the FENTRYR register.
- Set AA00h to the FENTRYR register.
- Data is written to the FENTRYR register while the FENTRYR register is a value other than 0000h.

1.2.3 Protection Unlock Register (FPR)

Address(es) 407E C180h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset	X	X	X	X	X	X	X	X

x: Undefined

This register protects the FPMCR register from being rewritten inadvertently when the CPU runs out of control. Writing to the FPMCR register is enabled only when the following procedure is used to access the register.

Procedure to unlock protection

1. Write A5h to the FPR register.
2. Write a set value to the FPMCR register.
3. Write the inverted set value to the FPMCR register.
4. Write a set value to the FPMCR register again.

When a procedure other than the above is used to write data, the FPSR.PERR flag is set to 1.

1.2.4 Protection Unlock Status Register (FPSR)

Address(es) 407E C184h

	b7	b6	b5	b4	b3	b2	b1	b0
	0	0	0	0	0	0	0	PERR
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PERR	Protect Error Flag	0: No error 1: An error occurred.	R
b7-b1	-	Reserved	These bits are read as 0.	R

PERR Flag (Protect Error Flag)

When the FPMCR register is not accessed as described in the procedure to unlock protection, data is not written to the register and this flag is set to 1.

[Setting condition]

- The FPMCR register is not accessed as described in the procedure to unlock protection.

[Clearing conditions]

- The FPMCR register is accessed according to the procedure to unlock protection described in section 1.2.3, Protection Unlock Register (FPR).

1.2.5 Flash P/E Mode Control Register (FPMCR)

Address(es) 407E C100h

	b7	b6	b5	b4	b3	b2	b1	b0
	FMS2	LVPE	-	FMS1	RPDIS	-	FMS0	-
Value after reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	-	Reserved	This bit is read as 0.	R
b1	FMS0	Flash Operating Mode Select 0	(FMS2 FMS1 FMS0) 0 0 0: Read mode 0 1 1: Discharge mode 1 1 1 1: Discharge mode 2 1 0 1: Code Flash P/E mode 0 1 0: Data flash P/E mode Settings other than above are prohibited.	R/W
b2	-	Reserved	This bit is read as 0.	R
b3	RPDIS	Code Flash P/E Disable	0: The programming of the code flash is enabled 1: The programming of the code flash is disabled	R/W
b4	FMS1	Flash Operating Mode Select 1	Refer to the description of the FMS0 bit.	R/W
b5	-	Reserved	This bit is read as 0.	R
b6	LVPE	Low-Voltage P/E Mode Enable	0: Low-voltage programming is disabled 1: Low-voltage programming is enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b7	FMS2	Flash Operating Mode Select 2	Refer to the description of the FMS0 bit.	R/W

The FPMCR register is to set the operating mode of the flash memory.

The FPMCR register is protected from the unauthorized setting. Refer to section 1.2.3, Protection Unlock Register (FPR) for details on how to unlock the protection.

FMS0, FMS1, and FMS2 Bits (Flash Operating Mode Select 0 to Flash Operating Mode Select 2)

These bits set the operating mode of the flash memory.

[How to enter the code flash from the read mode to the code flash P/E mode]

1. Set the FMS2 bit = 0, the FMS1 bit = 1, the FMS0 bit = 1, and the RPDIS bit = 0.
2. Wait for the P/E mode transition time (tDIS, refer to Electrical Characteristics).
3. Set the FMS2 bit = 1, the FMS1 bit = 1, the FMS0 bit = 1, and the RPDIS bit = 0.
4. Set the FMS2 bit = 1, the FMS1 bit = 0, the FMS0 bit = 1, and the RPDIS bit = 0.
5. Wait for the mode setup time (tMS, refer to Electrical Characteristics).

[How to enter the code flash from the code flash P/E mode to the read mode]

1. Set the FMS2 bit = 1, the FMS1 bit = 1, the FMS0 bit = 1, and the RPDIS bit = 0.
2. Wait for the read mode transition time (refer to Electrical Characteristics).
3. Set the FMS2 bit = 0, the FMS1 bit = 1, the FMS0 bit = 1, and the RPDIS bit = 0.
4. Set the FMS2 bit = 0, the FMS1 bit = 0, the FMS0 bit = 0, and the RPDIS bit = 1.

[How to enter the data flash from the read mode to the data flash P/E mode]

1. Set the FMS2 bit = 0, the FMS1 bit = 1, the FMS0 bit = 0, and the RPDIS bit = 0.

[How to enter the data flash from the data flash P/E mode to the read mode]

1. Set the FMS2 bit = 0, the FMS1 bit = 0, the FMS0 bit = 0, and the RPDIS bit = 1.
2. Wait for the read mode transition time (refer to Electrical Characteristics).

RPDIS Bit (Code Flash P/E Disable)

This bit protects the code flash from the unauthorized programming. Setting this bit to 0 allows the code flash to be programmed.

LVPE Bit (Low-Voltage P/E Mode Enable)

Setting the LVPE bit allows the flash macrocell to be programmed in low-voltage mode.

1.2.6 Flash Initial Setting Register (FISR)

Address(es) 407E C1D8h

	b7	b6	b5	b4	b3	b2	b1	b0
	SAS[1:0]		0	PCKA[4:0]				
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4-b0	PCKA[4:0]	Peripheral Clock Notification	These bits set the frequency of the FlashIF clock. FCLK [Products except RA2A1], ICLK [RA2A1]	R/W
b5	-	Reserved	This bit is read as 0.	R
b7-b6	SAS[1:0]	Start-Up Area Select	(b7, b6) (0 X): The start-up area is selected according to the start-up area settings of the extra area. (1 0): The start-up area is switched to the default area temporarily. (1 1): The start-up area is switched to the alternate area temporarily.	R/W

x: Don't care

Note: The FISR register can be set/cleared only in the P/E mode, and furthermore the SAS [1:0] bit can be set/cleared when the FSPR is 1. The FSPR bit is the protection flag of the access window and stored in the extra area.

PCKA [4:0] Bits (Peripheral Clock Notification)

These bits are used to set the frequency of the FlashIF clock (FCLK [Products except RA2A1], ICLK [RA2A1]). The H/W sequencer for the flash programming executes the commands according to the PCKA [4:0] bits. For that reason, it is necessary to set the frequency to the PCKA [4:0] before the execution of the programming and not to change during the programming.

Note that the wrong frequency setting causes the flash macrocell to be damaged.

The following describes how to set the PCKA [4:0] register when the frequency is not an integral number (for example, 31.5 MHz).

[When the frequency is higher than 4 MHz]

Set a rounded-up value for a non-integer frequency.

For example, set 32 MHz (PCKA bit = 11111b) when the frequency is 31.5 MHz.

[When the frequency is 4 MHz or lower]

Do not use a non-integer frequency. Use the frequency of 1, 2, 3, or 4 MHz.

Table 7. Frequency Settings

FlashIF Clock Frequency [MHz]	PCKA [4:0] Bit Setting	FlashIF Clock Frequency [MHz]	PCKA [4:0] Bit Setting	FlashIF Clock Frequency [MHz]	PCKA [4:0] Bit Setting
32	11111b	31	11110b	30	11101b
29	11100b	28	11011b	27	11010b
26	11001b	25	11000b	24	10111b
23	10110b	22	10101b	21	10100b
20	10011b	19	10010b	18	10001b
17	10000b	16	01111b	15	01110b
14	01101b	13	01100b	12	01011b
11	01010b	10	01001b	9	01000b
8	00111b	7	00110b	6	00101b
5	00100b	4	00011b	3	00010b
2	00001b	1	00000b	-	-

SAS [1:0] Bits (Start-Up Area Select)

These bits are used to select the start-up area. To change the start-up area, the following three methods can be used.

1. When selecting the start-up area according to the start-up area settings of the extra area with the SAS [1:0] bits set to 00b or 01b, the start-up area is selected according to the start-up area settings of the extra area. The settings are enabled after a reset is released.
2. When switching the start-up area to the default area temporarily when 10b is written to the SAS [1:0] bits, the start-up area is switched to the default area immediately after data is written to the register, regardless of the start-up area settings of the extra area.
   When a reset is generated after this, the area is selected according to the start-up area settings of the extra area.
3. When switching the start-up area to the alternative area temporarily when 11b is written to the SAS [1:0] bits, the start-up area is switched to the alternative area, regardless of the start-up area settings of the extra area.
   When a reset is generated after this, the area is selected according to the start-up area settings of the extra area.

1.2.7 Flash Reset Register (FRESETR)

Address(es) 407E C124h

	b7	b6	b5	b4	b3	b2	b1	b0
	0	0	0	0	0	0	0	FRESET
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FRESET	Software Reset of the registers	0: 1: The registers related to the flash programming are reset.	R/W
b7-b1	-	Reserved	These bits are read as 0.	R

FRESET Bit (Flash Reset)

When this bit is set to 1, the FASR, FSARH, FSARL, FEARH, FEARL, FWBH0/1, FWBL0/1, FCR, and FEXCR registers are reset. Setting this bit to 0 allows the corresponding registers to release from the reset state. Software commands are not allowed while the FRESET bit is 1.

1.2.8 Flash Area Select Register (FASR)

Address(es) 407E C104h

	b7	b6	b5	b4	b3	b2	b1	b0
								EXS
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	EXS	Extra Area Select	0: User area or data area 1: Extra area	R/W
b7-b1	-	Reserved	These bits are read as 0.	R

Note: The FASR register can be set/cleared only in the P/E mode.

EXS Bit (Extra Area Select)

Set this bit to 1 when programming the extra area using the FEXCR register.

Set this bit to 0 when not programming the extra area.

1.2.9 Flash Control Register (FCR)

Address(es) 407E C114h

	b7	b6	b5	b4	b3	b2	b1	b0
	OPST	STOP	-	DRC	CMD [3:0]			
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3-b0	CMD	Software Command Setting	b3 b0 0 0 0 1: Program 0 0 1 1: Blank check 0 1 0 0: Block erase 0 1 0 1: Consecutive read 0 1 1 0: Chip erase Settings other than above are prohibited.*1	R/W
b4	DRC	Data Read Completion	0: Data is not read or next data is requested. 1: Data reading is completed.	R/W
b5	-	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	STOP	Forced Processing Stop	When this bit is set to 1, the processing being executed can be forcibly stopped.	R/W
b7	OPST	Processing Start	0: Processing stops. 1: Processing starts.	R/W

Note: 1. This does not include writing 00h to the FCR register when the FSTATR1.FRDY bit is 1.
Note: The FCR register can be set/cleared only in the P/E mode and is not allowed to be reset by the FRESETR register while the software command is being executed.

CMD [3:0] Bits (Software Command Setting)

The following describes the function of each software command.

[Program]
Writing data of the FWBH0/1 and FWBL0/1 registers to the flash macrocell to the address pointed by the FSARH and FSARL registers.

[Blank check]
Confirms that the flash macrocell is in the blank state (not yet programmed) from the start address pointed by the FSARH and FSARL register to the end address pointed by the FEARH and FEARL register. The blank check command can execute within one flash macrocell. When the products have multiple flash macrocells, the blank check command must be executed every flash macrocell. Note that the blank check result cannot guarantee that the flash memory is erased.

[Block erase]
Erasing block of the flash memory

Set the start address of the target erasure block in the FSARH and FSARL registers, and set the end address of the target erasure block in the FEARH and FEARL registers. If a setting other than the above is made, erasure may not be executed correctly. The block erase command is allowed to execute within the one of flash macrocell. When the products have multiple flash macrocells, the block erase command must be executed every flash macrocell.

[Consecutive read]
Read the flash macrocell from the start address pointed by the FSARH and FSARL register to the end address pointed by the FEARH and FEARL register, and the read data is stored to the FRBH and FRBL register. The consecutive read command is allowed to execute within the one of flash macrocell. When the products have multiple flash macrocells, the consecutive read command must be executed every flash macrocell.

[Chip erase]
Erasing all block of the flash macrocell

Set the start address of the target erasure block in the FSARH and FSARL registers, and set the end address of the target erasure block in the FEARH and FEARL registers. If a setting other than the above is made, erasure may not be executed correctly. The chip erase command is allowed to execute within the one of flash macrocell. When the products have multiple flash macrocells, the chip erase command must be executed every flash macrocell.

DRC Bit (Data Read Completion)

After executing the consecutive read command and reading the FRBH and FRBL registers, writing 1 to the DRC bit completes the processing for reading the data. Writing 0 to the DRC bit starts reading the next data.

STOP Bit (Forced Processing Stop)

This bit is to stop the execution of the erase command or the blank check command.

After setting 1 to the STOP bit, it is necessary to wait until the FSTATR1.FRDY bit becomes 1 (processing completed) before setting the OPST bit to 0.

OPST Bit (Processing Start)

This bit is to start the command set to the CMD [2:0] bits. Setting the OPST bit to 0 terminates the execution of the command after the FRDY bit of the FSTATR1 register becomes 1, and it is necessary to confirm the FRDY bit to 0.

Note that no commands can be executed when the ID authorization for the flash programmer has failed.

Note that the program and the block erase and the read commands cannot be executed when the address of each commands points the area protected by the access window.

1.2.10 Flash Extra Area Control Register (FEXCR)

Address(es) 407E C1DCh

	b7	b6	b5	b4	b3	b2	b1	b0
	OPST	-	-	-	-	CMD[2:0]		
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2-b0	CMD[2:0]	Software Command Setting	b2 b0 0 0 1: Start-up area selection and security setting 0 1 0: Access window information program 0 1 1: OCDID1 program 1 0 0: OCDID2 program 1 0 1: OCDID3 program 1 1 0: OCDID4 program Settings other than above are prohibited.*1	R/W
b6-b3	-	Reserved	These bits are read as 0. The write value should be 0.	R
b7	OPST	Processing Start	0: Processing stops. 1: Processing starts.	R/W

Note: 1. This does not include writing 00h to the FEXCR register when the FSTATR1.EXRDY bit is 1.
Note: That the FEXCR register can be set/cleared only in the P/E mode, and cannot be reset by the FRESETR register while the software command is being executed.

The FEXCR register programs the extra area 0. Before execution of each command, it is necessary to set data to the FWBL0 and the FWBH0 register.

In the case of programming by the FEXCR register, the programming area is erased automatically before a program operation. Therefore, it is not necessary to erase beforehand.

CMD [2:0] Bits (Software Command Setting)

These bits select the software command (“start-up area selection and security setting” or “access window information program” or “OCDID program”). The following describes the function of each software command.

[Start-up area selection and security setting]

Setting data to the FWBL0 register, this command is allowed to select the start-up area from the default area (8 KBKB) to the alternative area (next 8 KB) and set the security. Refer to the section 1.3 in details.

- Bit 8 of the FWBL0 register is 0: the alternative area (next 8 KB) is selected as the start-up area.
- Bit 8 of the FWBL0 register is 1: the default area (8 KB) is selected as the start-up area.
- Bit 14 of the FWBL0 register is 0:
  - The access window cannot be updated because the access window information program command cannot be executed.
  - The start-up area cannot be changed.
  - Data of the SAS bits of the FISR register cannot be changed.

Note that the start-up area selection and security setting command cannot set 1 to the corresponding bit of the extra area after setting 0 to the corresponding bit of the extra area.

The following describes the extra bit mapping for the start-up area selection and security setting.

Address (P/E): 0000_0008h

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FSPR *1	*1	*1		*1	*1	BTFLG								

Note: *1. Once 0 is set as data in these bits, it cannot be changed to 1.

[Access window information program]

This command is to set the access window used for area protection. The program command and block erase command and consecutive read command to the protected area cannot be executed. The chip erase command cannot be executed when the access window is set (the start block address of the access window is not equal to the end one). It is necessary to set the start block address of the access window to the FWBL0 register (b0 to b11) and the next block address of the end block address of the access window to the FWBH0 register (b0 to b11) before the execution of the access window information program command. When the start address and the end address are set to the same value, all areas of the code flash can be accessed. When the start address is larger than the end block address, all areas of the code flash cannot be accessed.

The FWBL0.bit11 for the start block address must be set to 0 when the access window is set (the end block address of the access window is larger than the start one).

[Products except RA2A1] The FWBL0.bit0 and the FWBH0.bit0 for the access window must be set to 0.

The following describes the extra bit mapping for Access window information program.

Address (P/E): 0000_0010h

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
				FAWE[11:0]											
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
				FAWS[11:0]											

[OCDID1-4 program]

These commands set the OCDID [127:0].

Table 8. OCDID Settings

Command	OCDID	FWBH0	FWBL0
OCDID1 program	OCDID [31:0].	OCDID [31:16]	OCDID [15:0]
OCDID2 program	OCDID [63:32]	OCDID [63:48]	OCDID [47:32]
OCDID3 program	OCDID [95:64].	OCDID [95:80]	OCDID [79:64]
OCDID4 program	OCDID [127:96]	OCDID [127:112]	OCDID [111:96]

The following describes the extra bit mapping for OCDID1-4 program.

Address (P/E): 0000_0018h

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
OCDID[31:16]															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
OCDID[15:0]															

Address (P/E): 0000_0020h

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
OCDID[63:48]															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
OCDID[47:32]															

Address (P/E): 0000_0028h

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
OCDID[95:80]															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
OCDID[79:64]															

Address (P/E): 0000_0030h

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
OCDID[127:112]															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
OCDID[111:96]															

OPST Bit (Processing Start)

This bit is to start the command set to the CMD [2:0] bits. Setting the OPST bit to 0 terminates the execution of the command after the EXRDY bit of the FSTATR1 register becomes 1, and it is necessary to confirm the EXRDY bit to 0.

1.2.11 Flash Processing Start Address Register H (FSARH)

Address(es) 407E C110h

	b15	b14	b13	b12	b11	b10	b9	b8
								0
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
	0	0	0	0				
Value after reset	0	0	0	0	0	0	0	0

Note: FSARH register can be set/cleared only in the P/E mode.

1.2.12 Flash Processing Start Address Register L (FSARL)

Address(es) 407E C108h

	b15	b14	b13	b12	b11	b10	b9	b8
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset	0	0	0	0	0	0	0	0

Note: The FSARL register can be set/cleared only in the P/E mode.

Set the FSARH and FSARL register to the start address of the software command. When this register is read while executing a software command set by the FEXCR register, an undefined value is read. After execution of the program command, the sequencer of the software command increments data automatically. The auto-increment function of the program command eliminates setting the next address to the FSARH and FSARL register when the next address is consecutive address. The following describes the increment unit.

The code flash: +8h [Products except RA2A1]

The code flash: +4h [RA2A1]

Data flash: +1h

Refer to Figure 1 and Figure 2 for details on the addresses of the flash memory.

1.2.13 Flash Processing End Address Register H (FEARH)

Address(es) 407E C120h

	b15	b14	b13	b12	b11	b10	b9	b8
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset	0	0	0	0	0	0	0	0

Note: The FEARH register can be set/cleared only in the P/E mode.

1.2.14 Flash Processing End Address Register L (FEARL)

Address(es) 407E C118h

	b15	b14	b13	b12	b11	b10	b9	b8
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset	0	0	0	0	0	0	0	0

Note: The FEARL register can be set/cleared only in the P/E mode.

Set the FEARH and FEARL register the end address of the blank check, the block erase, the chip erase and the consecutive read command. When the FEARH and FEARL registers are read while executing a software command set by the FEXCR register, an undefined value is read.

Refer to Figure 1 and Figure 2 for details on the addresses of the flash memory.

1.2.15 Flash Write Buffer Register L0 (FWBL0)

Address(es) 407E C130h

	b15	b14	b13	b12	b11	b10	b9	b8
	WDATA[15:8]							
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
	WDATA[7:0]							
Value after reset	0	0	0	0	0	0	0	0

Note: The FWBL0 register can be set/cleared only in the P/E mode.

1.2.16 Flash Write Buffer Register H0 (FWBH0)

Address(es) 407E C138h

	b15	b14	b13	b12	b11	b10	b9	b8
	WDATA[31:24]							
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
	WDATA[23:16]							
Value after reset	0	0	0	0	0	0	0	0

Note: The FWBH0 register can be set/cleared only in the P/E mode.

[Products except RA2A1]

1.2.17 Flash Write Buffer Register L1 (FWBL1)

Address(es) 407E C140h

	b15	b14	b13	b12	b11	b10	b9	b8
	WDATA[47:40]							
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
	WDATA[39:32]							
Value after reset	0	0	0	0	0	0	0	0

Note: The FWBL1 register can be set/cleared only in the P/E mode.

[Products except RA2A1]

1.2.18 Flash Write Buffer Register H1 (FWBH1)

Address(es) 407E C144h

	b15	b14	b13	b12	b11	b10	b9	b8
	WDATA[63:56]							
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
	WDATA[55:48]							
Value after reset	0	0	0	0	0	0	0	0

Note: The FWBH0 register can be set/cleared only in the P/E mode.

The FWBL0, FWBH0, FWBL1 and FWBH1 registers set program data of the program command, the Start-up selection and security setting command, the access window information program command and the OCDID program command. The following describes how to set data according to each command

Register	What is set to the register
FWBH1 FWBL1	Bit 63-32 of the programming data for the code flash of RA4M1 and RA4W1 products
FWBH0 FWBL0	• Bit 31-0 of the programming data of the program command for the code flash. • Bit 7-0 of the programming data of the program command for the data flash. • Bit 31-0 of the programming data of the start-up selection and security setting command, the access window information program command and the OCDID program command.

1.2.19 Flash Read Buffer Register L0 (FRBL0)

Address(es) 407E C188h

	b15	b14	b13	b12	b11	b10	b9	b8
	RDATA[15:8]							
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
	RDATA[7:0]							
Value after reset	0	0	0	0	0	0	0	0

The FRBL0 register stores bit 15 to bit 0 of the read data of the code flash or the data flash read when the consecutive read command is executed.

When the data flash is read, 00h is stored to bit 15-8.

1.2.20 Flash Read Buffer Register H0 (FRBH0)

Address(es) 407E C190h

	b15	b14	b13	b12	b11	b10	b9	b8
	RDATA[31:24]							
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
	RDATA[23:16]							
Value after reset	0	0	0	0	0	0	0	0

The FRBH0 register stores bit 31-16 of read data of the code flash when the consecutive read command is executed.

[Products except RA2A1]

1.2.21 Flash Read Buffer Register L1 (FRBL1)

Address(es) 407E C148h

	b15	b14	b13	b12	b11	b10	b9	b8
	RDATA[47:40]							
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
	RDATA[39:32]							
Value after reset	0	0	0	0	0	0	0	0

The FRBL1 register stores bit 47-32 of read data of the code flash when the consecutive read command is executed. The FRBH1 register is dedicated for the RA4M1 and RA4W1 products.

[Products except RA2A1]

1.2.22 Flash Read Buffer Register H1 (FRBH1)

Address(es) 407E C14Ch

	b15	b14	b13	b12	b11	b10	b9	b8
	RDATA[63:56]							
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
	RDATA[55:48]							
Value after reset	0	0	0	0	0	0	0	0

The FRBH1 register stores bit 63-48 of read data of the code flash when the consecutive read command is executed. The FRBH1 register is dedicated for the RA4M1 and RA4W1 products.

1.2.23 Flash Status Register 00 (FSTATR00)

Address(es) 407E C128h

	b15	b14	b13	b12	b11	b10	b9	b8
	0	0	0	0	0	0	0	0
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	EILGLERR	ILGLERR	BCERR0	PRGERR01	PRGERR0	ERERR0
Value after reset	X	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ERERR0	Erase Error Flag 0	0: Erasure terminates normally. 1: An error occurred during erasure.	R
b1	PRGERR0	Program Error Flag 0	0: Programming terminates normally. 1: An error occurred during programming.	R
b2	PRGERR01	Program Error Flag 01	0: Programming by the FEXCR register terminates normally. 1: An error occurred during programming.	R
b3	BCERR0	Blank Check Error Flag 0	0: Blank checking terminates normally. 1: An error occurred during blank checking.	R
b4	ILGLERR	Illegal Command Error Flag	0: No illegal software command or illegal access is detected. 1: An illegal command or illegal access is detected.	R
b5	EILGLERR	Extra Area Illegal Command Error Flag	0: No illegal command or illegal access to the extra area is detected. 1: An illegal command or illegal access to the extra area is detected.	R
b7-b6	-	Reserved	0 or 1.	
b15-b8	-	Reserved	These bits are read as 0.	R

This status register confirms the execution result of a software command. Each error flag is set to 0 when the next software command is executed.

ERERR Flag 0 (Erase Error Flag 0)

The value of the ERERR Flag 0 is undefined when the FCR.STOP bit is set to 1 (processing is forcibly stopped) during erasure.

PRGERR Flag 0 (Program Error Flag 0)

The PRGERR Flag 0 is set when the program command of the FCR register or any command of the FEXCR register are abnormally terminated.

PRGERR Flag 01 (Program Error Flag 00)

The PRGERR Flag 01 is set when any command of the FEXCR register are abnormally terminated.

ILGLERR Flag (Illegal Command Error Flag)

The ILGLERR flag indicates the execution of the software command of the FCR register with an unexpected condition.

[Setting condition]

- Programming/erasure/read commands are executed to an area protected by the access window range.
- The chip erase command is executed when the access window is set (the start block address of the access window is not equal to the end one)
- The blank check, the block erase, consecutive read and the chip erase commands are executed when the start address set to the FSARH and FSARL registers is larger than the end address set to the FEARH and FEARL registers.
- The program, the block erase, the chip erase and the blank check commands are executed when the FASR.EXS bit is 1.
- The data flash address is set to the FSARH and FSARL registers and a software command is executed in the code flash P/E mode.
- The code flash address is set to the FSARH and FSARL registers and a software command is executed in the data flash P/E mode.
- The code flash and the data flash are set to P/E mode simultaneously and a software command is executed.

[Clearing conditions]

- The next software command is executed.

EILGLERR Flag (Extra Area Illegal Command Error Flag)

The EILGLERR flag indicates the execution of the software command of the FEXCR register with the unexpected condition.

[Setting condition]

- The software commands of the FEXCR register is executed when the EXS bit of the FASR register is 0.
- The access window information program command is executed when the FSPR bit is 0.

[Clearing conditions]

- The next software command is executed.

[Products except RA2A1]

1.2.24 Flash Status Register 01 (FSTATR01)

Address(es) 407E C13Ch

	b15	b14	b13	b12	b11	b10	b9	b8
	0	0	0	0	0	0	0	0
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
	0	0	0	0	BCERR1	-	PRGERR1	ERERR1
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ERERR1	Erase Error Flag 1	0: Erasure terminates normally. 1: An error occurred during erasure.	R
b1	PRGERR1	Program Error Flag 1	0: Programming terminates normally. 1: An error occurred during programming.	R
b2	-	Reserved	This bit is read as 0.	R
b3	BCERR1	Blank Check Error Flag 1	0: Blank checking terminates normally. 1: An error occurred during blank checking.	R
b7-b4	-	Reserved	These bits are read as 0.	R

This status register confirms the execution result of a software command. Each error flag is set to 0 when the next software command is executed. The FSTATR01 register is dedicated for the RA4M1 and RA4W1 products.

ERERR Flag 1 (Erase Error Flag 1)

This bit indicates the result of the erase processing for bit 63 to bit 32 of the code flash. The value of this flag is undefined when the FCR.STOP bit is set to 1 (processing is forcibly stopped) during erasure.

PRGERR Flag 1 (Program Error Flag 1)

This bit indicates the result of the program processing for bit 63 to bit 32 of the the code flash.

BCERR Flag 1 (Blank Check Error Flag 1)

This bit indicates the result of the blank check processing for bit 63 to bit 32 of the code flash.

1.2.25 Flash Status Register 02 (FSTATR2)

Address(es) 407E C1F0h

	b15	b14	b13	b12	b11	b10	b9	b8
	0	0	0	0	0	0	0	0
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
	0	0	EILGLERR	ILGLERR	BCERR	PRGERR01	PRGERR	ERERR
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ERERR	Erase Error Flag	The ERERR bit is logical add of the ERERR0 bit of the FSTATR00 register and the ERERR1 bit of the FSTATR01 register.	R
b1	PRGERR	Program Error Flag	The PRGERR bit is logical add of the PRGERR0 bit of the FSTATR00 register and the PRGERR1 bit of the FSTATR01 register.	R
b2	PRGERR01	Program Error Flag 01	This bit is same as the PRGERR01 bit of the FSTATR00 register.	R
b3	BCERR	Blank Check Error Flag	The BEERR bit is logical add of the BCERR0 bit of the FSTATR00 register and the BCERR1 bit of the FSTATR01 register.	R
b4	ILGLERR	Illegal Command Error Flag	This bit is same as the ILGLERR bit of the FSTATR00 register.	R
b5	EILGLERR	Extra Area Illegal Command Error Flag	This bit is same as the EILGLERR bit of the FSTATR00 register.	R
b15-6	-	Reserved	These bits are read as 0	R

1.2.26 Flash Status Register1 (FSTATR1)

Address(es) 407E C12Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	EXRDY	FRDY	0	0	0	1	DRRDY	0
Value after reset	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	-	Reserved	This bit is read as 0.	R
b1	DRRDY	Data Read Ready Flag	0: Other than below 1: The read processing of the consecutive read command at each address is terminated and read data is stored to the FRBH and FRBL registers.	R
b2	-	Reserved	This bit is read as 1.	R
b5－b3	-	Reserved	These bits are read as 0.	R
b6	FRDY	Flash Ready Flag	0: Other than below 1: The software command of the FCR register is terminated.	R
b7	EXRDY	Extra Area Ready Flag	0: Other than below 1: The software command of the FEXCR register is terminated.	R

This status register confirms the execution result of a software command. Each flag is set to 0 when the next software command is executed.

1.2.27 Flash Error Address Monitor Register H (FEAMH)

Address(es) 407E C1E8h

	b15	b14	b13	b12	b11	b10	b9	b8
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset	0	0	0	0	0	0	0	0

1.2.28 Flash Error Address Monitor Register L (FEAML)

Address(es) 407E C1E0h

	b15	b14	b13	b12	b11	b10	b9	b8
Value after reset	0	0	0	0	0	0	0	0

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset	0	0	0	0	0	0	0	0

The error address is withdrawn from the FEAML and the FEAMH register after the software commands execution.

Refer to Figure 1 and Figure 2 for details on the addresses of the flash memory.

1.2.29 Flash Start-Up Setting Monitor Register (FSCMR)

Address(es) 407E C1C0h

	b15	b14	b13	b12	b11	b10	b9	b8
	-	FSPR	-	-	-	-	-	SASMF
Value after reset	0	x*1	x*1	x*1	0	x*1	x*1	x*1

	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0

Note 1: The reset value depends on the state of the extra area.

Bit	Symbol	Bit Name	Description	R/W
b7-b0	—	Reserved	These bits are read as 0.	R
b8	SASMF	Start-Up Area Setting Monitor Flag	0: Setting to start up using the alternative area 1: Setting to start up using the default area	R
b10-b9	—	Reserved	These bits are read as 1 or 0. Writing to these bits has no effect.	R
b11	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R
b13-b12	—	Reserved	These bits are read as 1 or 0. Writing to these bits has no effect.	R
b13-b9	—	Reserved	These bits are read as 1. Writing to these bits has no effect.	R
b14	FSPR	Access Window Protection Flag	0: Access window setting disabled. 1: Access window setting enabled.	R
b15	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R

This register monitors the extra area setting. Data of this register is updated at the reset sequence or the execution of the software command of the FEXCR register.

1.2.30 Flash Access Window Start Address Monitor Register (FAWSMR)

Address(es) 407E C1C8h

	b15	b14	b13	b12	b11	b10	b9	b8
	-	-	-	-				
Value after reset	0	0	0	0	The value set by the user*1			

	b7	b6	b5	b4	b3	b2	b1	b0
	FAWS[11:0]							
Value after reset	The value set by the user*1							

Note: 1. The value in the blank product is 1. It is set to the same value set in bit 11 to bit 0 in the FWBH0 register after the access window information program command is executed.

This register confirms the set value of the access window start address used for area protection.

1.2.31 Flash Access Window End Address Monitor Register (FAWEMR)

Address(es) 407E C1D0h

	b15	b14	b13	b12	b11	b10	b9	b8
	-	-	-	-				
Value after reset	0	0	0	0	The value set by the user*1			

	b7	b6	b5	b4	b3	b2	b1	b0
	FAWE[11:0]							
Value after reset	The value set by the user*1							

Note: 1. The value of the blank product is 1. It is set to the same value set in bit 11 to bit 0 in the FWBL0 register after the access window information program command is executed.

This register confirms the set value of the access window end address used for area protection.

[RA2A1]

1.2.32 Flash Wait Cycle Register (FLWAITR)

Address(es) 407E FFC0h

	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	FLWAIT[2:0]		
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2-b0	FLWAIT[2:0] *1	Flash Wait Cycle	Wait cycle of the code flash read occurs for the CPU read access. 3’b000: 0 wait 3’b001: 1 wait 3’b010: Reserved 3’b011: Reserved 3’b100: Reserved 3’b101: Reserved 3’b110: Reserved 3’b111: 7 wait	R/W
b7-b3	—	Reserved	These bits are read as 0. The write value should be 0.	R

Note: 1. Setting other than 3’b000 is permitted in only high-speed mode.

This register sets the wait cycle number of the code flash read for CPU read access.

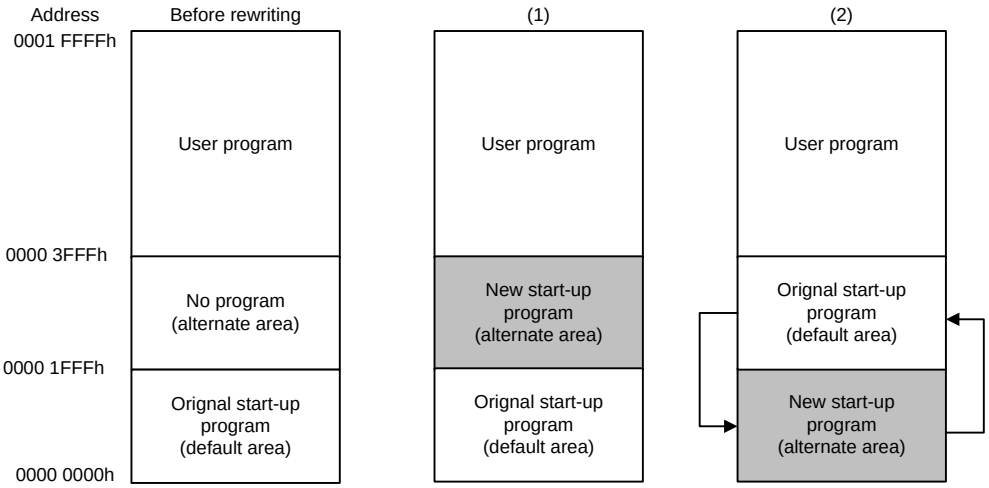
To increase CPU clock frequency, set FLWAITR.FLWAIT before changing the CPU clock frequency. To decrease the CPU clock frequency, set FLWAITR.FLWAIT after changing CPU clock frequency.

1.3 Start-Up Program Protection

When programming of the start-up area is interrupted by a temporary power loss, the start-up program may not be successfully programmed and the user program may not start properly.

This problem can be avoided by programming the start-up program without erasing the existing start-up program using start-up program protection. This function is available in products with a 16 KB or larger code flash.

Figure 5 shows an overview of the start-up program protection. In this figure, the default area indicates the 8-KB region from the start address and the alternate area indicates the next 8-KB region.



(1) Program a new start-up program in the alternate area. If the alternate area fails to be rewritten, the new start-up program can be rewritten again after starting up using the default area because the original start-up program is in the default area.
(2) After the alternate area is successfully rewritten, the default area and the alternate area are switched using the self-programming library. After that, the program in the alternate area starts after a reset.

Figure 5. Overview of the Start-Up Program Protection

1.4 Area Protection

Area protection enables rewriting only the selected blocks (access window) in the user area and disables programming the other blocks. The data flash is not protected by the access window.

Select the start block and end block to set the access window. The access window is changeable and valid at the programming mode (the boot mode, the self-programming mode, and the OCD mode).

Figure 6 and Figure 7 show the area protection overview.

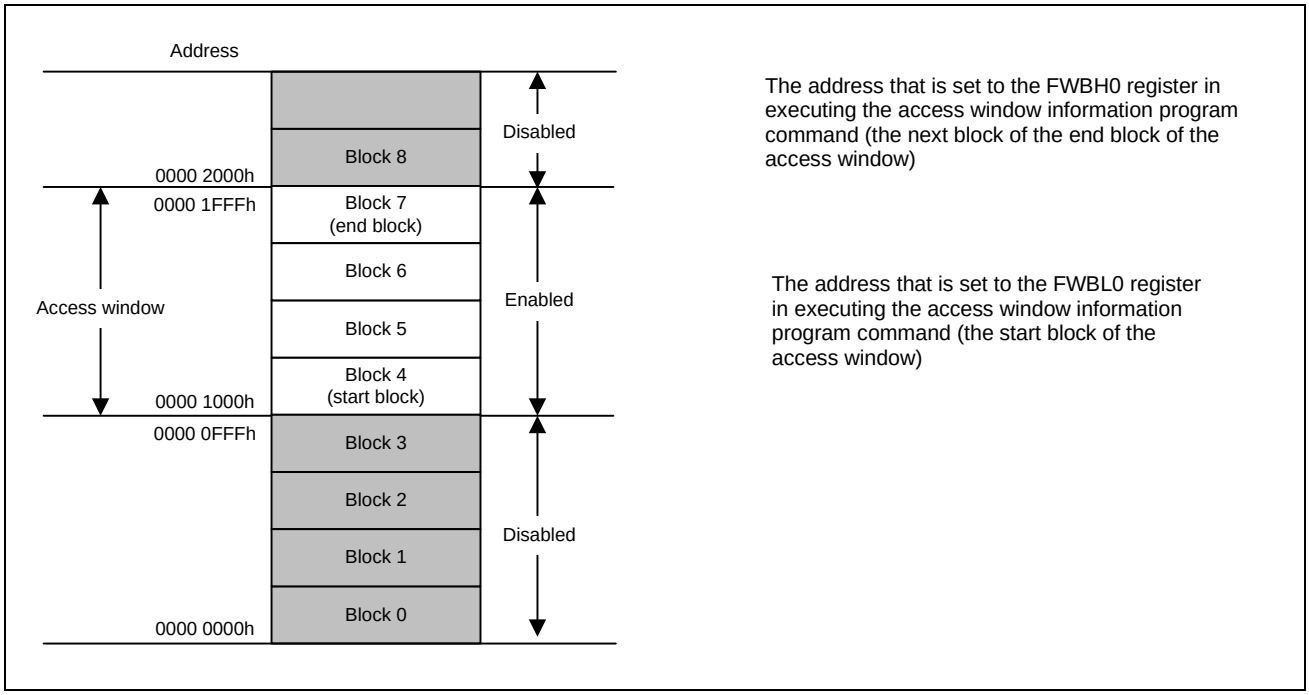


Figure 6. Area Protection Overview [RA2A1]

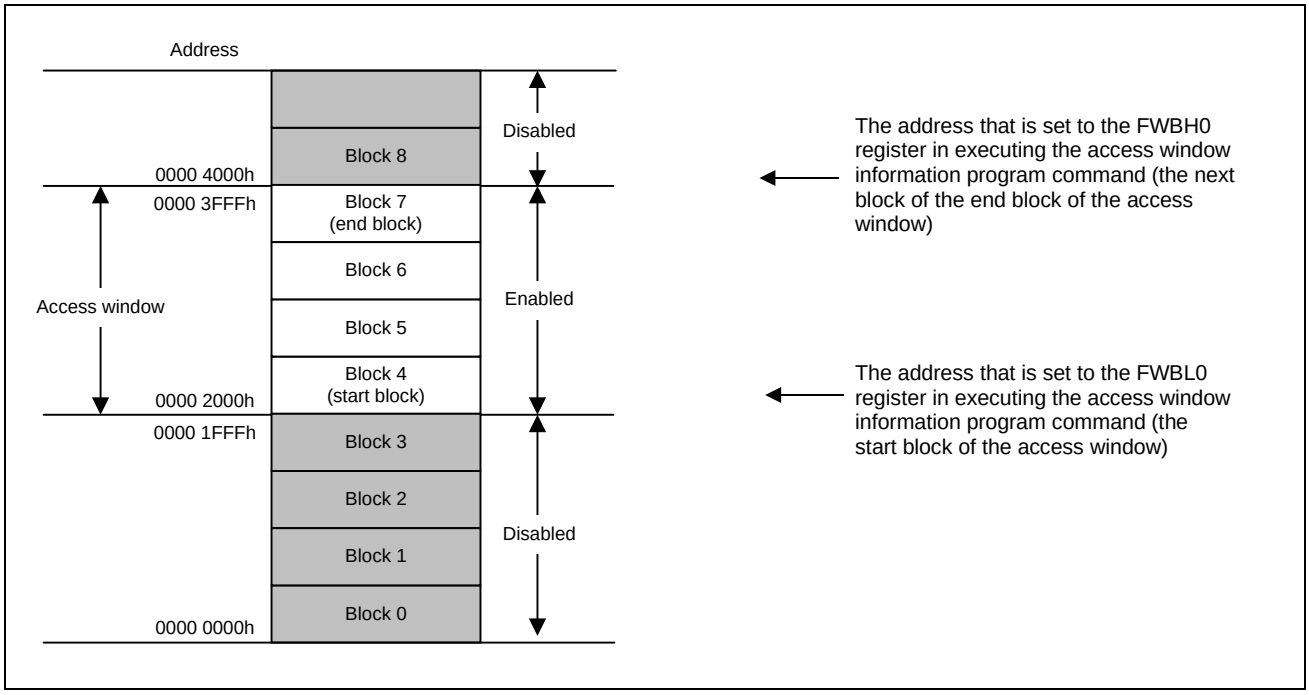


Figure 7. Area Protection Overview [Products except RA2A1]

1.5 Programming and Erasure

The code flash and data flash can be programmed and erased by changing the mode of the dedicated sequencer for programming and erasure, and by issuing commands for programming and erasure.

The mode transitions and commands required to program or erase the code flash and data flash are described below. The descriptions apply in common to boot mode and single-chip mode.

1.5.1 Sequencer Modes

The sequencer has four modes. Transitions between modes are caused by writing to the FENTRYR register, writing to the DFLCTL register, or issuing commands to set the FPMCR register. Figure 8 is a diagram of mode transitions of the flash memory.

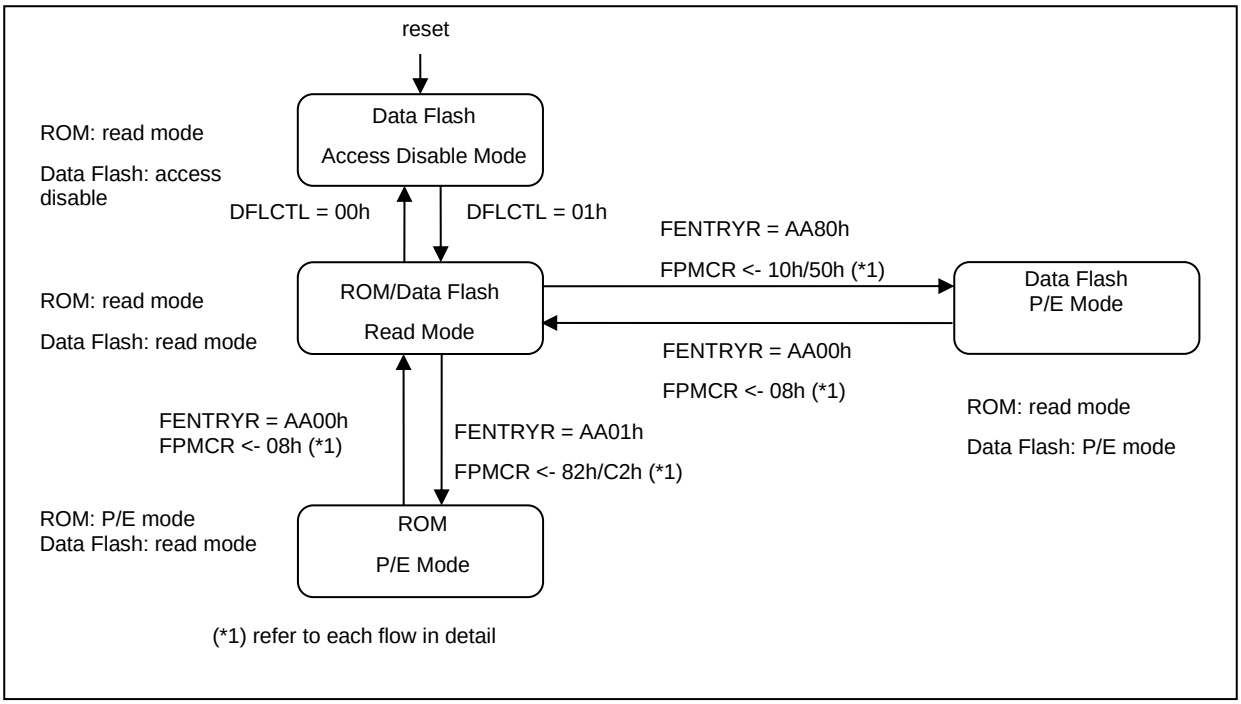


Figure 8. Mode Transitions of the Flash Memory

1.5.1.1 Data Flash Access Disable Mode

Data Flash Access Disable mode is disabled to access to the data flash. Issuing the reset causes this mode. The data flash transits the read mode by setting the DFLCTL.DFLEN bit =1.

1.5.1.2 Read Mode

Read mode is for high-speed reading of the code flash/data flash. Reading from a code flash address for reading can be accomplished in one ICLK clock.

There is one read mode: code flash/data flash read mode.

(1) Code flash/data flash Read Mode

This mode is for reading the code flash and data flash. The sequencer enters this mode when the FENTRYR.FENTRY0 bit is set to 0 with the FENTRYR.FENTRYD bit set to 0.

1.5.1.3 P/E Modes

(1) Code flash P/E Mode

The code flash P/E mode is for programming and erasure of the code flash. The sequencer enters this mode when the FENTRYR.FENTRYD bit is set to 0 with the FENTRYR.FENTRY0 bit set to 1. In this mode, it is impossible to access the data flash.

(2) Data flash P/E Mode

The data flash P/E Mode is for programming and erasure of the data flash. High-speed reading from the code flash is possible. The sequencer enters this mode when the FENTRYR.FENTRY0 bit is set to 0 with the FENTRYR.FENTRYD bit set to 1.

1.5.2 Software Commands

Software commands consist of commands for programming and erasure and commands for programming start-up program area information and access window information. Table 9 lists the software commands for use with the flash memory.

Table 9. Software Commands

Command	Function
Program	Code flash programming (4 bytes) Data flash programming (1 byte)
Block erase	Code flash/data flash erasure
Chip erase	Code flash/data flash erasure
Consecutive read	Read the specified area during code flash P/E mode or data flash P/E mode.
Blank check	Check whether the specified area is blank. Confirm that data is not programmed in the area. This command does not guarantee whether the area remains erased.
Start-up area information and security program	Set the FSPR or the SASMF to the extra area
Access window information program	Set the access window used for area protection to the extra area
OCDID program	Set the OCDID to the extra area

1.5.3 Software Command Usage

The following describes the usage of each software command.

1.5.3.1 Switching from Data Flash Access Disable Mode to Read Mode

It is necessary to enter the code flash/data flash read mode from the data flash access disable mode. Figure 9 shows the procedure for entering to the code flash/data flash read mode from the data flash access disable mode.

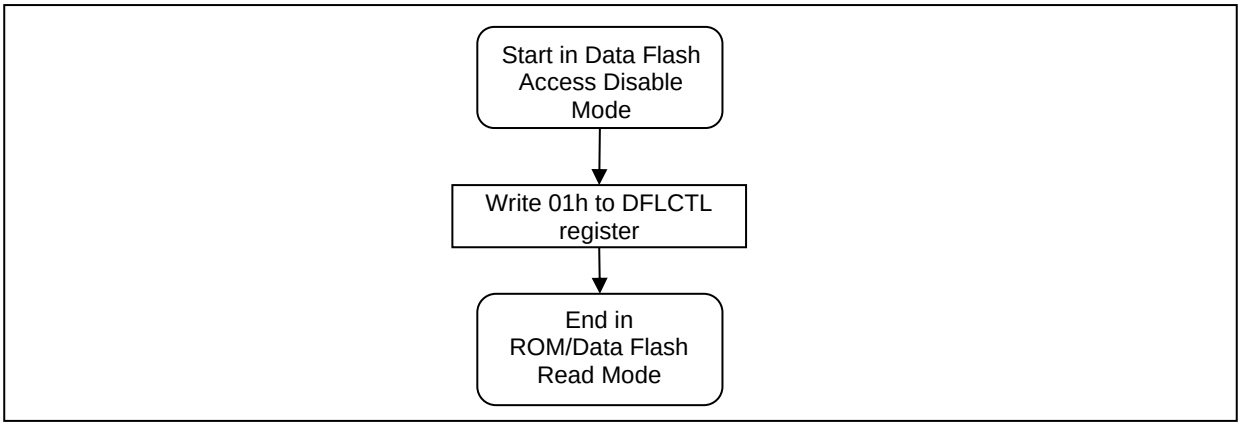


Figure 9. Mode Transitions to Read Mode from Data Flash Access Disable Mode

1.5.3.2 Switching to the code flash P/E Mode

It is necessary to enter the code flash P/E mode by setting the FENTRY0 bit of the FENTRYR register before executing the software command for the code flash. Figure 10 shows the procedure for entering to the code flash P/E Mode.

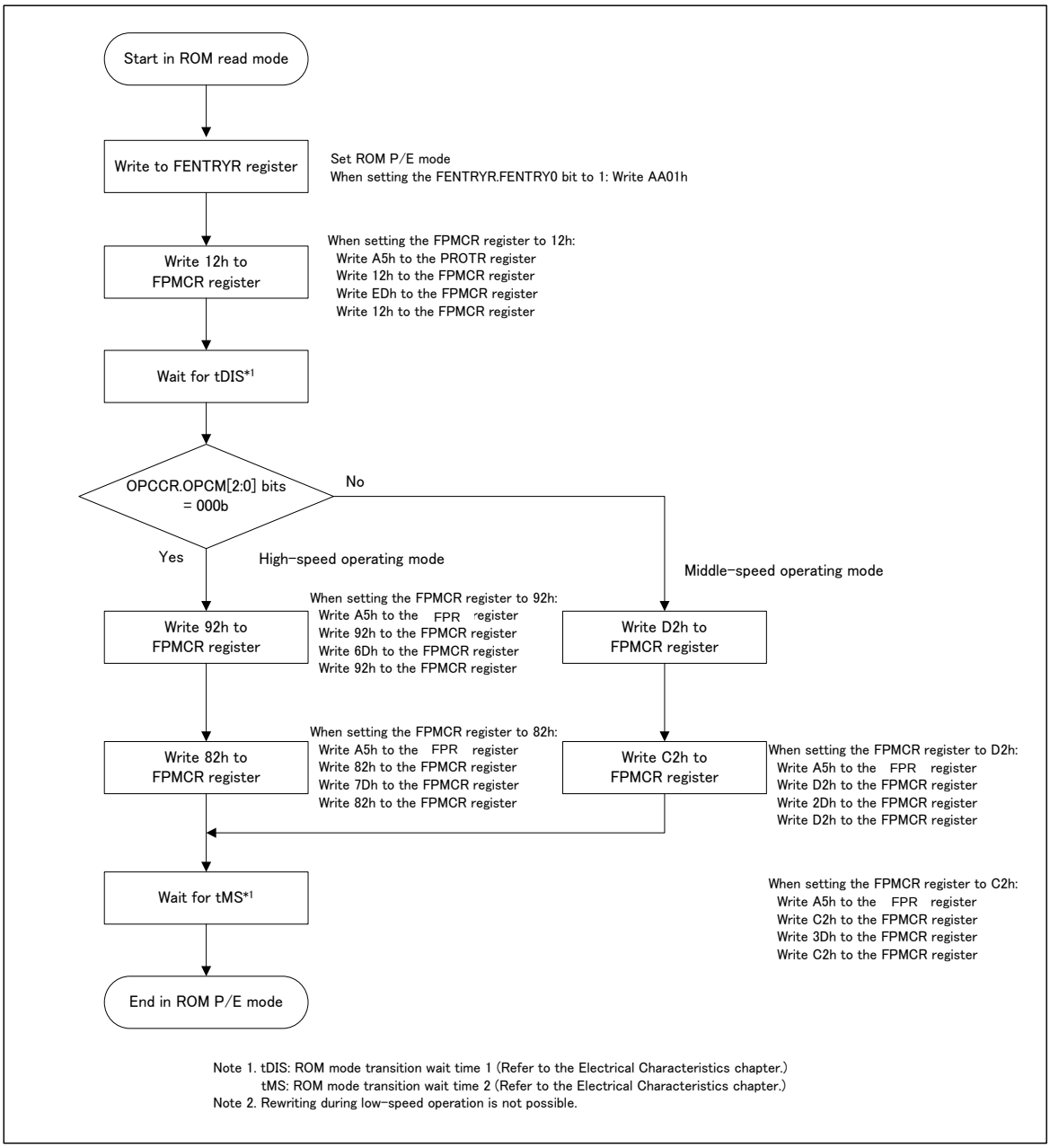


Figure 10. Procedure for Entering the Code flash P/E Mode

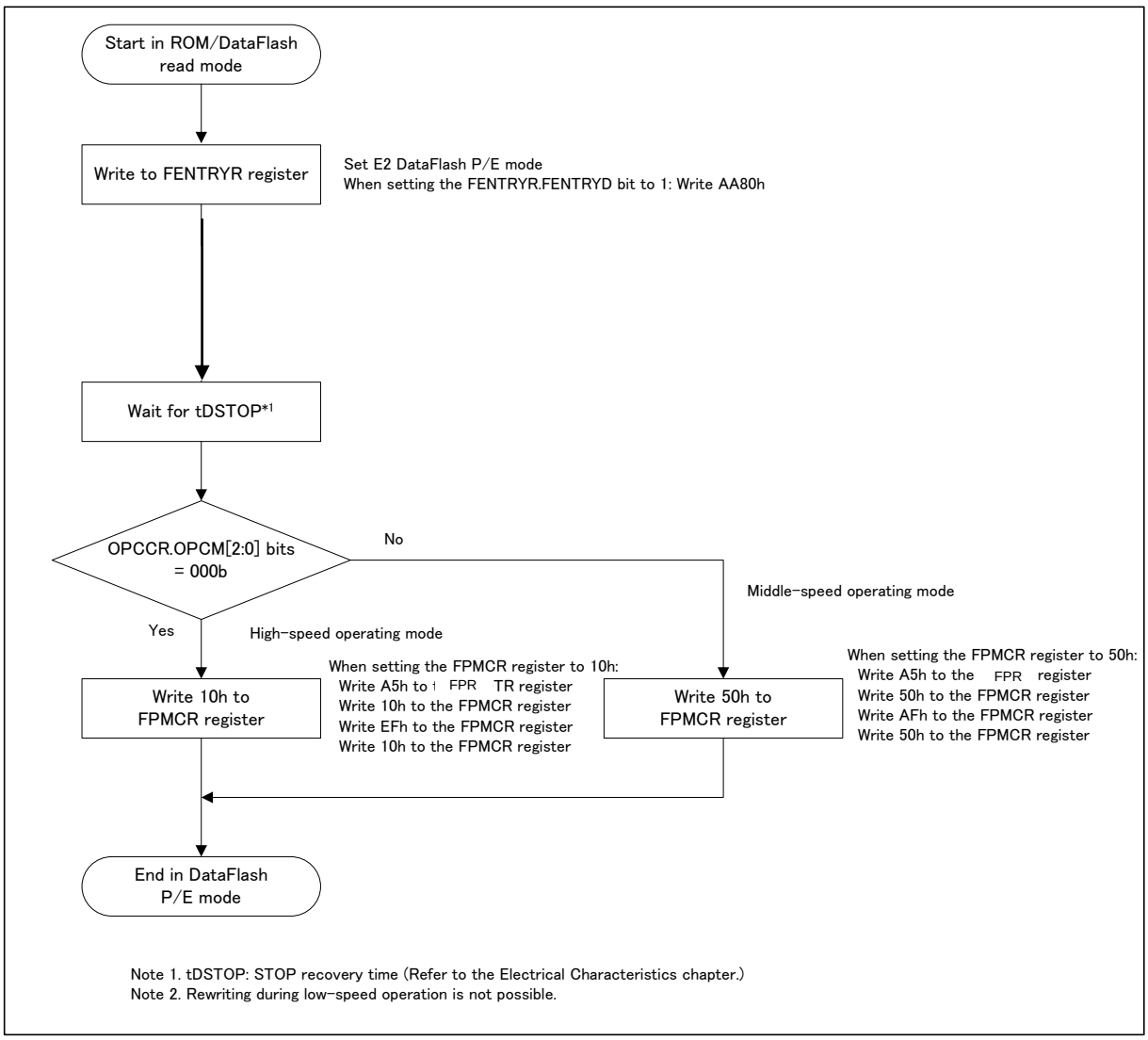


Figure 11. Procedure for Changing from the Read Mode to the Data Flash P/E Mode

(1) Switching the code flash to the read mode

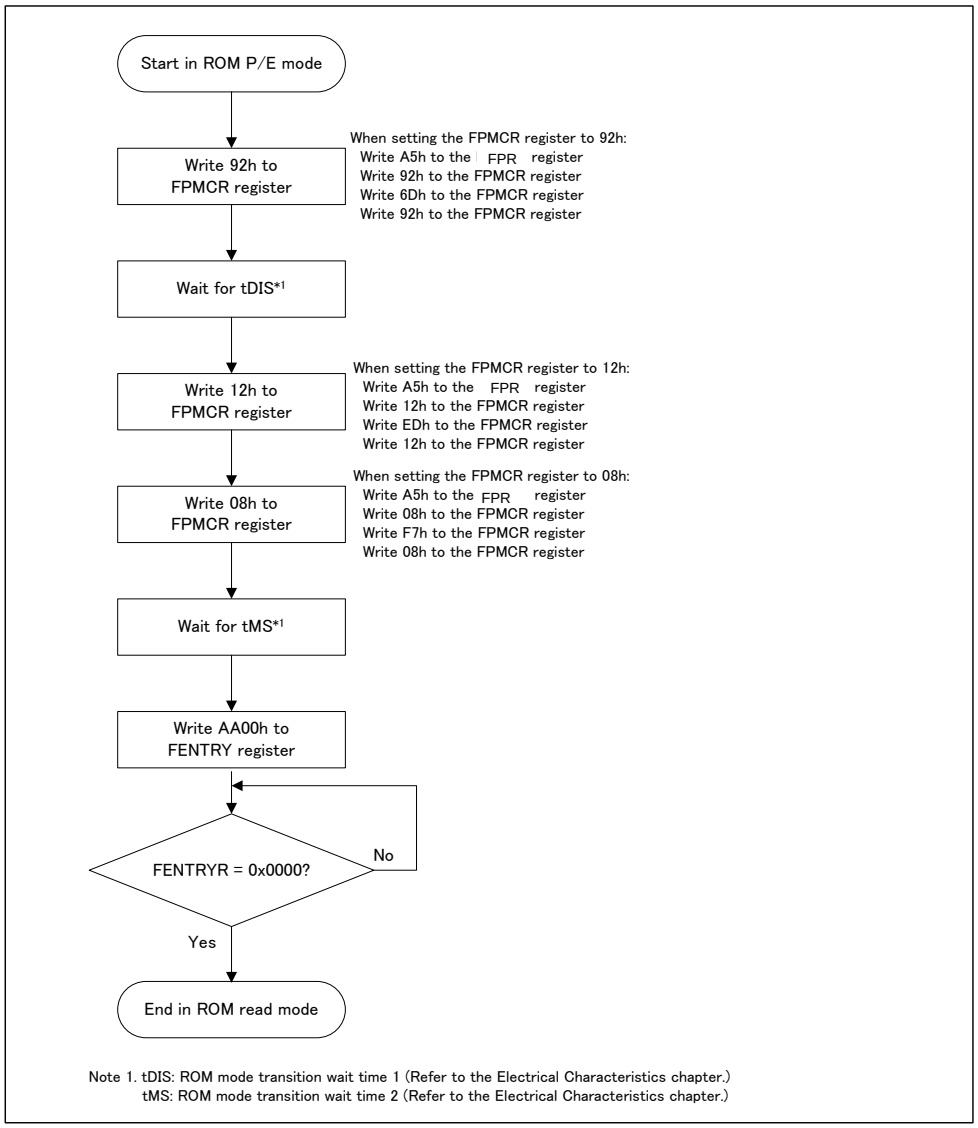


Figure 12. Procedure for Entering the Code Flash Read Mode

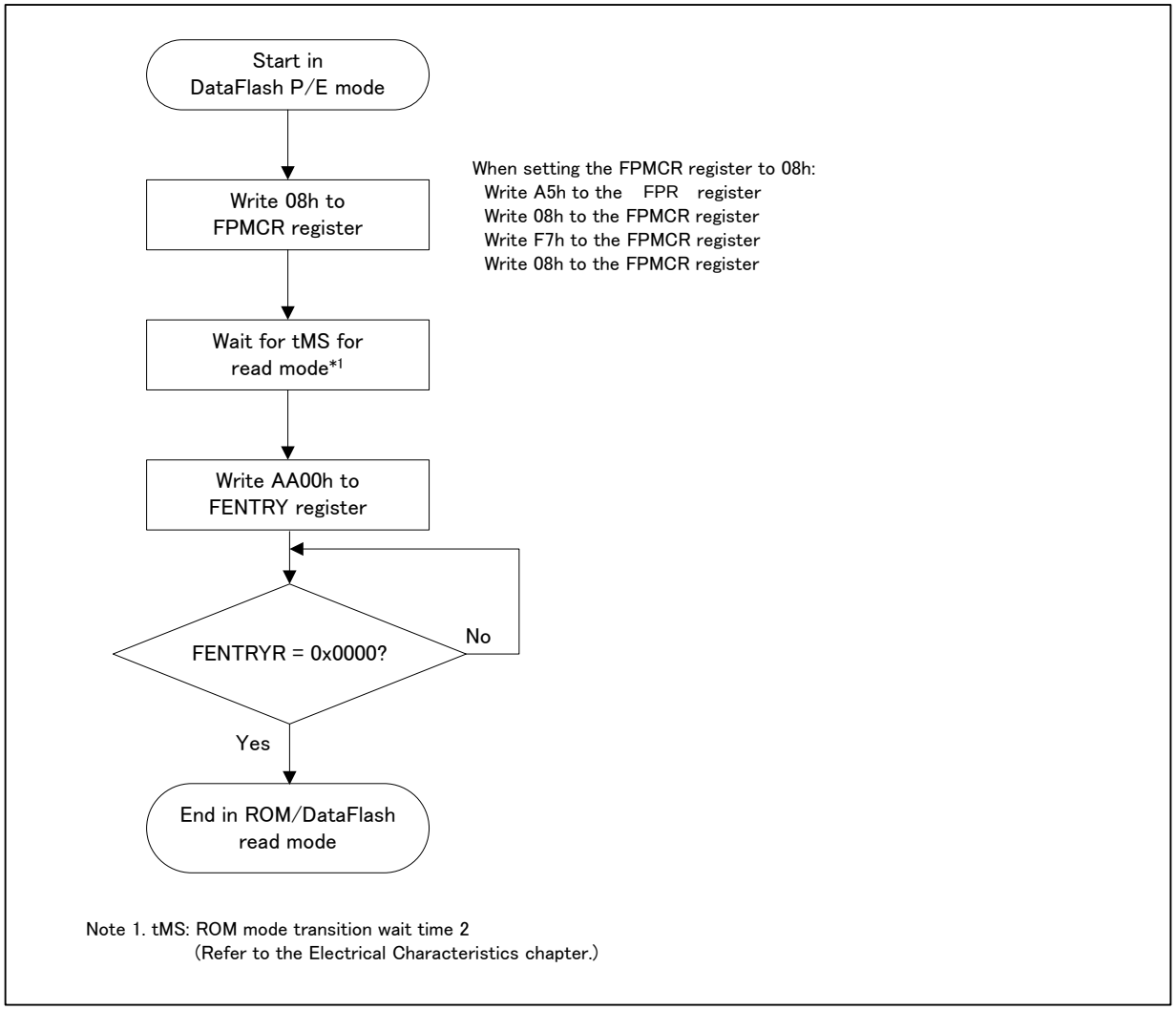


Figure 13. Procedure for Changing from the Data Flash P/E Mode to the Code Flash/Data Flash Read Mode

1.5.3.3 Flowchart for Programming the Code Flash or the Data Flash

Figure 14 describes the flow chart for programming the code flash or the data flash.

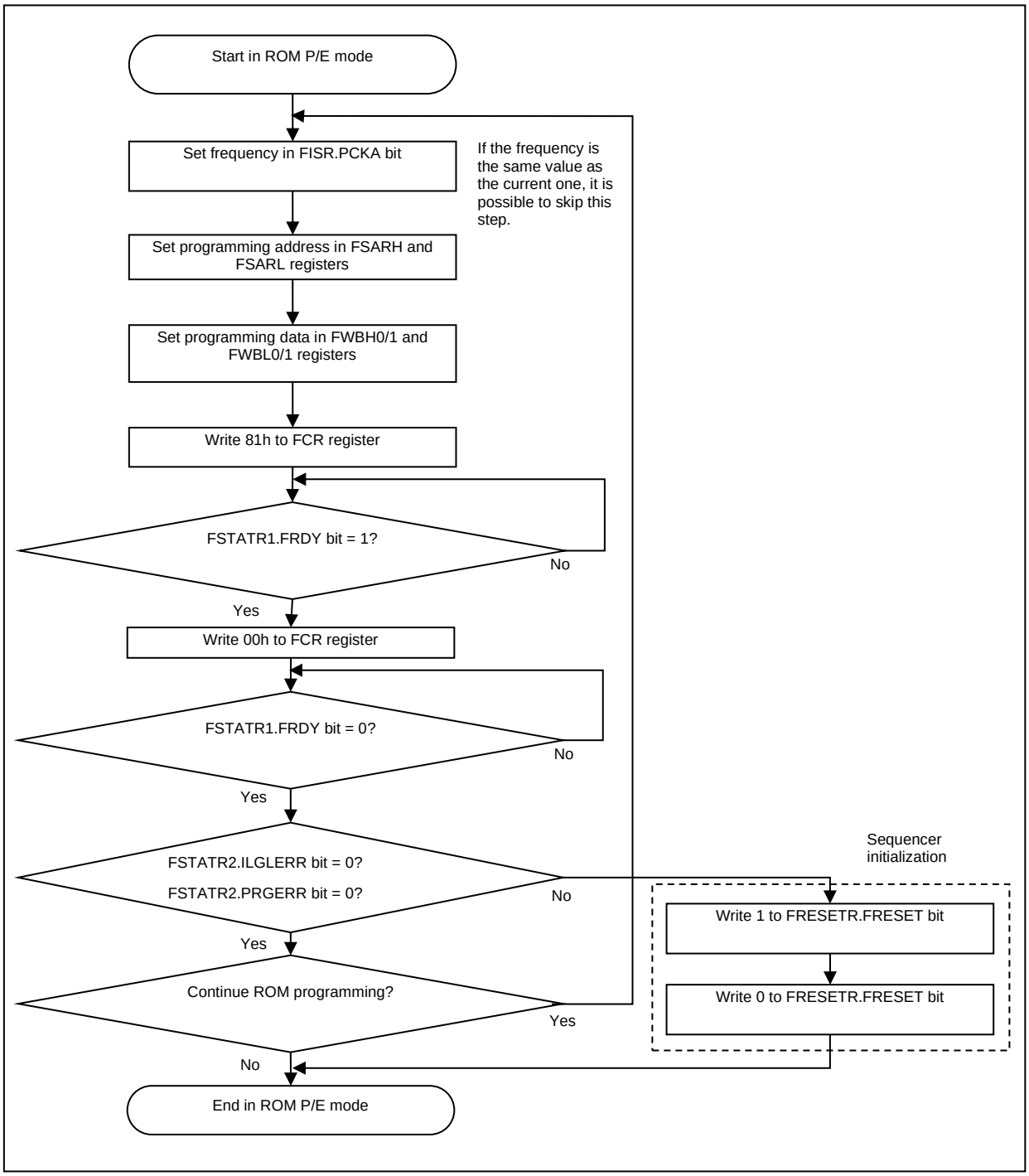


Figure 14. Flowchart for Programming the Code Flash

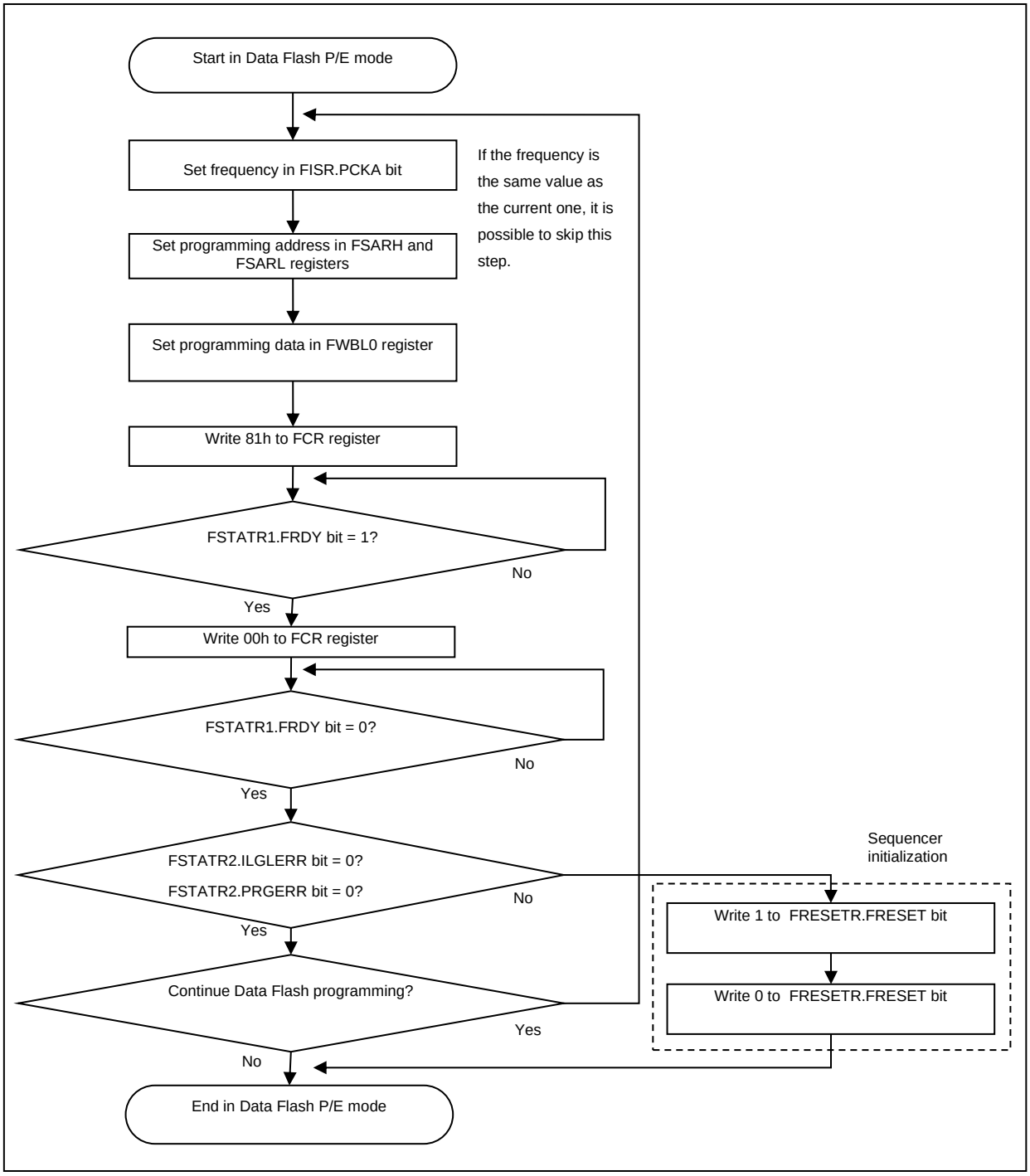


Figure 15. Flowchart for Programming the Data Flash

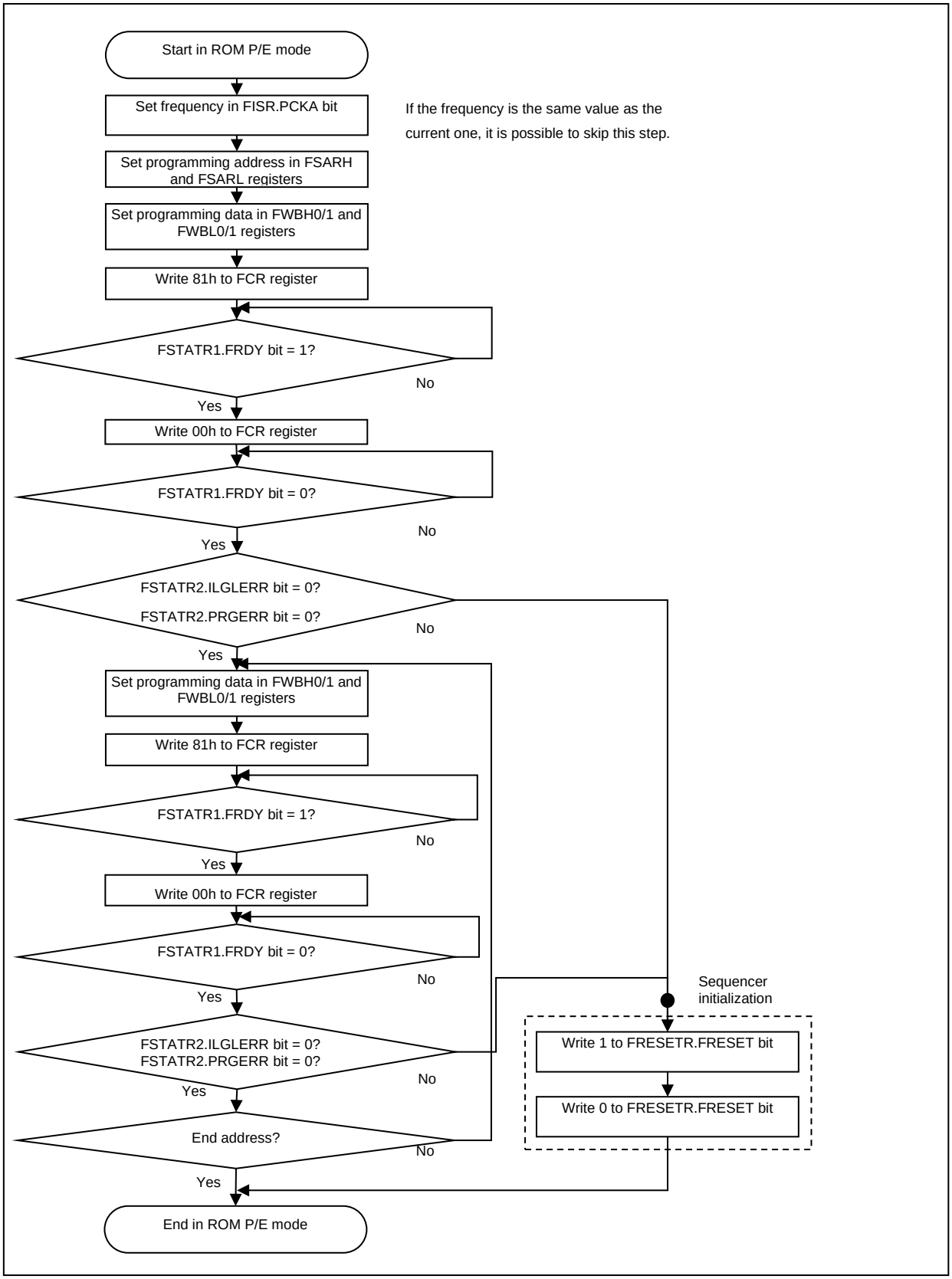


Figure 16. Flowchart for Consecutive Programming of the Code Flash

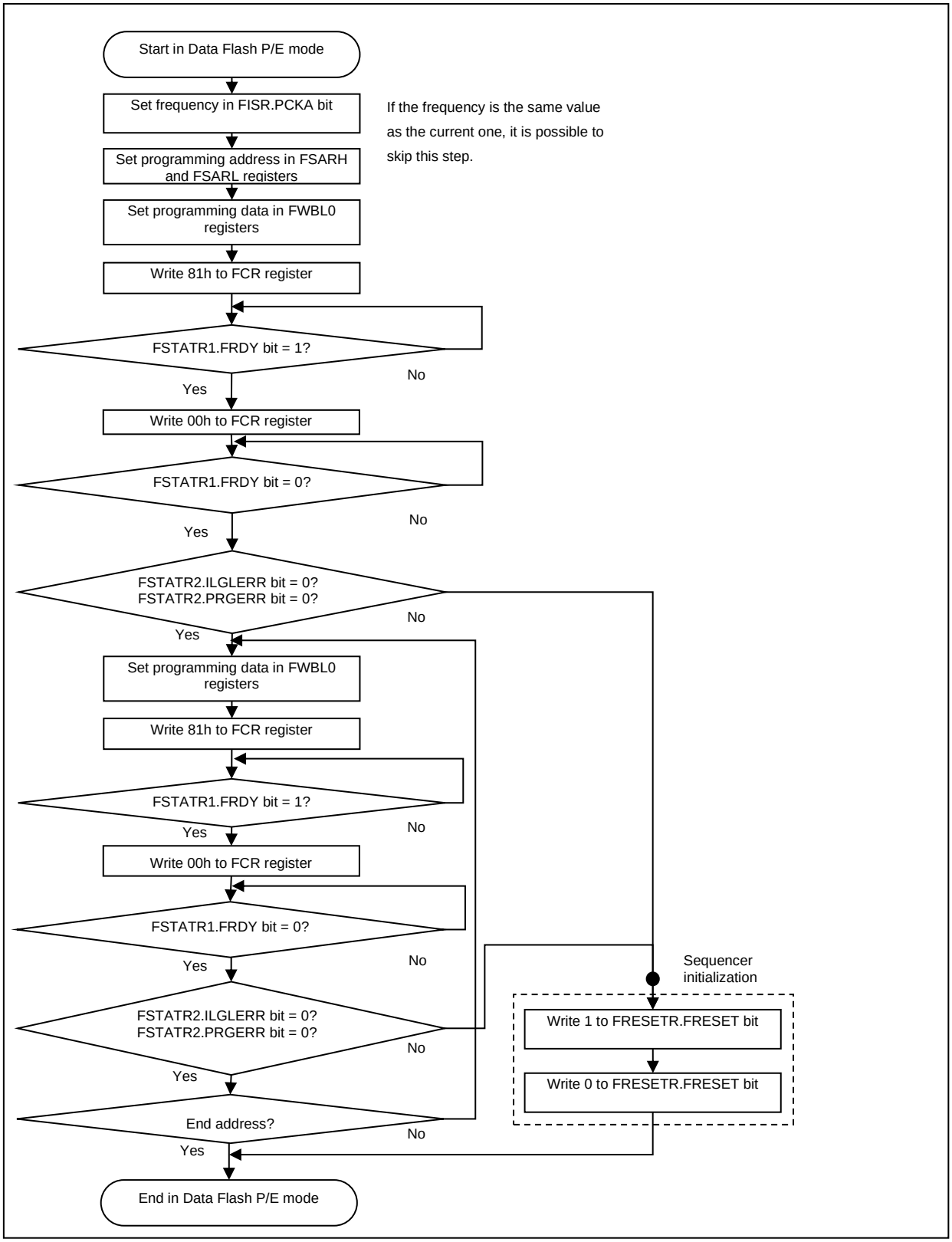


Figure 17. Flowchart for Consecutive Programming of the Data Flash

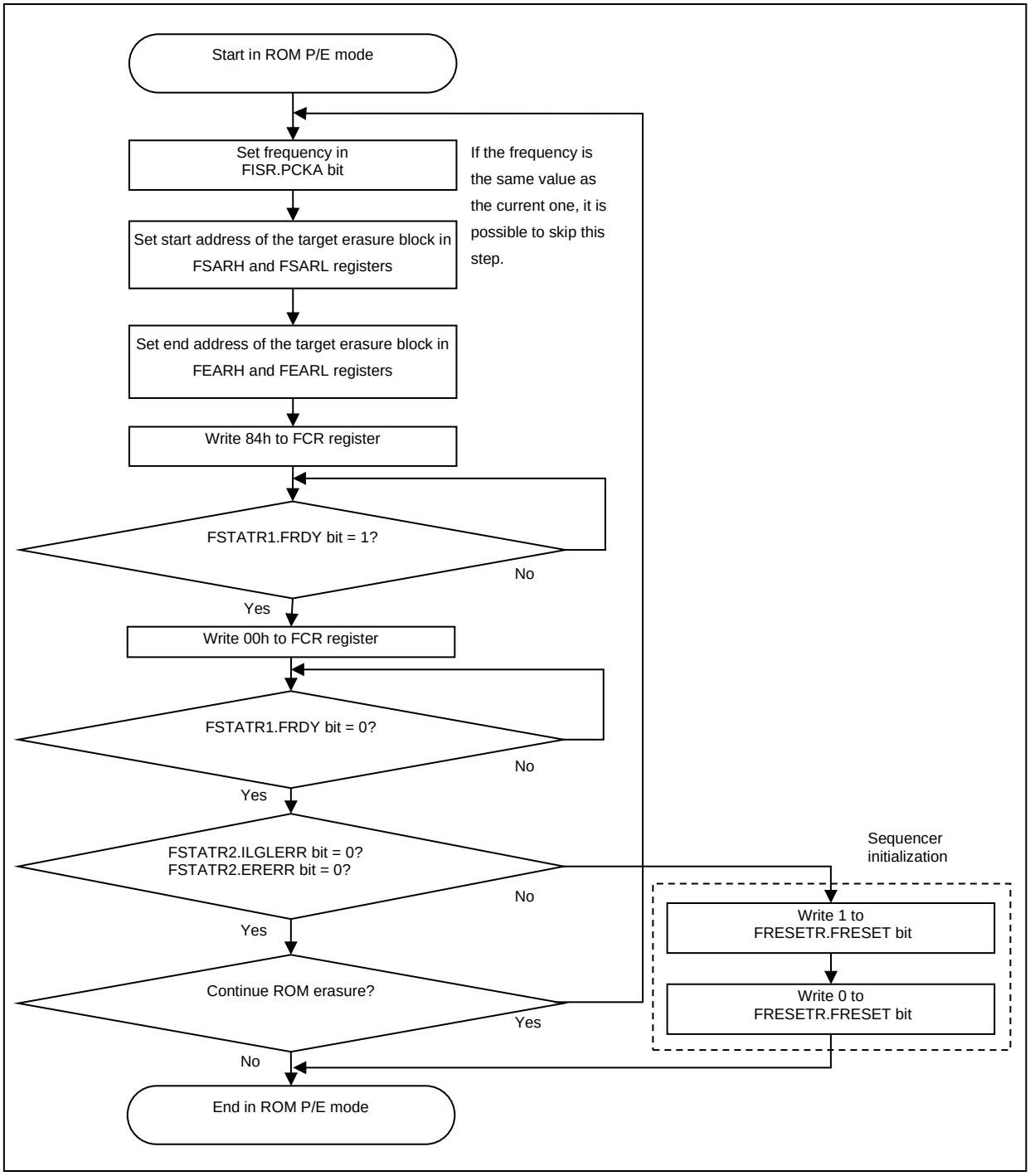


Figure 18. Flowchart for Code Flash Block Erase Procedure

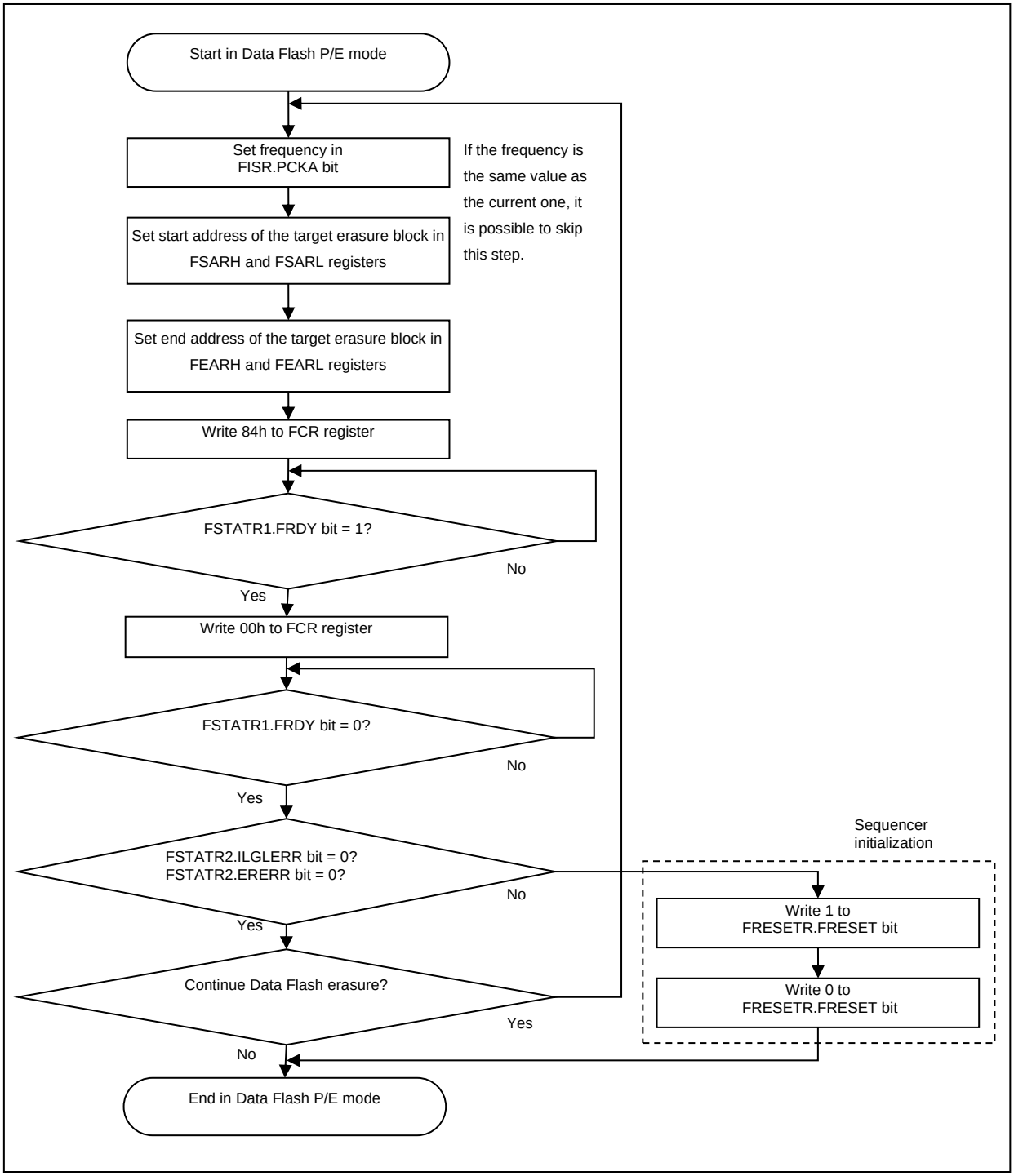


Figure 19. Flowchart for Data Flash Block Erase Procedure

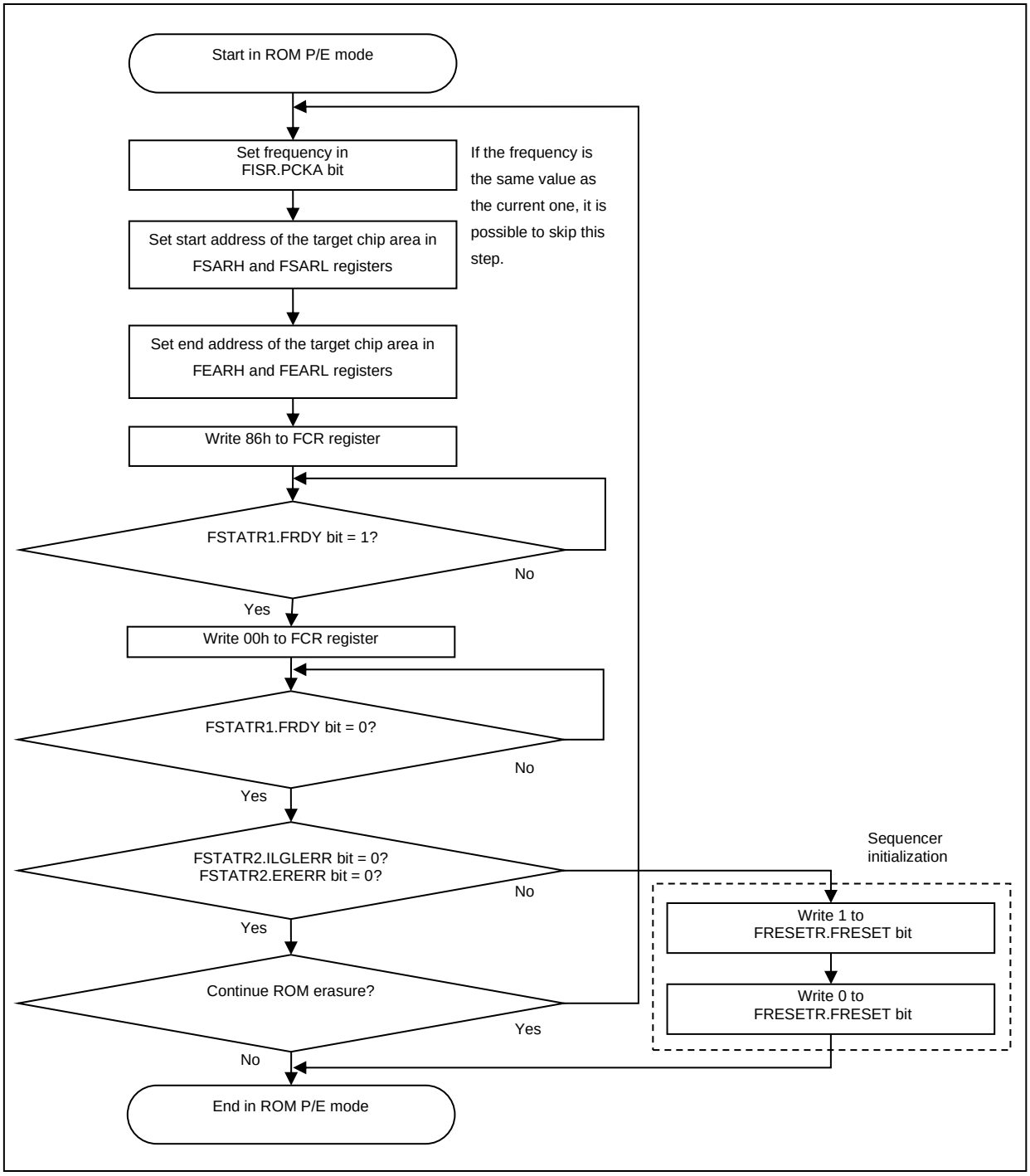


Figure 20. Flowchart for Code Flash Chip Erase Procedure

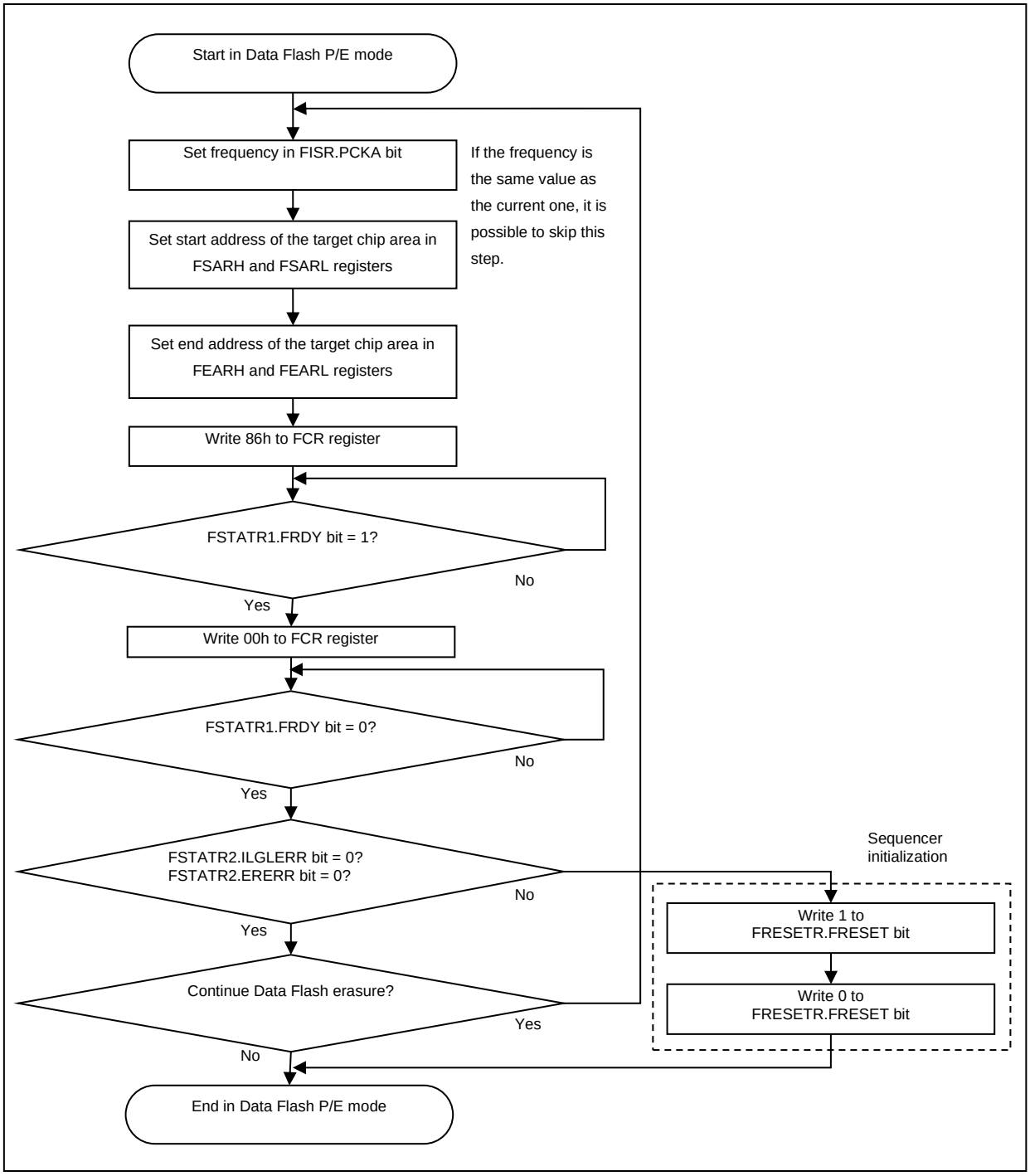


Figure 21. Data Flash Chip Erase Procedure

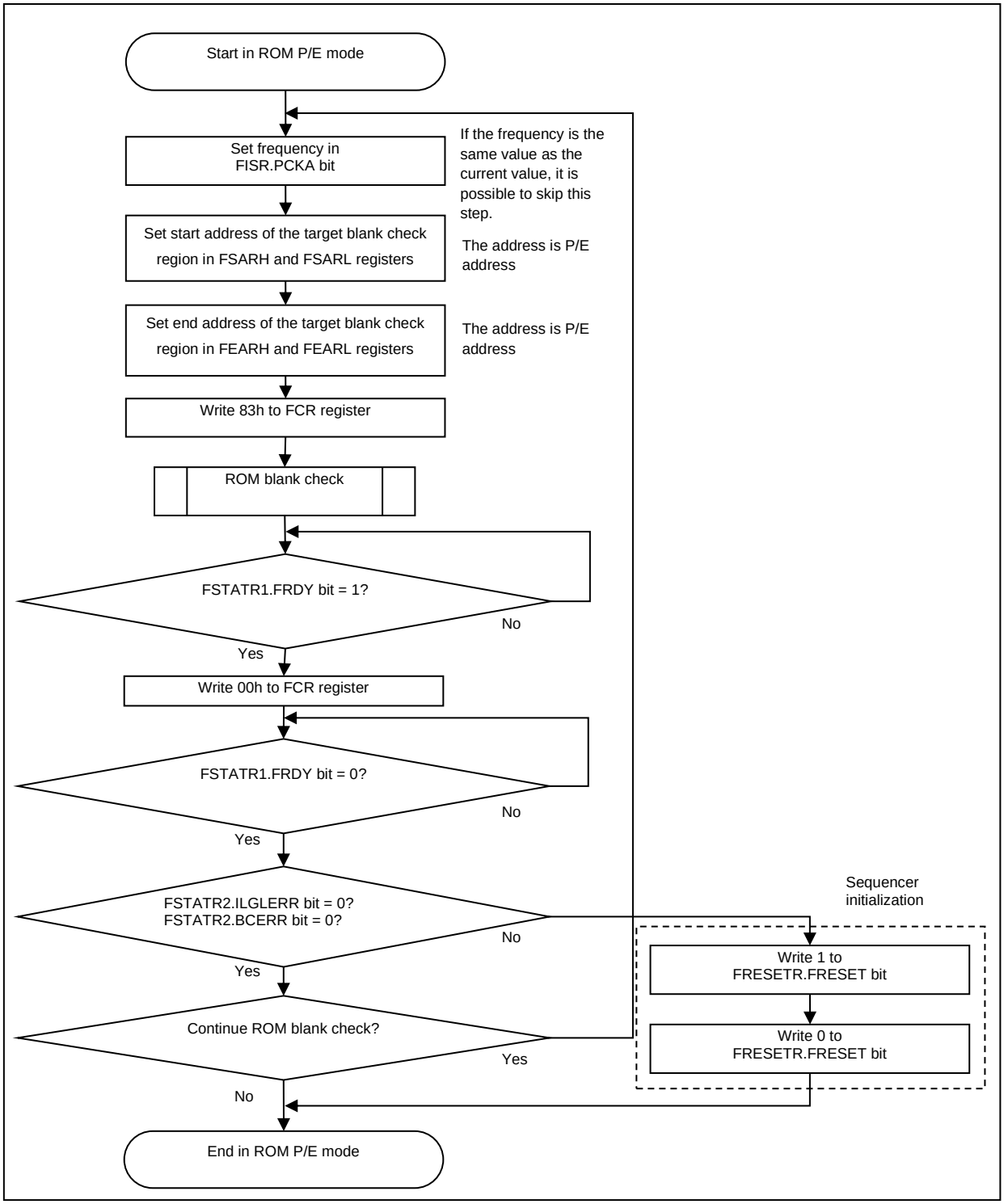


Figure 22. Flowchart for Code Flash Blank Check Procedure

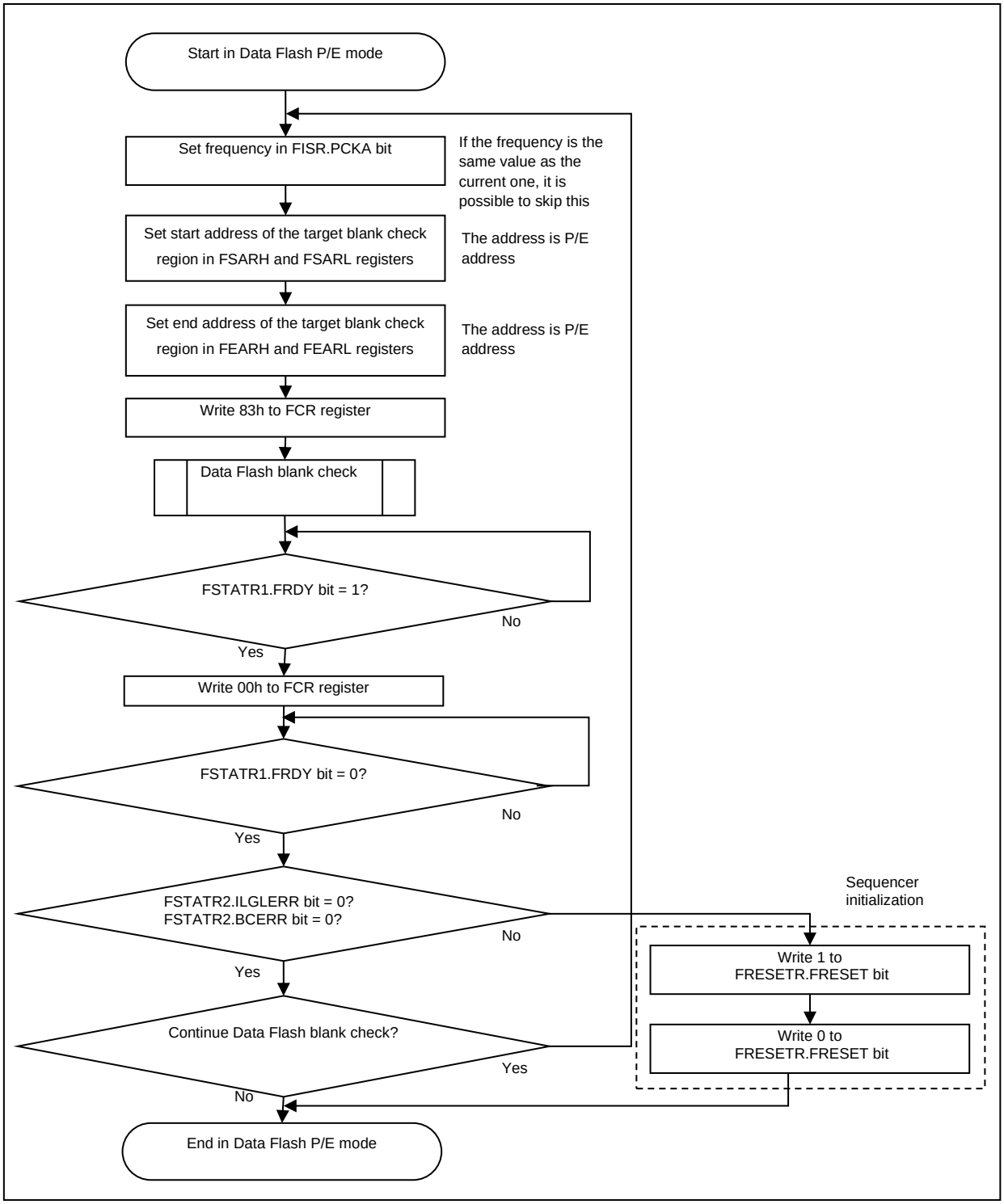


Figure 23. Data Flash Blank Check Procedure

1.5.3.4 Program/Access Window Information Program/OCDID information Program

Figure 24 is a simple flowchart of the procedure for the start-up area information and FSPR program/access window information program/OCDID information program.

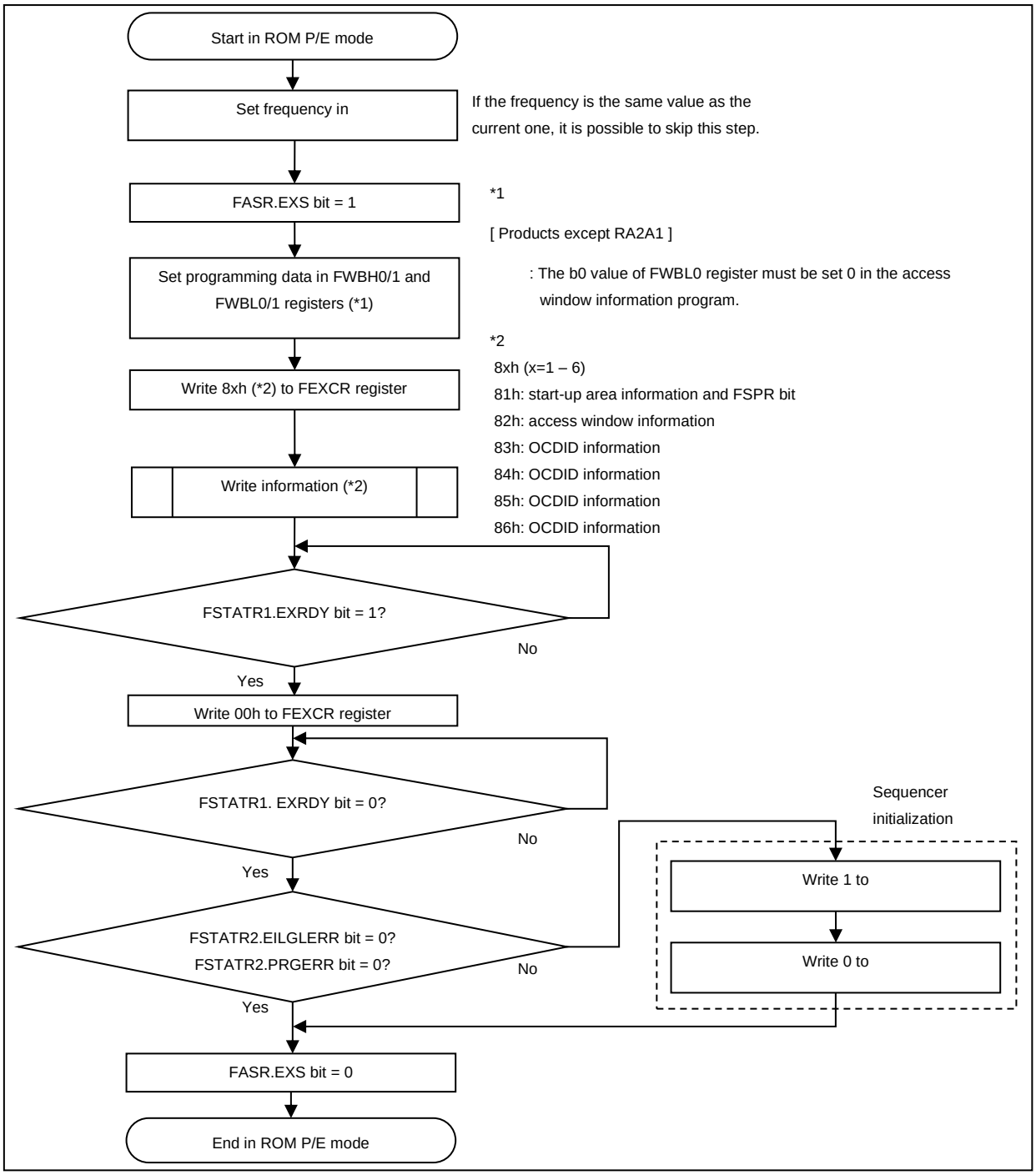


Figure 24. Simple Flowchart of the Procedure for the Start-Up Area Information and FSPR Program/Access Window Information Program/OCDID information Program

Order of the FSPR bit setting by Start-Up Area Information and FSPR Program

Set the FSPR bit after programing of the start-up area information and the access window information. If the FSPR bit is set before programing of the start-up area information and the access window information, the start-up area information and the access window information cannot be programmed because of the security function by the FSPR. When programming using the hex file, programming is in ascending order of the address. In this case, the FSPR bit will be written in before the access window information. Therefore, divide the hex file for FSPR into another file, and use it after the access window information setting.

1.5.3.5 Consecutive Read

Figure 25 is a simple flowchart for the procedure for consecutive read.

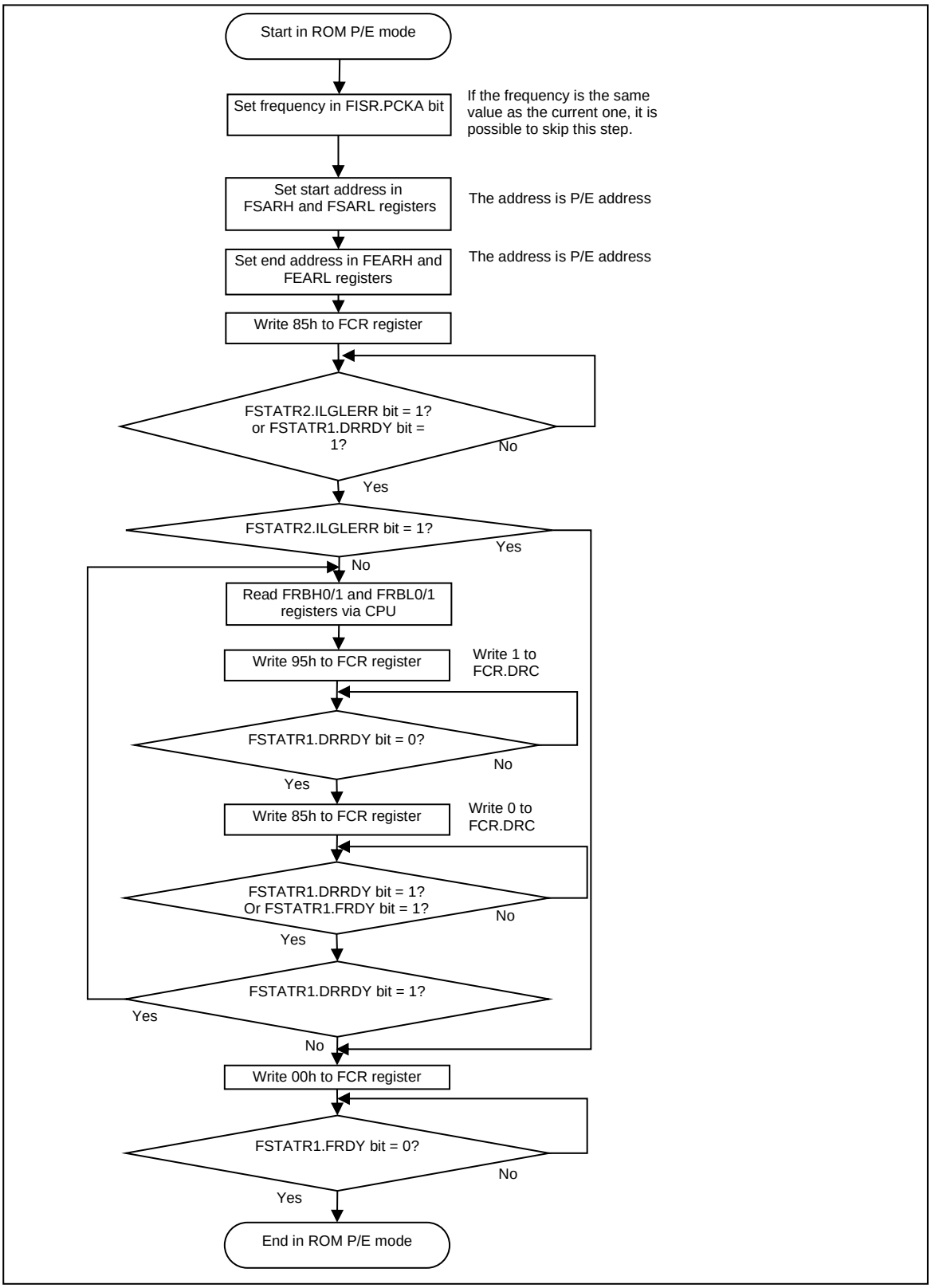


Figure 25. Simple Flowchart of the Procedure for Consecutive Read

1.5.3.6 Forced Stop by Software Command

Figure 26 is a simple flowchart of the procedure for the forced stop in order to stop the blank check command or the block erase command forcibly. When the forced stop is executed, FEAMH/FEAML registers store the stopped address value. In case of the blank check command, the blank check can restart from the stopped address by copying the value of FEAMH/FEAML registers to FSARH/FSARL registers respectively.

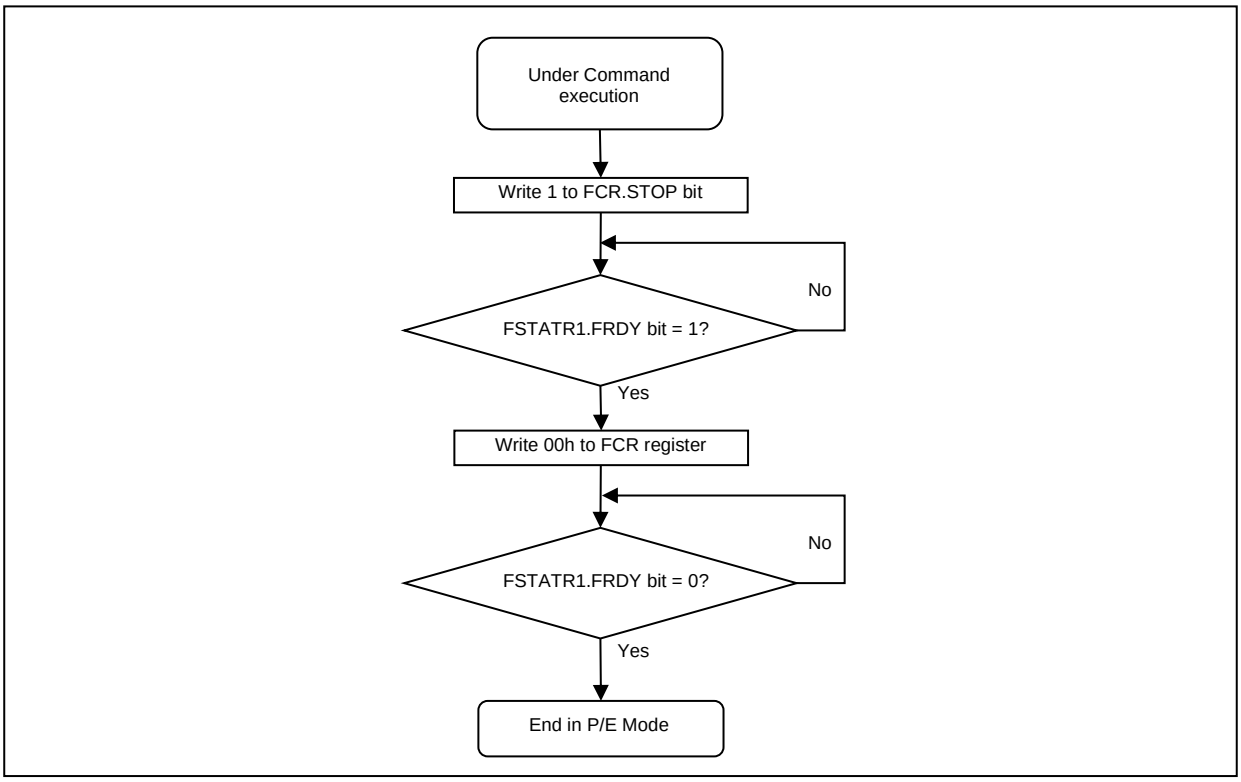


Figure 26. Simple Flowchart of the Procedure for Forced Stop

1.6 Usage Notes

1.6.1 Erase Suspended Area

Data in areas where an erase operation is suspended is undefined. To avoid malfunctions caused by reading undefined data, do not execute commands and read data in the area where an erase operation is suspended.

1.6.2 Suspension by Erase Suspend Commands

When suspending an erase operation by the erase suspend command, complete the operation by a resume command.

1.6.3 Additional Programming Disabled

The same address cannot be programmed more than once. When programming an area that has been already programmed, erase the area first.

1.6.4 Reset during Program/Erase

If inputting a reset from the RES# pin, release the reset after reset input time of at least tRESW (refer to Electrical Characteristics section) within the range of the operating voltage defined in the electrical characteristics.

The IWDT reset and software reset can be used regardless of tRESW.

1.6.5 Non-Maskable Interrupt Disabled during Program/Erase

When a non-maskable interrupt (NMI pin interrupt, oscillation stop detection interrupt, IWDT underflow/refresh error, voltage monitoring 1 interrupt, or voltage monitoring 2 interrupt) occurs during a program/erase operation, the vectors are fetched from the code flash, and undefined data is read. Therefore, do not generate a non-maskable interrupt during a program/erase operation on the code flash.

(The description in section 1.6.5 applies only to the code flash.)

1.6.6 Location of Interrupt Vectors during a Program/Erase Operation

When an interrupt occurs during a program/erase operation, the vector may be fetched from the code flash. To avoid fetching the vector from the code flash, set the destination for fetching interrupt vectors to an area other than the code flash with the interrupt table.

1.6.7 Program/Erase in Low-Speed Operating Mode

Do not program or erase the flash memory when low-speed operating mode is selected by the SOPCCR register for low-power consumption functions.

1.6.8 Abnormal Termination during Program/Erase

When the voltage exceeds the range of the operating voltage during a program/erase operation or when a program/erase operation is not completed successfully due to a reset or prohibited actions described in (9), erase the area again.

1.6.9 Actions Prohibited during Program/Erase

To prevent the damage to the flash memory, comply with the following instructions.

- Do not use an MCU power supply that is outside the operating voltage range.
- Do not update the value of the OPCCR.OPCM[1:0] bits.
- Do not update the value of the SOPCCR.SOPCM bit.
- Do not change the division ratio of the flash interface clock (FCLK [Products except RA2A1], ICLK [RA2A1]).
- Do not place the MCU in software standby mode.
- Do not access the data flash during a program/erase operation to the code flash.
- Do not change the DFLCTL.DFLEN bit value during a program/erase operation to the data flash.

1.6.10 FlashIF clock (FCLK [Products except RA2A1], ICLK [RA2A1]) during Program/Erase

For programming/erasure by self-programming, it is necessary to set the FlashIF clock and specify an integer frequency in the flash initial setting register (FISR). Note that when the frequency (FCLK [Products except RA2A1], ICLK [RA2A1]) is 4 to 32 MHz, a rounded-up value should be set for a non-integer frequency such as 12.5 MHz (that is, 12.5 MHz should be set rounded up to 13 MHz).

2. RV40F-Type Flash Memory Phase 2 (RA6M1, RA6M2, RA6M3, RA6T1)

2.1 Features

The features of the flash memory are described in the MCU user's manual. See the user's manual for information on the capacity, block configuration, and addresses of the flash memory in a given product.

Programming/Erasure

A dedicated sequencer for the flash memory (flash sequencer) executes programming and erasure via the peripheral bus. The flash sequencer also supports the suspension and resumption of processing, and background operations (BGO).

Security Functions

The flash memory incorporates hardware functions to prevent illicit tampering.

Safety Functions

The flash memory incorporates hardware functions to prevent erroneous writing.

Interrupts

The flash memory supports an interrupt to indicate completion of processing by the flash sequencer and an error interrupt to indicate operations that were in error.

Table 10. FPSYS Specification

Item		Specification
Flash Memory (Memory size configuration of each products depend on the product's specification.)	Code Flash	FLP double-side without ECC Up to 2M Bytes FLI double-side without ECC None / Up to 2M Bytes
	Data Flash	EEP without ECC None / Up to 64K Bytes
Supported Chip Operation Mode		Following chip operation modes are supported. self- programming mode Serial programming mode On chip debugger mode
Flash Sequencer Command	Code Flash	Program : 128 Bytes Erase1 : 1 block (8K Bytes or 32K Bytes) P/E suspend P/E resume Forced stop Status clear Config Program (16 Bytes)
	Data Flash	Program : 4/8/16 Bytes (within one EEP) Erase1 : 1 block (64 Bytes) Erase2 : 64/128/256 Bytes P/E suspend P/E resume Forced stop Blank check : 4~64K Bytes (within one EEP) Status clear
Dual Operation		BGO (Back Ground Operation) FLI read with EEP program/erase is possible. Overlay FLI read with other FLI program/erase is possible. Reverse BGO EEP read with FLI program/erase is possible.
Security Function		Serial programming mode protection ID authentication OCD mode protection ID authentication
Safety Function		Software protect Flash sequencer command protection by FENTRYR register. Flash memory is protected by FWEPROR register. The user area is protected by the access window in the self-programing mode, the serial programming mode and the OCD mode. The access window is allowed to be locked by the FSPR bit. Error protect Error is detected when unintended commands or prohibit settings occur. Flash sequencer command is not accepted after error detection. Boot area protection The start-up area select function allows the customer to safely update the boot program. The size of the start-up area is 8K bytes. The start-up area locates at the user area, and is allowed to be locked by the FSPR bit.
Reset Transfer		Flash memory internal reset transfer Flash and product trimming Redundancy information FACI reset transfer Security and safety setting Product trimming

Item	Specification
Interrupt Request	Flash sequencer ready (processing end) A positive pulse (1 clkf width) interrupt request. "intflend" pin : Enabled by FRDYIE bit. Flash sequencer error "intflerr" pin : Enabled by CFAEIE/CMDLKIE/DFAEIE bits. High level sensitive interrupt request.
Address conversion	Little-endian is supported

2.2 Module Configuration

Modules related to the flash memory are configured as shown in Figure 27. The flash sequencer is configured of the FCU and FACI. The FCU executes basic control of rewriting of the flash memory. The FACI receives FACI commands via the peripheral bus and controls FCU operations accordingly.

In response to a reset, the FACI transfers data from the flash memory to the option byte storage registers.

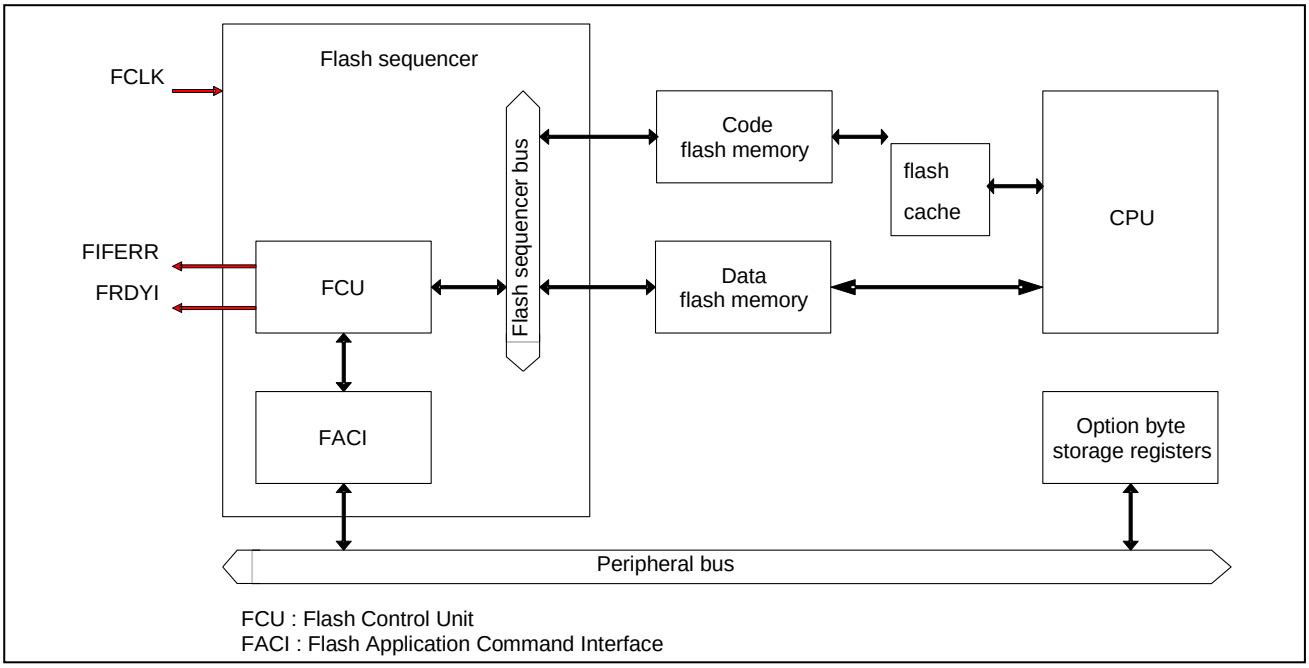


Figure 27. Configuration of Flash Memory Related Modules

2.3 Address Space

Using the hardware interface with the flash memory requires accessing to all registers of the hardware, which is for the issuing of FACI commands. Table 11 gives information on all of these areas.

Table 11. Information on the Hardware Interface Area

Area	Address	Capacity
Area containing the various registers of the hardware	See section 1.2, Registers.	See section 1.2, Registers.
FACI command-issuing area	407E 0000h	4 bytes

Refer to the user's manual for information on the addresses of the flash memory.

2.4 Registers

This section gives information on registers to which access is required. When nothing is mentioned in particular, the initialization condition of the register is only a reset.

For information on the option byte storage registers, see the user's manual for the product you are using.

Table 12. List of Registers

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Reference Page
4001 E416h	FLASH	Flash P/E Protect Register	FWEPROR	8	8	
407F E010h	FLASH	Flash Access Status Register	FASTAT	8	8	58
407F E014h	FLASH	Flash Access Error Interrupt Enable Register	FAEINT	8	8	60
407F E018h	FLASH	Flash Ready Interrupt Enable Register	FRDYIE	8	8	60
407F E030h	FLASH	FACI Command Start Address Register	FSADDR	32	32	61
407F E034h	FLASH	FACI Command End Address Register	FEADDR	32	32	62
407F E080h	FLASH	Flash Status Register	FSTATR	32	32	62
407F E084h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	66
407F E08Ch	FLASH	Flash Sequencer Set-Up Initialization Register	FSUINITR	16	8, 16	68
407F E0A0h	FLASH	FACI Command Register	FCMDR	16	16	68
407F E0D0h	FLASH	Data Flash Blank Check Control Register	FBCCNT	8	8	69
407F E0D4h	FLASH	Data Flash Blank Check Status Register	FBCSTAT	8	8	69
407F E0D8h	FLASH	Data Flash Programming Start Address Register	FPSADDR	32	32	70
407F E0DCh	FLASH	Flash Access Window Monitor Register	FAWMON	32	32	71
407F E0E0h	FLASH	Flash Sequencer Processing Switching Register	FCPSR	16	16	72
407F E0E4h	FLASH	Flash Sequencer Processing Clock Notification Register	FPCKAR	16	8, 16	72
407F E0E8h	FLASH	Flash Start-Up Area Control Register	FSUACR	16	16	73
407F C040h	FLASH	Data Flash Access Wait Register	FCKMHZ	8	8	74

2.4.1 Flash P/E Protect Register (FWEPROR)

Address (es): 4001 E416h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	FLWE[1:0]	
Value after reset	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b1-b0	FLWE[1:0]	Flash Programming and Erasure	00: Prohibits programming and erasure of the code flash, data flash or blank checking. 01: Permits programming and erasure of the code flash, data flash or blank checking. 10: Prohibits programming and erasure of the code flash, data flash or blank checking. 11: Prohibits programming and erasure of the code flash, data flash or blank checking.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

It is possible that the programming and erasure of the code flash memory, data flash memory or blank checking are prohibited by software.

FWEPROR register is initialized by a reset due to the mainly following,

- The signal on the RES# pin
- The transitions to the deep software standby mode
- The transitions to the software standby mode

* refer to the document of Reset about other reset conditions**.**

FLWE [1:0] Bits (Flash Programming and Erasure)

These bits are used to set the flash P/E protection. The value after reset is “10” and the programming and erasure of the code flash, data flash and blank checking are prohibited.

2.4.2 Flash Access Status Register (FASTAT)

Address (es): 407F E010h

	b7	b6	b5	b4	b3	b2	b1	b0
	CFAE	—	—	CMDLK	DFAE	—	—	—
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	DFAE	Data Flash Memory Access Violation Flag	0: No data flash memory access violation has occurred. 1: A data flash memory access violation has occurred.	R/W*1
b4	CMDLK	Command Lock Flag	0: The flash sequencer is not in the command-locked state. 1: The flash sequencer is in the command-locked state	R
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	CFAE	Code Flash Memory Access Violation Flag	0: No code flash memory access violation has occurred. 1: A code flash memory access violation has occurred.	R/W*1

Note: 1. Only 0 can be written to clear the flag after 1 is read.

The FASTAT register indicates whether a code flash or data flash memory access violation has occurred. If any of the CFAE, CMDLK and DFAE bits is set to 1, the flash sequencer enters the command-locked state (see section 2.8.2, Error Protection). To release it from the command-locked state, a status clear command or forced stop command must be issued to the FACI.

DFAE Bit (Data Flash Memory Access Violation Flag)

This bit indicates whether a data flash memory access violation occurred. When this bit is set to 1, the ILGLERR bit in the FSTATR register is set to 1, placing the flash sequencer in the command-locked state.

[Setting Conditions]

In general, commands being issued in data flash memory P/E mode as described below.

- An FACI command being issued while the setting of b18 to b0 in the FSADDR register is 1 0000h to 7 FFFFh (indicating the reserved portion of the data area)

[Clearing Condition]

- When this bit is written to 0 after this bit is set to 1.
- When the flash sequencer starts to process a status clear or forced stop command.

CMDLK Bit (Command Lock Flag)

This bit indicates that the flash sequencer is in the command-locked state.

[Setting Condition]

- The flash sequencer detects an error and enters the command-locked state.

[Clearing Condition]

- When the flash sequencer starts to process a status clear or forced stop command.

CFAE Bit (Code Flash Memory Access Violation Flag)

This bit indicates whether a code flash memory access violation has occurred. If this bit is set to 1, the ILGLERR bit in the FSTATR register is set to 1, placing the flash sequencer in the command-locked state.

[Setting Conditions]

An FACI command being issued in code flash memory P/E mode while settings are as follows:

- The setting of the FSADDR register is reserved portion of the user area.
- A configuration set command being issued while the setting of the FSADDR register is out of 0000 A100h to 0000 A170h.

[Clearing Condition]

- When this bit is written to 0 after this bit is set to 1.
- When the flash sequencer starts to process a status clear or forced stop command.

2.4.3 Flash Access Error Interrupt Enable Register (FAEINT)

Address (es): 407F E014h

	b7	b6	b5	b4	b3	b2	b1	b0
	CFAEIE	—	—	CMDLKIE	DFAEIE	—	—	—
Value after reset	1	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	DFAEIE	Data Flash Memory Access Violation Interrupt Enable	0: Generation of an FIFERR interrupt request is disabled when FASTAT.DFAE is set to 1. 1: Generation of an FIFERR interrupt request is enabled when FASTAT.DFAE is set to 1.	R/W
b4	CMDLKIE	Command Lock Interrupt Enable	0: Generation of an FIFERR interrupt request is disabled when FASTAT.CMDLK is set to 1. 1: Generation of an FIFERR interrupt request is enabled when FASTAT.CMDLK is set to 1.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	CFAEIE	Code Flash Memory Access Violation Interrupt Enable	0: Generation of an FIFERR interrupt request is disabled when FASTAT.CFAE is set to 1. 1: Generation of an FIFERR interrupt request is enabled when FASTAT.CFAE is set to 1.	R/W

The FAEINT register enables or disables generation of a flash access error (FIFERR) interrupt request.

IE Bit (Data Flash Memory Access Violation Interrupt Enable)

This bit enables or disables generation of an FIFERR interrupt request when a data flash memory access violation occur leading to the DFAE bit in the FASTAT register being set to 1.

CMDLKIE Bit (Command Lock Interrupt Enable)

This bit enables or disables generation of an FIFERR interrupt request when the flash sequencer enters the command-locked state leading to the CMDLK bit in the FASTAT register being set to 1.

CFAEIE Bit (Code Flash Memory Access Violation Interrupt Enable)

This bit enables or disables generation of an FIFERR interrupt request when a code flash memory access violation occur leading to the CFAE bit in the FASTAT register being set to 1.

2.4.4 Flash Ready Interrupt Enable Register (FRDYIE)

Address (es): 407F E018h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	FRDYIE
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FRDYIE	Flash Ready Interrupt Enable	0: Generation of an FRDY interrupt request is disabled 1: Generation of an FRDY interrupt request is enabled	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The FRDYIE register enables or disables generation of a flash ready (FRDY) interrupt.

FRDYIE Bit (Flash Ready Interrupt Enable)
This bit is used to enable or disable generation of an FRDY interrupt request when the FRDY bit in the FSTATR register is changed from 0 to 1 on completion of processing by the flash sequencer of programming, erasure or a blank checking command.

2.4.5 FACI Command Start Address Register (FSADDR)

Address (es): 407F E030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FSADDR[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FSADDR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description		R/W
b31 to b0	FSADDR [31:0]	Start Address for FACI Command Processing	[Command] Program (code flash memory): Program (data flash memory): 4, 8, 16-byte writing: Erase1 (code flash memory): Erase1 (data flash memory): Erase 2 (data flash memory): Blank check: Configuration set:	[Address boundary] 128-byte 4, 8,16 -byte 8-KB or 32-KB 64-byte 64-byte 4-byte 16-byte	R/W*1

Note: 1. Writing to these bits is only possible when the FRDY bit in the FSTATR register is 1. Writing to these bits while the FRDY bit = 0 is ignored. Note that b0 and b1 are read-only.

The FSADDR register specifies the address where the target area for command processing starts when the FACI command for programming, Erase1/2, blank checking, configuration setting is issued.

The FSADDR value is initialized when the SUINIT bit in the FSUINITR register is set to 1. It is also initialized by a reset.

FSADDR [31:0] Bits (Start Address for FACI Command Processing)

These bits specify the start address for FACI command processing. The bits from b31 to b24 are ignored in FACI command processing for the code flash memory. The bits from b31 to b19 are ignored in FACI command processing for the data flash memory. Bits corresponding to address bits of lower order than the corresponding boundary listed above are also ignored.

Refer to the user's manual for information on the addresses of the code flash memory and the data flash memory.

Refer to the MCU user's manual for information on the addresses of the configuration setting.

2.4.6 FACI Command End Address Register (FEADDR)

Address (es): 407F E034h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FEADDR[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FEADDR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	FEADDR [31:0]	End Address for FACI Command Processing	The end address for FACI command processing	R/W*1

Note: 1. Writing to these bits is only possible when the FRDY bit in the FSTATR register is 1. Writing to these bits while the FRDY bit = 0 is ignored. Note that b0 and b1 are read-only.

The FEADDR register specifies the end address of the target area for blank check command processing. When incremental mode is selected as the addressing mode for blank checking (that is, when FBCCNT.BCDIR = 0), the address specified in the FSADDR register should be smaller than the address in the FEADDR register. Conversely, the address in the FSADDR register should be larger than the address in the FEADDR register when decremental mode is selected as the addressing mode for blank checking (i.e. when FBCCNT.BCDIR = 1). If the settings of the BCDIR, FSADDR, and FEADDR bits are inconsistent with the above rules, the flash sequencer enters the command-locked state (see section 2.8.2, Error Protection).

The FEADDR value is initialized when the SUINIT bit in the FSUINITR register is set to 1. It is also initialized by a reset.

FEADDR [31:0] Bits (End Address for FACI Command Processing)

These bits specify the end address for blank check command processing. The bits from b31 to b19, b1, and b0 are ignored in command processing.

Refer to the user's manual for information on the addresses of the data flash memory.

2.4.7 Flash Status Register (FSTATR)

Address (es): 407F E080h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	ILGCOMERR	FESETERR	SECERR	OTERR	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	DBFULL	ERSSPD	PRGSPD	—	FLWEERR	—	—	—	—	—	—
Value after reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	FLWEERR	Flash Write/Erase Protect Error Flag	0: An error has not occurred. 1: An error has occurred.	R
b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b8	PRGSPD	Programming Suspend Status Flag	0: The flash sequencer is in a state other than those corresponding to the value 1. 1: The flash sequencer is in the programming suspension processing state or the programming suspended state.	R
b9	ERSSPD	Erasure Suspend Status Flag	0: The flash sequencer is in a state other than those corresponding to the value 1. 1: The flash sequencer is in the erasure suspension processing state or the erasure-suspended state.	R
b10	DBFULL	Data Buffer Full Flag	0: The data buffer is empty. 1: The data buffer is full.	R
b11	SUSRDY	Suspend Ready Flag	0: The flash sequencer cannot receive P/E suspend commands. 1: The flash sequencer can receive P/E suspend commands.	R
b12	PRGERR	Programming Error Flag	0: Programming has been completed successfully. 1: An error has occurred during programming.	R
b13	ERSERR	Erasure Error Flag	0: Erasure has been completed successfully. 1: An error has occurred during erasure.	R
b14	ILGLERR	Illegal Command Error Flag	0: The flash sequencer has not detected an illegal FACI command or illegal flash memory access. 1: The flash sequencer has detected an illegal FACI command or illegal flash memory access.	R
b15	FRDY	Flash Ready Flag	0: Program, Erase1/2, P/E suspend, P/E resume, forced stop, blank check or configuration set command processing is in progress. 1: None of the above is in progress.	R
b19 to b16	–	Reserved	These bits are read as 0. The write value should be 0.	R/W
b20	OTERR	Other Error	0: "Status Clear" or "Forced Stop" command processing is completed. 1: An error has been detected.	R
b21	SECERR	Security Error	0: "Status Clear" or "Forced Stop" command processing is completed. 1: An error has been detected.	R
b22	FESETERR	FENTRY Setting Error	0: "Status Clear" or "Forced Stop" command processing is completed. 1: An error has been detected.	R
b23	ILGCOMERR	Illegal Command Error	0: "Status Clear" or "Forced Stop" command processing is completed. 1: An error has been detected.	R
b31 to b24	–	Reserved	These bits are read as 0. The write value should be 0.	R/W

The FSTATR register indicates the state of the flash sequencer.

FLWEERR Bit (Flash Write/Erase Protect Error Flag)

This bit indicates a violation of the flash memory overwrite protection setting in the FWEPROR register. If this bit is 1, the flash sequencer is in the command-locked state.

[Clearing Condition]

- The flash sequencer starts processing of a forced stop command.

PRGSPD Bit (Programming Suspend Status Flag)

This bit indicates that the flash sequencer is in the programming suspension processing state or programming suspended state.

[Setting Condition]

- The flash sequencer starts processing in response to a programming suspend command.

[Clearing Conditions]

- Reception of the P/E resume command by the flash sequencer (after write access to the FACI command-issuing area is completed).
- The flash sequencer starts processing of a forced stop command.

ERSSPD Bit (Erasure Suspend Status Flag)

This bit indicates that the flash sequencer is in the erasure suspension processing state or erasure suspended state.

[Setting Condition]

- The flash sequencer starts processing in response to an erasure suspend command.

[Clearing Conditions]

- Reception of the P/E resume command by the flash sequencer (after write access to the FACI command-issuing area is completed).
- The flash sequencer starts processing of a forced stop command.

DBFULL Bit (Data Buffer Full Flag)

This bit indicates the state of the data buffer when a program command is issued. The FACI incorporates a buffer for write data (data buffer). When data for writing to the flash memory are written to the FACI command-issuing area while the data buffer is full, the FACI inserts a wait cycle in the peripheral bus.

[Setting Condition]

- The data buffer becomes full while program commands are being issued.

[Clearing Condition]

- The data buffer becomes empty.

SUSRDY Bit (Suspend Ready Flag)

This bit indicates whether the flash sequencer can receive a P/E suspend command.

[Setting Condition]

- After starting programming/erasure processing, the flash sequencer enters a state in which P/E suspend commands can be received.

[Clearing Conditions]

- Reception of the P/E suspend command or forced stop command by the flash sequencer (after write access to the FACI command-issuing area is completed).
- During programming or erasure, the flash sequencer enters the command-locked state.
- Programming or erasure has been completed.

PRGERR Bit (Programming Error Flag)

This bit indicates the result of programming of the flash memory. If this bit is 1, the flash sequencer is in the command-locked state.

[Setting Conditions]

- An error occurs during programming.

[Clearing Condition]

- The flash sequencer starts processing of a status clear or forced stop command.

ERSERR Bit (Erasure Error Flag)

This bit indicates the result of erasure of the flash memory. If this bit is 1, the flash sequencer is in the command-locked state.

[Setting Conditions]

- An error has occurred during erasure.

[Clearing Condition]

- The flash sequencer starts processing of a status clear or forced stop command.

ILGLERR Bit (Illegal Command Error Flag)

This bit indicates that the flash sequencer has detected an illegal FACI command or flash memory access. If this bit is 1, the flash sequencer is in the command-locked state.

[Setting Conditions] (See section 2.8.2, Error Protection)

- The flash sequencer has detected an illegal command.
- The flash sequencer has detected illegal flash memory access.
- The setting of FENTRYR is invalid.

[Clearing Condition]

- The flash sequencer starts processing of a status clear or forced stop command while the DFAE or CFAE bit in the FASTAT register is 0.

If the flash sequencer completes processing of a status clear or forced stop command while the CFAE or DFAE bit in the FASTAT register is 1, this bit is set to 1. This bit is temporarily set to 0 during processing of a forced stop command, and is re-set to 1 when the CFAE or DFAE bit is detected as 1 on completion of command processing.

FRDY Bit (Flash Ready Flag)

This bit indicates the command processing state of the flash sequencer.

[Setting Conditions]

- The flash sequencer completes command processing.
- The flash sequencer receives a P/E suspend command and suspends programming of the flash memory.
- The flash sequencer has received a forced stop command and ended command processing.

[Clearing Conditions]

- The flash sequencer has received an FACI command.
- For programming and configuration setting, the first write access to the FACI command-issuing area.
- For other commands, the last write access to the FACI command-issuing area.

OTERR Bit (Other Error Flag)

When this bit is "1", flash sequencer enters "Command Lock" state.

[Setting conditions]

- An error has been detected.

[Clearing condition]

"Status Clear" or "Forced Stop" command processing is completed.

SECERR Bit (Security Error Flag)

When this bit is "1", flash sequencer enters "Command Lock" state.

[Setting conditions]

An error has been detected.

[Clearing condition]

"Status Clear" or "Forced Stop" command processing is completed.

FESETERR Bit (FENTRY Setting Error Flag)

When this bit is "1", flash sequencer enters "Command Lock" state.

[Setting conditions]

An error has been detected.

[Clearing condition]

"Status Clear" or "Forced Stop" command processing is completed.

ILGCOMERR Bit (Illegal Command Error Flag)

When this bit is "1", flash sequencer enters "Command Lock" state.

[Setting conditions]

An error has been detected.

[Clearing condition]

"Status Clear" or "Forced Stop" command processing is completed.

2.4.8 Flash P/E Mode Entry Register (FENTRYR)

Address (es): 407F E084h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
				KEY[7:0]					FENTRYD	—	—	—	—	—	—	FENTRYC
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FENTRYC	Code Flash P/E Mode Entry	0: Code flash is in read mode. 1: Code flash is in P/E mode.	R/W*1, *2
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	FENTRYD	Data Flash P/E Mode Entry	0: Data flash is in read mode. 1: Data flash is in P/E mode.	R/W*1, *2
b15 to b8	KEY[7:0]	Key Code		R/W*3

Note 1. Writing to these bits is only possible when the FRDY bit in the FSTATR register is 1. Writing to these bits while the FRDY bit = 0 is ignored.

Note 2. Writing to these bits is only possible when 16 bits are written and the value written to the KEY bits is AAh.

Note 3. Written values are not retained by these bits.

FENTRYR is used to specify code flash P/E mode and data flash P/E mode. To specify code flash P/E mode or data flash P/E mode so that the flash sequencer can receive FACI commands, set either the FENTRYD or FENTRYC bit to 1 to place the flash sequencer in P/E mode.

Note that setting this register to a value other than 0001h and 0080h, the ILGLERR bit in the FSTATR register will be set to 1, leading to the flash sequencer being placed in the command-locked state.

FENTRYR is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

FENTRYC Bit (Code Flash P/E Mode Entry)

This bit specifies the P/E mode for code flash memory.

[Setting Condition]

- 1 being written to the FENTRYC bit while writing to FENTRYR is enabled and FENTRYR is 0000h.

[Clearing Conditions]

- 8 bits being written to FENTRYR while the FRDY bit is 1.
- A value other than AAh is specified in the KEY bits and 16 bits are written to FENTRYR while the FRDY bit is 1.
- 0 being written to the FENTRYC bit while writing to FENTRYR is enabled.
- FENTRYR being written to while writing to FENTRYR is enabled and the value of FENTRYR is other than 0000h.

FENTRYD Bit (Data Flash P/E Mode Entry)

This bit specifies the P/E mode for data flash memory.

[Setting Condition]

- 1 being written to the FENTRYD bit while writing to FENTRYR is enabled and FENTRYR is 0000h.

[Clearing Conditions]

- 8 bits being written to FENTRYR while the FRDY bit is 1
- Writing of 16 bits to FENTRYR with a value other than AAh specified for the KEY bits while the FRDY bit is 1
- 0 being written to the FENTRYD bit while writing to FENTRYR is enabled
- FENTRYR being written to while writing to FENTRYR is enabled and the value of FENTRYR is other than 0000h

KEY [7:0] Bits (Key Code)

These bits control permission and prohibition of writing to the FENTRYD or FENTRYC bits.

2.4.9 Flash Sequencer Set-Up Initialization Register (FSUINITR)

Address (es): 407F E08Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
				KEY[7:0]					—	—	—	—	—	—	—	SUINIT
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SUINIT	Set-Up Initialization	0: The FEADDR, FCPSR, FSADDR, FENTRYR, and FBCCNT flash sequencer set-up registers keep their current values. 1: The FEADDR, FCPSR, FSADDR, FENTRYR, and FBCCNT flash sequencer set-up registers are initialized.	R/W*1, *2
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code		R/W*3

Note 1. Writing to these bits is only possible when the FRDY bit in the FSTATR register is 1. Writing to these bits while the FRDY bit = 0 is ignored.

Note 2. Writing to these bits is only possible when 16 bits are written and the value written to the KEY bits is 2Dh.

Note 3. Written values are not retained by these bits.

FSUINITR is used for initialization of the flash sequencer set-up.

SUINIT Bit (Set-Up Initialization)

This bit initializes the following flash sequencer set-up registers.

- FEADDR
- FCPSR
- FSADDR
- FENTRYR
- FBCCNT

KEY [7:0] Bits (Key Code)

These bits control permission and prohibition of writing to the SUINIT bit.

2.4.10 FACI Command Register (FCMDR)

Address (es): 407F E0A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
				CMDR[7:0]								PCMDR[7:0]				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	PCMDR[7:0]	Pre-command Flag	The command just before the latest command is stored.	R
b15 to b8	CMDR[7:0]	Command Flag	The latest command is stored.	R

FCMDR records the two most recent commands accepted by the FACI.

PCMDR [7:0] Bits (Pre-command Flag)

These bits indicate the command received immediately before the latest command received by the FACI.

CMDR [7:0] Bits (Command Flag)

These bits indicate the latest command received by the FACI.

Table 13. States of FCMDR after Receiving Commands

Command	CMDR	PCMDR
Program	E8h	Previous Command
Erase 1	D0h	20h
Erase 2	D0h	21h
P/E suspend	B0h	Previous Command
P/E resume	D0h	Previous Command
Status clear	50h	Previous Command
Forced stop	B3h	Previous Command
Blank check	D0h	71h
Configuration set	40h	Previous Command
Config Clear	D0h	43h

2.4.11 Blank Check Control Register (FBCCNT)

Address (es): 407F E0D0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BCDIR
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BCDIR	Blank Check Direction	0: Blank checking is executed from lower addresses to higher addresses (incremental mode). 1: Blank checking is executed from higher addresses to lower addresses (decremental mode).	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FBCCNT specifies the addressing mode in processing of a blank check command. FBCCNT is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

BCDIR Bit (Blank Check Direction)

This bit specifies the addressing mode for blank checking.

2.4.12 Blank Check Status Register (FBCSTAT)

Address (es): 407F E0D4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BCST
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BCST	Blank Check Status Flag	0: The target area is in the non-programmed state (that is, is blank; the area has been erased but has not yet been re-programmed). 1: The target area has been programmed with 0s or 1s.	R
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FBCSTAT stores the results of checking in response to a blank check command.

BCST Bit (Blank Check Status Flag)

This bit indicates the results of checking in response to a blank check command.

2.4.13 Data Flash Programming Start Address Register (FPSADDR)

Address (es): 407F E0D8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PSADR [16]
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSADR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b16 to b0	PSADR[18:0]	Programmed Area Start Address	The address of the first programmed area	R
b31 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FPSADDR indicates the address of the first programmed area to be found in processing of a blank check command.

PSADR [16:0] Bits (Programmed Area Start Address)

These bits indicate the address of the first programmed area to be found in processing of a blank check command. The address is an offset from the address where the data flash memory starts. The setting of these bits is only effective if the BCST bit in the FBCSTAT register is 1, while the FRDY bit in the FSTATR register is 1. When the BCST bit in the FBCSTAT register is 0, the PSADR bit holds the address produced by the previous check.

2.4.14 Flash Access Window Monitor Register (FAWMON)

Address (es): 407F E0DCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BTFLG	—	—	—	—	FAWE[10:0]										
Value after reset	1/0	0	0	0	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FSPR	—	—	—	—	FAWS[10:0]										
Value after reset	1/0	0	0	0	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

Bit	Symbol	Bit Name	Description	R/W
b10 to b0	FAWS[10:0]	Start Block Address of Access Window	The start block address for the access window function	R
b14 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R
b15	FSPR	Protection Flag of programing to set Access Window, Boot Flag and Start-up Area Control	0: Protected state 1: Non-protected state	R
b26 to b16	FAWE[10:0]	End Block Address of Access Window	The end block address for the access window function	R
b30 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R
b31	BTFLG	Flag of Start-Up Area select for Boot Swap	0: The start-up area is the alternate block (block 1) 1: The start-up area is the default block (block 0)	R

FAWS [10:0] Bits (Start Block Address of Access Window)

These bits indicate the start block address of the access window.

In response to a reset or configuration set command, the FACI transfers data from the flash memory to this register.

FSPR Bit (Protection Flag of Programing to set Access Window)

This bit indicates the protection state against the configuration set command for the access window, the BTFLG bit and the start-up area control register.

In response to a reset or configuration set command, the FACI transfers data from the flash memory to this register.

FAWE [10:0] Bits (End Block Address of Access Window)

These bits indicate the end block address of the access window. The end block address is the next block address of the P/E acceptable region defined by the access window.

In response to a reset or configuration set command, the FACI transfers data from the flash memory to this register.

BTFLG Bit (Flag of Start-Up Area select for Boot Swap)

This bit indicates whether the address of the start-up area is exchanged for the boot swap function or not.

In response to a reset or configuration set command, the FACI transfers data from the flash memory to this register.

2.4.15 Flash Sequencer Processing Switching Register (FCPSR)

Address (es): 407F E0E0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ESUSPMD
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ESUSPMD	Erasure Suspend Mode	0: Suspension priority mode 1: Erasure priority mode	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FCPSR is for selecting the erasure suspension mode. FCPSR is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

ESUSPMD Bit (Erasure Suspend Mode)

This bit is for selecting the erasure suspension mode when a P/E suspend command is issued while the flash sequencer is executing erasure processing (see section 2.6.3.10, P/E Suspend Command). This bit should be set before issuing “Erase1 or Erase2” command.

2.4.16 Flash Sequencer Processing Clock Notification Register (FPCKAR)

Address (es): 407F E0E4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								PCKA[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	PCKA[7:0]	Flash Sequencer Operating Clock Notification	These bits are used to set the operating frequency of the flash sequencer while processing FACI commands.	R/W*1, *2
b15 to b8	KEY[7:0]	Key Code	Key code	R/W*3

Note 1. Writing to these bits is only possible when the FRDY bit in the FSTATR register is 1. Writing to these bits while the FRDY bit = 0 is ignored.

Note 2. Writing to these bits is only possible when 16 bits are written and the value written to the KEY bits is 1Eh.

Note 3. Written values are not retained by these bits.

FPCKAR specifies the operating frequency of the flash sequencer while processing FACI commands. The highest operating frequency for the given product is set as the initial value.

PCKA [7:0] Bits (Flash Sequencer Operating Clock Notification)

These bits specify the operating frequency of the flash sequencer while processing FACI commands. Set the desired frequency in these bits before issuing an FACI command. Specifically, convert the frequency represented in MHz into a binary number and set it in these bits.

Example:

Frequency is 35.9 MHz (PCKA = 24h)

Round up the first decimal place of 35.9 MHz to a whole number (= 36) and convert it into a binary number.

If the value set in these bits is smaller than the actual operating frequency of the flash sequencer, the flash memory overwriting characteristics cannot be guaranteed. If the value set in these bits is greater than the actual operating frequency of the flash sequencer, the flash memory overwriting characteristics can be guaranteed but the FACI command processing time such as the time overwriting takes will increase.

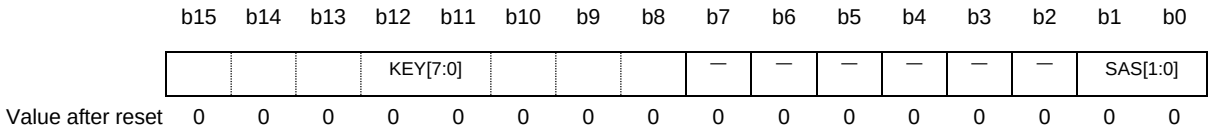
The minimum FACI command processing time is obtained when the operating frequency of the flash sequencer is the same as the PCKA value.

KEY [7:0] Bits (Key Code)

These bits control permission and prohibition of writing to the PCKA bit.

2.4.17 Flash Start-Up Area Control Register (FSUACR)

Address (es): 407F E0E8h



Bit	Symbol	Bit Name	Description	R/W
b1 to b0	SAS[1:0]	Start Up Area Select	0X: Start-up area is selected by BTFLG bit 10: Start-up area is temporarily switched to the default area (block0) 11: Start-up area is temporarily switched to the alternate area (block 1)	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	Key code	R/W*2

Note 1. Following described the write condition of these bits (these condition are required at the same time).
1. Access size to this register is 16 bits.
2. The value of KEY [7:0] is 66h.
3. The FSPR bit is 1.

Note 2. Written values are not retained by these bits.

The FSUAC register sets the start-up area for the boot swap function.

SAS [1:0] Bits (Start-up Area Select)

These bits are used to select the start-up area. Three methods are capable for changing the start-up area.

KEY [7:0] Bits (Key Code)

These bits control permission and prohibition of writing to the SAS [1:0] bits.

2.4.18 Data Flash Access Wait Register (FCKMHZ)

Address (es): 407F C040h

	b7	b6	b5	b4	b3	b2	b1	b0
	FCKMHZ[7:0]							
Value after reset	0	0	1	1	1	1	0	0

Set the frequency of the clock of DATA FLASH in FCKMHZ[7:0]. And it puts the access wait in accordance with the DATA FLASH frequency.

The number of wait in accordance with the setting of FCKMHZ

DATA FLASH Access Wait

FCKMHZ[7:0] *	Wait number
8'h00～8'h09	0
8'h0a～8'h13	1
8'h14～8'h1d	2
8'h1e～8'h27	3
8'h28～8'h31	4
8'h32～8'h3b	5
8'h3c	6
8’h3d～8’hff	Reserved

* clkf_bpf is assumed to max 60 MHz.

A read operation takes wait number + 2 cycles of FCLK.

2.5 Operating Modes of the Flash Sequencer

The flash sequencer has three operating modes as shown in Figure 28. Transitions between modes are initiated by changing the value of the FENTRYR register.

When the value of the FENTRYR register is 0000h, the flash sequencer is in read mode. In this mode, it does not receive FACI commands. The code flash memory and data flash memory are both readable.

When the value of the FENTRYR register is 0001h, the flash sequencer is in code flash P/E mode where the code flash memory can be programmed or erased by FACI commands. In this mode, the data flash memory is not readable. In addition, the code flash memory is not readable if background operation (BGO) is disabled. If BGO is enabled, the code flash memory is readable. As for the condition for enabling BGO, refer to the user’s manual for the product you are using.

When the value of the FENTRYR register is 0080h, the flash sequencer is in data flash P/E mode where the data flash memory can be programmed or erased by FACI commands. In this mode, the data flash memory is not readable. However, the code flash memory is readable.

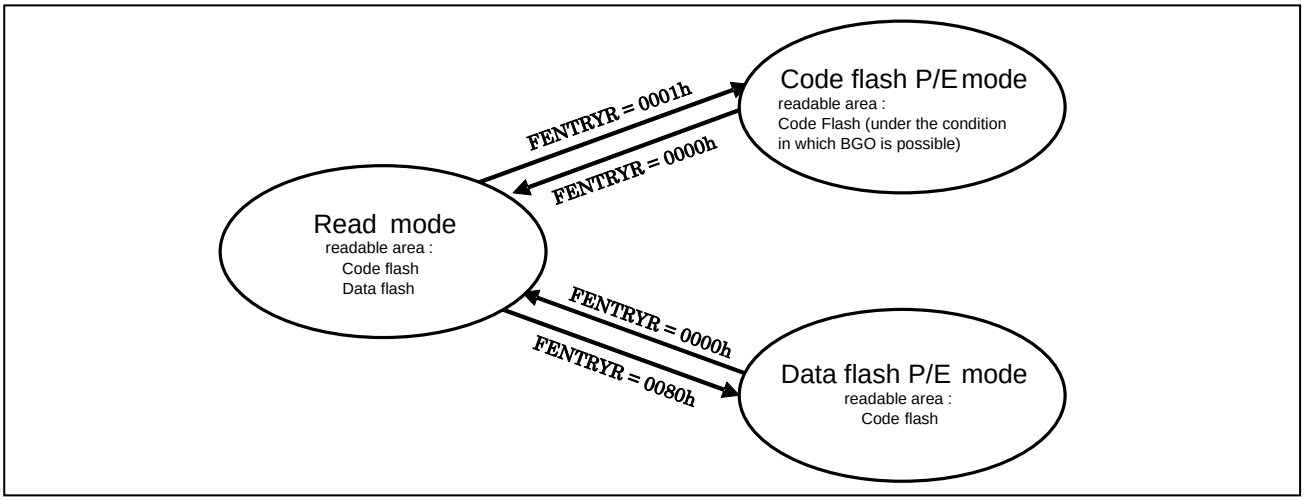


Figure 28. Modes of the Flash Sequencer

2.6 FACI Commands

2.6.1 List of FACI Commands

Table 14. List of FACI Commands

FACI Command	Function
Program	This is used to program the user area and data area. Units of programming are 128 bytes for the user area and 4, 8 or 16 bytes for the data area.
Erase 1	User area and data area can be erased. Erase unit is 8K bytes or 32K bytes for user area, and 64 bytes for data flash.
Erase 2	Data area can be erased. Erase unit is 64, 128 or 256 bytes for data flash.
P/E suspend	This suspends programming or erasure processing.
P/E resume	This resumes suspended programming or erasure processing.
Status clear	This initializes the ILGLERR, ERSERR, and PRGERR bits in the FSTATR register and releases the flash sequencer from the command-locked state.
Forced stop	This forcibly stops processing of FACI commands and initializes the FSTATR register.
Blank check	This is used to check if data areas are blank. Units of blank checking: 4 bytes to 64 KB (specified in 4-byte units).
Configuration set	This is used to set the ID, security function and safety function. Units of setting: 16 bytes.

The FACI commands are issued by writing to the FACI command-issuing area (see Table 11). When write access as shown in Table 15 proceeds in the specified state, the flash sequencer executes the processing corresponding to the given command (see section 2.6.2, Relationship between the Flash Sequencer State and FACI Commands).

Table 15. FACI Command Formats

FACI Commands	Number of Write Access	Data to be Written to the FACI Command-Issuing Area			
		1st Access	2nd Access	3rd to (N+2)th Access	(N+3)th Access
Program (user area) N = 64	67	E8h	40h (=N)	WD_1 to WD_{64}	D0h (*1)
Program (data area) 4-byte programming: N = 2 8-byte programming: N = 4 16-byte programming: N = 8	N+3	E8h	02h (=N) 04h (=N) 08h (=N)	WD_1 to WD_N(*2)	D0h (*1)
Erase 1 (Code Flash)	2	20h	D0h	-	-
Erase 1 (Data Flash 64 Byte)	2	20h	D0h	-	-
Erase 2 (Data flash 64/128/256 Byte	2	21h	D0h	-	-
P/E suspend	1	B0h	-	-	-
P/E resume	1	D0h	-	-	-
Status clear	1	50h	-	-	-
Forced stop	1	B3h	-	-	-
Blank check	2	71h	D0h	-	-
Configuration set N = 8	11	40h	08h (=N)	WD_1 to WD_8	D0h

Note1: When using RA6M1, RA6M2, RA6M3, or RA6T1, please check Appendix 1.

Note2: WD_N (N = 1, 2,…): Nth 16-bit data to be programmed.

The flash sequencer clears the FSTATR.FRDY bit to 0 at the start of processing of a command other than the status clear command and sets this bit to 1 on completion of command processing.

If the setting of the FRDYIE.FRDYIE bit is 1, a flash ready (FRDY) interrupt is generated when the FSTATR.FRDY bit is set to 1.

2.6.2 Relationship between the Flash Sequencer State and FACI Commands

The sets of FACI commands that can be accepted in each of the modes/states of the flash sequencer are fixed. FACI commands should be issued after the transition of the flash sequencer to the code flash P/E mode or data flash P/E mode and checking of the state of the flash sequencer. Use the FSTATR and FASTAT registers to check the state of the flash sequencer. In addition, the occurrence of errors in general can be checked by reading the CMDLK bit in the FASTAT register; its value is the logical OR of the ILGLERR, ERSERR, PRGERR, FCUERR, and FLWEERR bits in the FSTATR register.

Table 16 lists the available commands in each operating mode.

Table 16. Operating Mode and Available Commands

Operation Mode	FENTRYR	Available Commands
Read mode	0000h	None
Code flash P/E mode	0001h	Program Erase 1 P/E suspend P/E resume Status clear Forced stop Config Program
Data flash P/E mode	0080h	Program Erase 1 Erase 2 P/E suspend P/E resume Status clear Forced stop Blank check

Table 17 shows the state of the flash sequencer and acceptable FACI commands. An appropriate mode is assumed to have been set before the commands are executed.

Table 17. Acceptable FACI Commands and the State of the Flash Sequencer

	"Program" or "Erase1/2" command processing	"Config Program" command processing	"Program" or " Erase1/2" command suspension processing	"Blank Check" command processing	Programming Suspended	Erasure Suspended	Programming while Erasure is Suspended	Command-Locked State (FRDY = 1)	Command-Locked State (FRDY = 0)	Processing of Forced Stop Command	Other State
FRDY bit	0	0	0	0	1	1	0	1	0	0	1
SUSRDY bit	1	0	0	0	0	0	0	0	0	0	0
ERSSPD bit	0	0	0/1	0/1	0	1	1	0/1	0/1	0	0
PRGSPD bit	0	0	0/1	0/1	1	0	0	0/1	0/1	0	0
CMDLK bit	0	0	0	0	0	0	0	1	1	0	0
Program	X	X*5	X	X	X	O*4	X	X	X	X	O
Erase1/2	X	X*5	X	X	X	X	X	X	X	X	O
P/E suspend	O	X*5	X	X	X	X	X	--	X	X	--
P/E resume	X	X*5	X	X	O	O	X	X	X	X	X
Status clear	X	X*5	X	X	O	O	X	O	X	X	O
Forced stop	O	O*5	O	O	O	O	O	O	O	O	O
Blank check	X	X*5	X	X	O*1	O*1	X	X	X	X	O*1
Configuration set	X	X*5	X	X	X	X	X	X	X	X	O*1

o: Acceptable

×: Not acceptable (places the sequencer in the command-locked state)

—: Ignored

Note 1. Only acceptable in data flash P/E mode.

Note 2. Acceptable after a code flash "Erase1" command is finished correctly.

Note 3. Acceptable when programming area is other than erase suspending sector.

Note 4. When “Configuration set” is processing and in case of FSTATR.DBFULL bit = “1”, please do not issue this command.

2.6.3 Usage of FACI Commands

This section gives an overview of the usage of FACI commands.

2.6.3.1 Overview of Command Usage in Code Flash P/E Mode

Figure 29 and Figure 30 respectively show an overview of FACI command usage in code flash P/E mode for products in which background operation (BGO) is possible and that for products in which BGO is not possible. For which commands are available in code flash P/E mode, see Table 16.

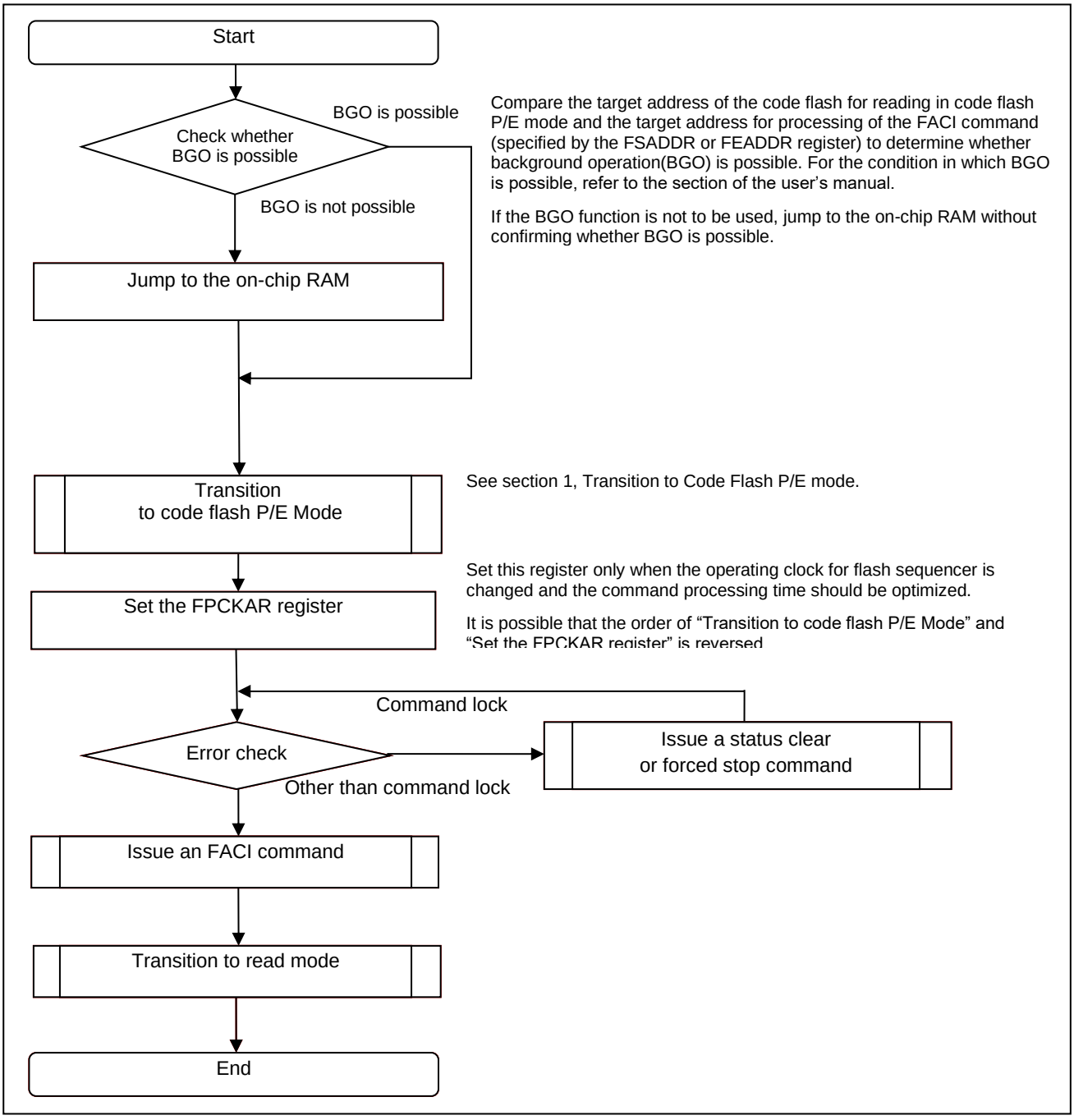


Figure 29. Overview of Command Usage in Code Flash P/E Mode (for products in which BGO is possible)

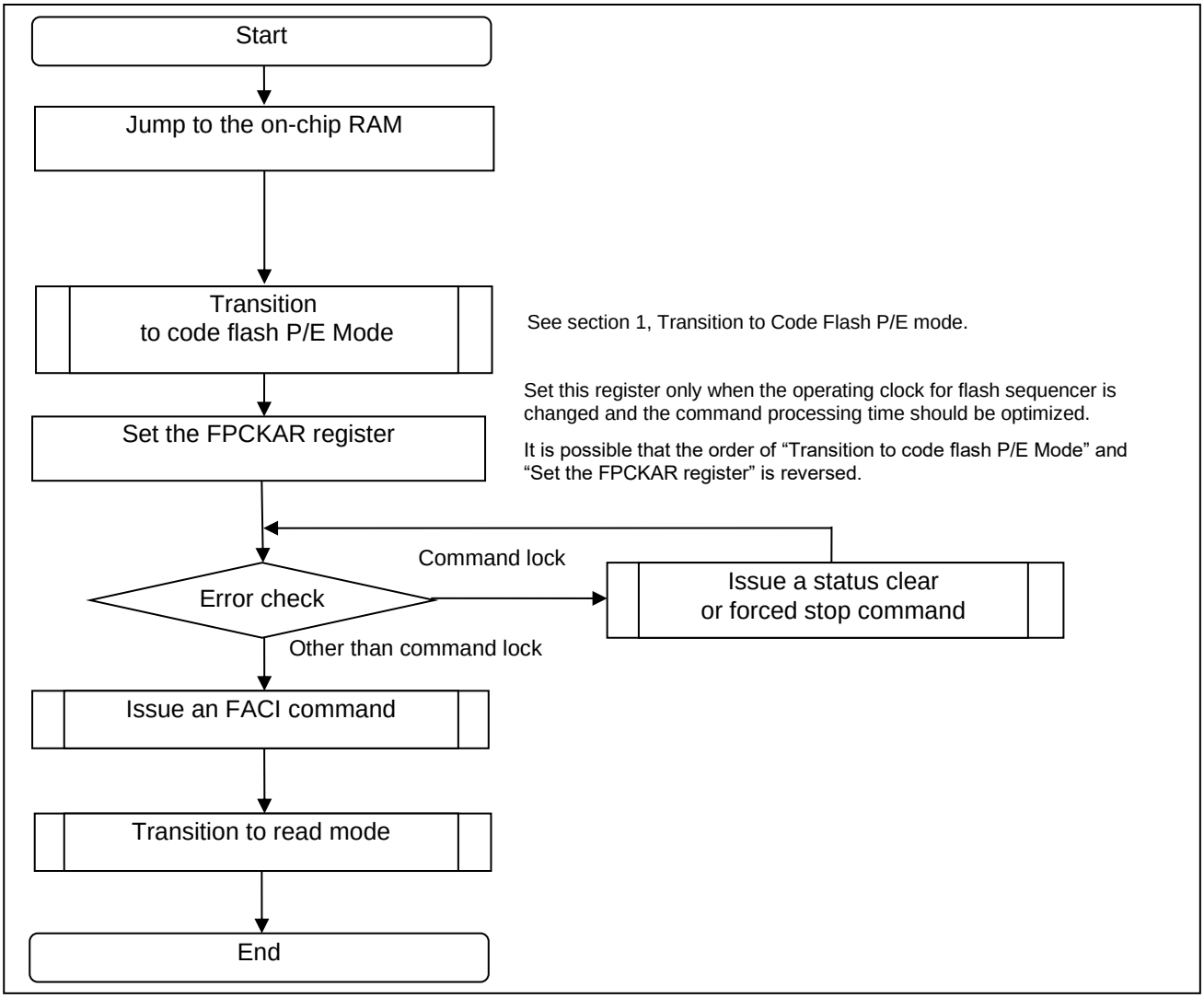


Figure 30. Overview of Command Usage in Code Flash P/E Mode (for products in which BGO is not possible)

2.6.3.2 Overview of Command Usage in Data Flash P/E Mode

An overview of FACI command usage in data flash P/E mode is shown below. For which commands are available in data flash P/E mode, Table 16.

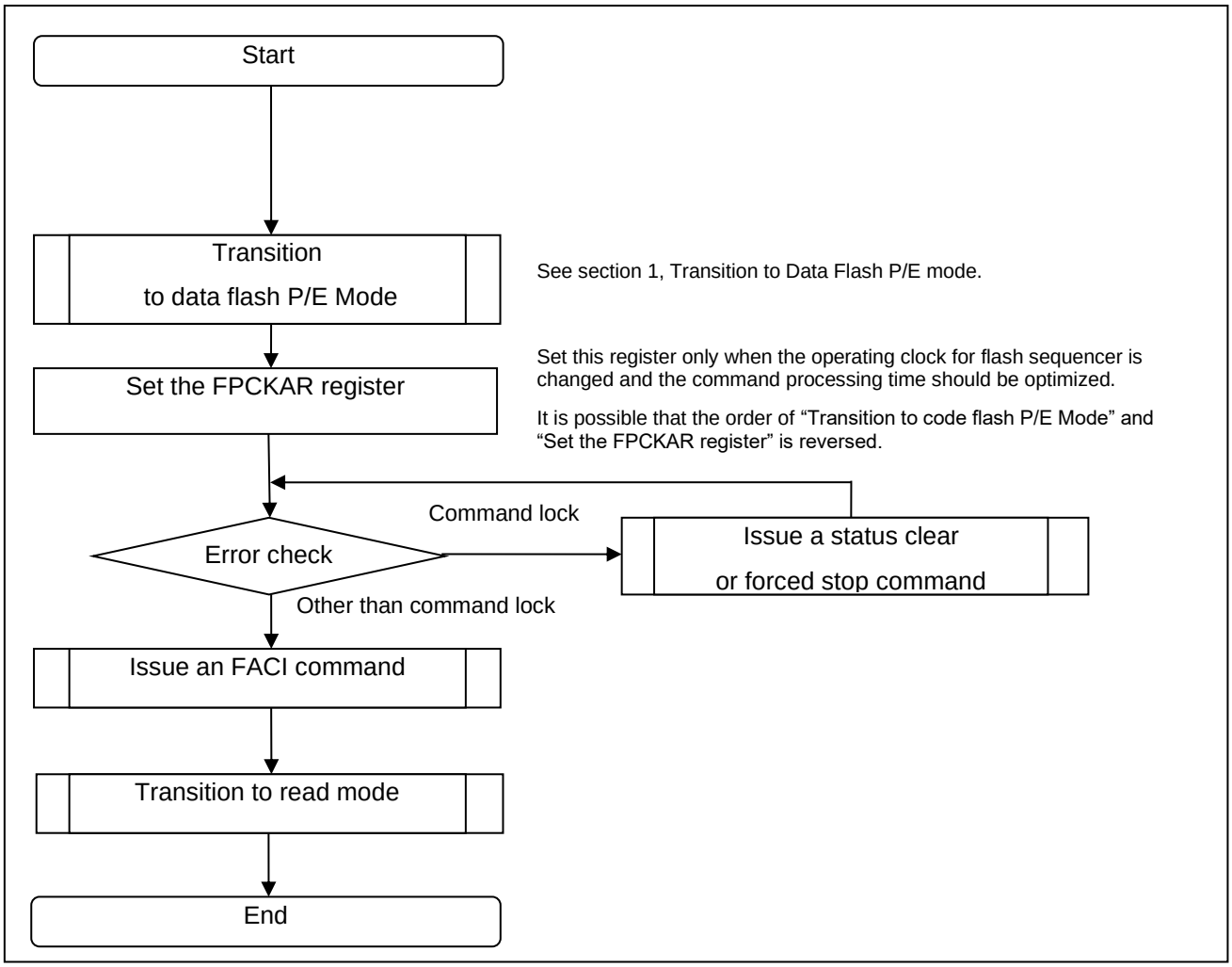


Figure 31. Overview of Command Usage in Data Flash P/E Mode

2.6.3.3 Transition to Code Flash P/E Mode

To issue the FACI commands for the code flash memory, a transition to code flash P/E mode is required. To cause the transition to code flash P/E mode, set the FENTRYRC bit in the FENTRYR register to 1.

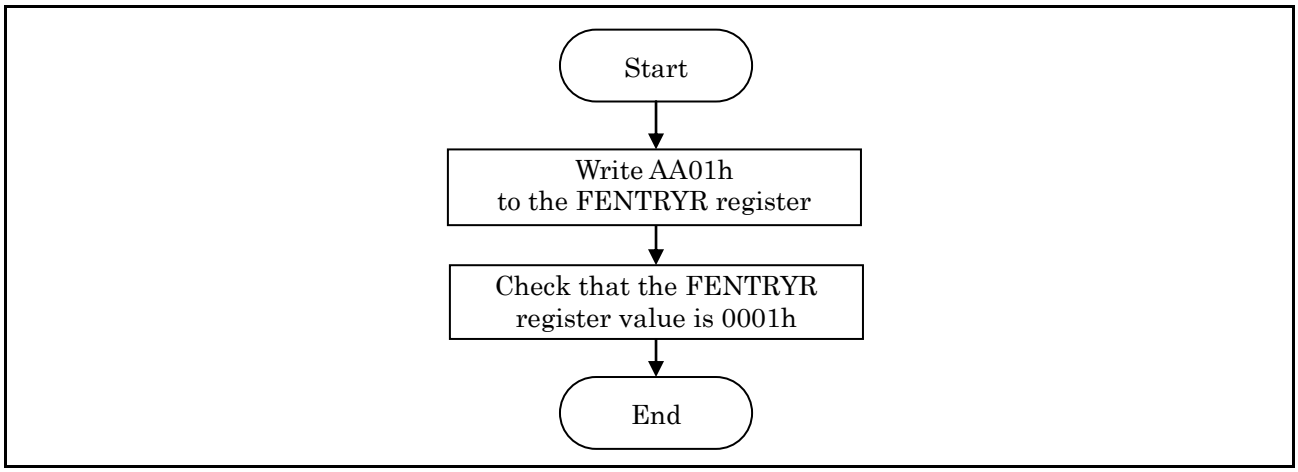


Figure 32. Procedure for Transition to Code Flash P/E Mode

2.6.3.4 Transition to Data Flash P/E Mode

To issue the FACI commands for the data flash memory, a transition to data flash P/E mode is required. To cause the transition to data flash P/E mode, set the FENTRYRD bit in the FENTRYR register to 1.

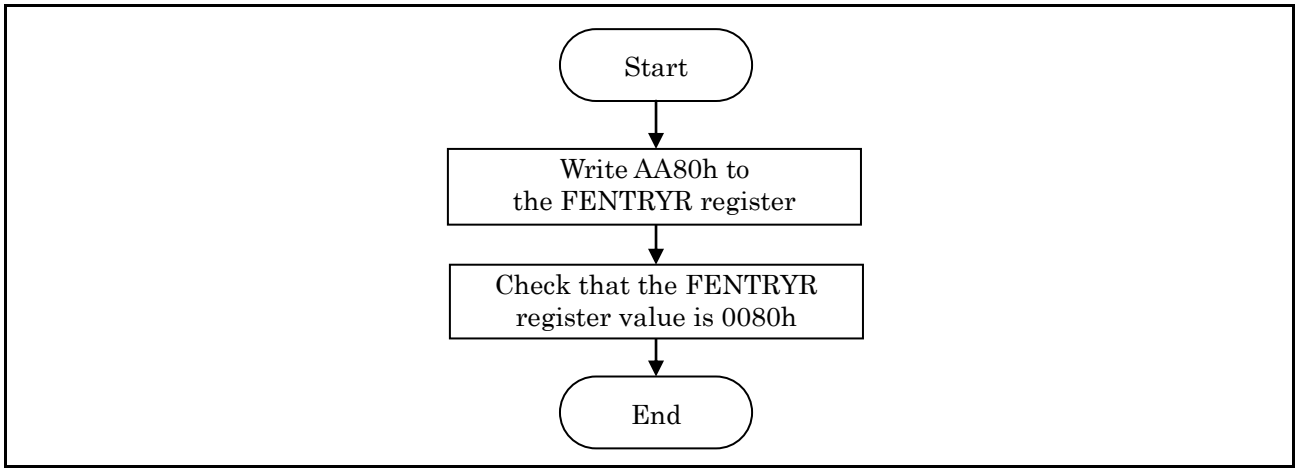
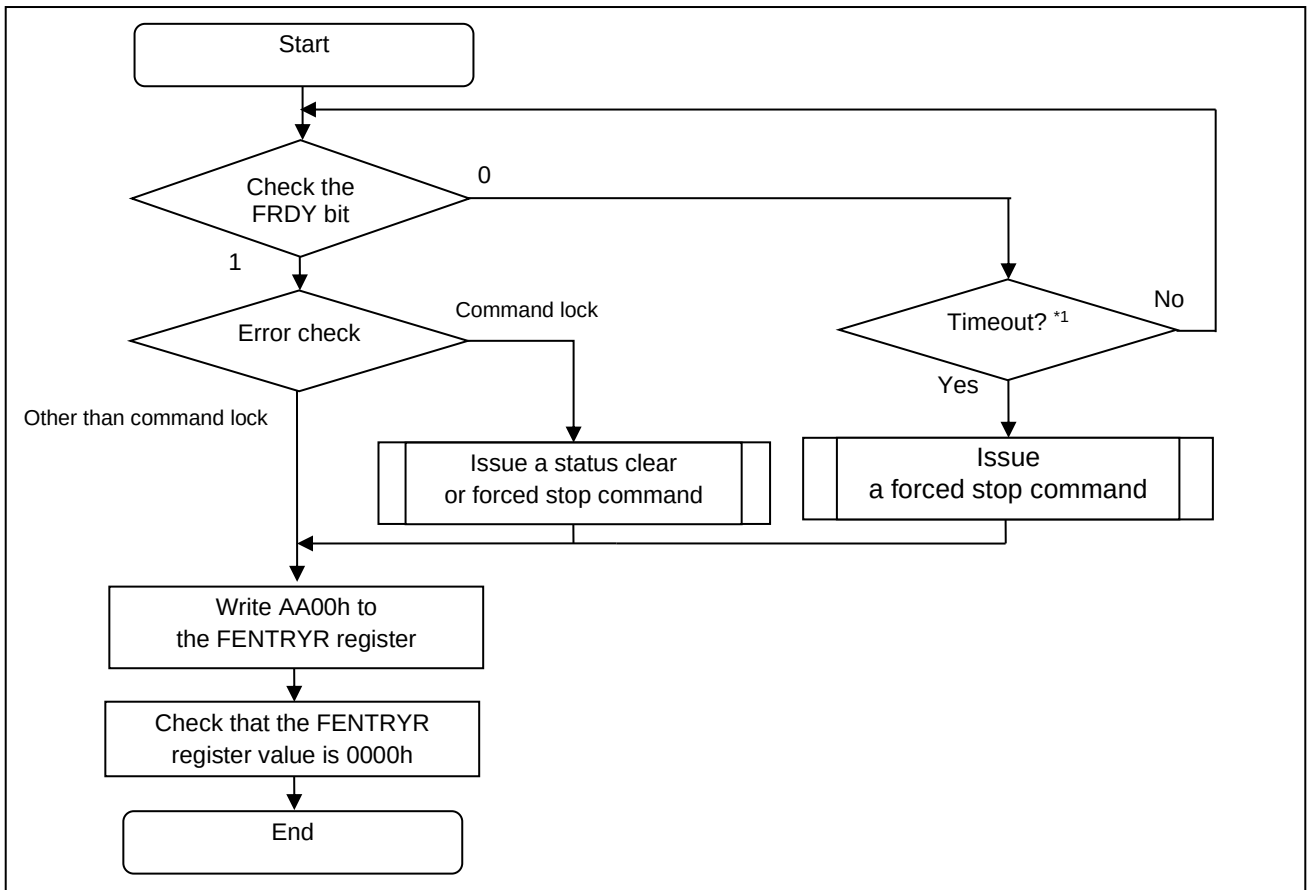


Figure 33. Procedure for Transition to Data Flash P/E Mode

2.6.3.5 Transition to Read Mode

To read the flash memory without using the BGO function, a transition to read mode is required. To cause the transition to read mode, set the FENTRYR register to 0000h. The transition to read mode should be made after processing by the flash sequencer is completed and while operation is in other than in the command-locked state.



Note: 1. Judgment of the timeout is based on 1.1 times the maximum time for processing of the FACI command that is in progress (see section 1. Electrical Characteristics)

Figure 34. Procedure for Transition to Read Mode

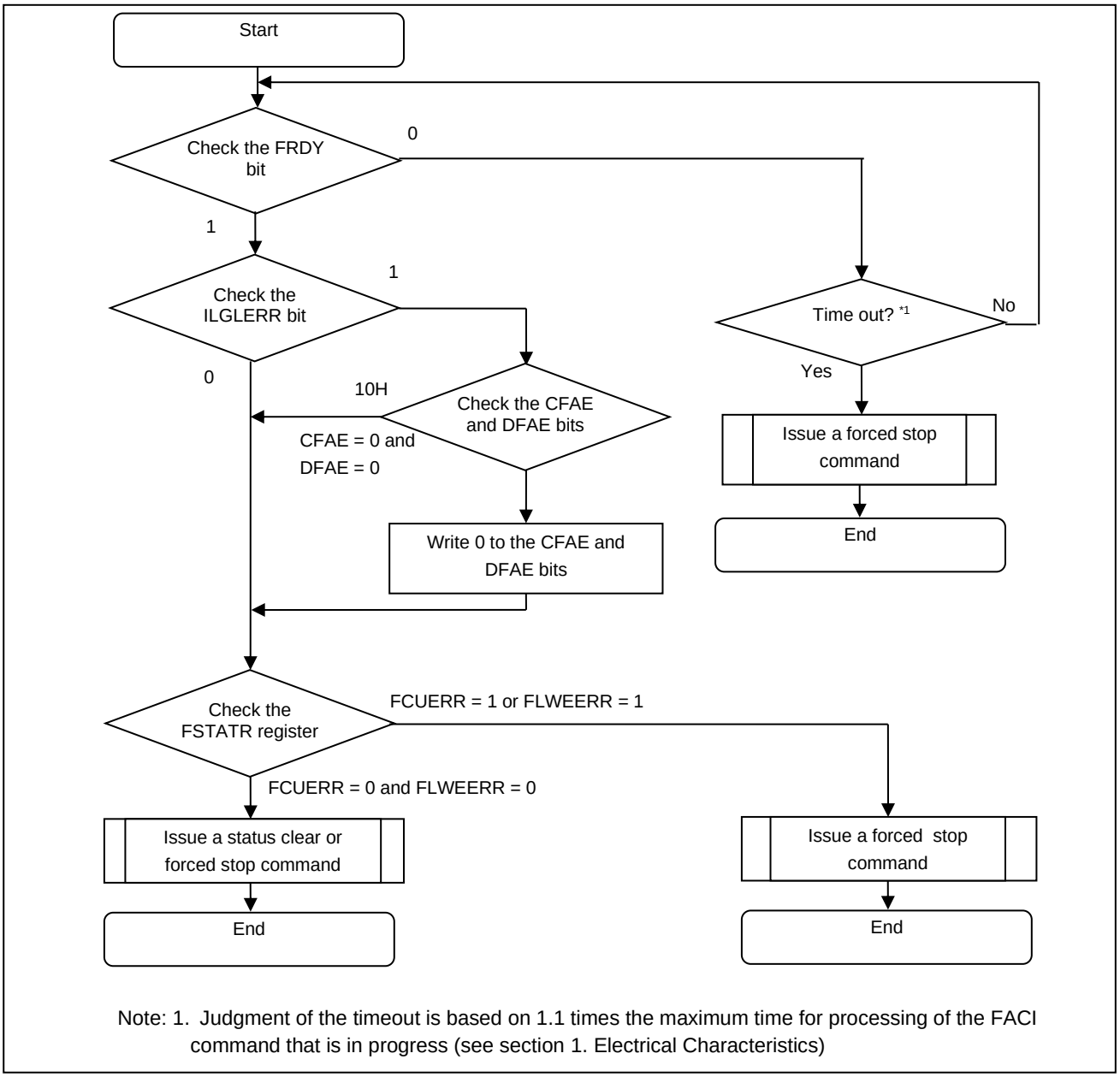
2.6.3.6 Recovery from the Command-Locked State

When the flash sequencer enters the command-locked state, FACI commands cannot be accepted. To release the sequencer from the command-locked state, use the status clear command, forced stop command, or FASTAT register.

When the command-locked state is detected by checking for an error before issuing the P/E suspend command, the FRDY bit in the FSTATR register may hold 0 although command processing has not been completed. If processing is not completed in time beyond the maximum programming/erasure time specified in the electrical characteristics, this can be considered a timeout, and the flash sequencer should be stopped by the forced stop command.

When the ILGLERR bit in the FSTATR register is 1, check the FASTAT value. If the CFAE or DFAE bit in the FASTAT register is 1, the status clear and forced stop commands cannot be used to release the sequencer from the command-locked state.

The FCUERR and FLWEERR bits in the FSTATR register are not changed from 1 to 0 by the status clear command. When these bits are set to 1, use the forced stop command for release from the command-locked state. The other bits that indicate the command-locked state can be changed from 1 to 0 by the status clear or forced stop command.



Note: 1. Judgment of the timeout is based on 1.1 times the maximum time for processing of the FACI command that is in progress (see section 1. Electrical Characteristics)

Figure 35. Recovery from the Command-Locked State

2.6.3.7 Program Command

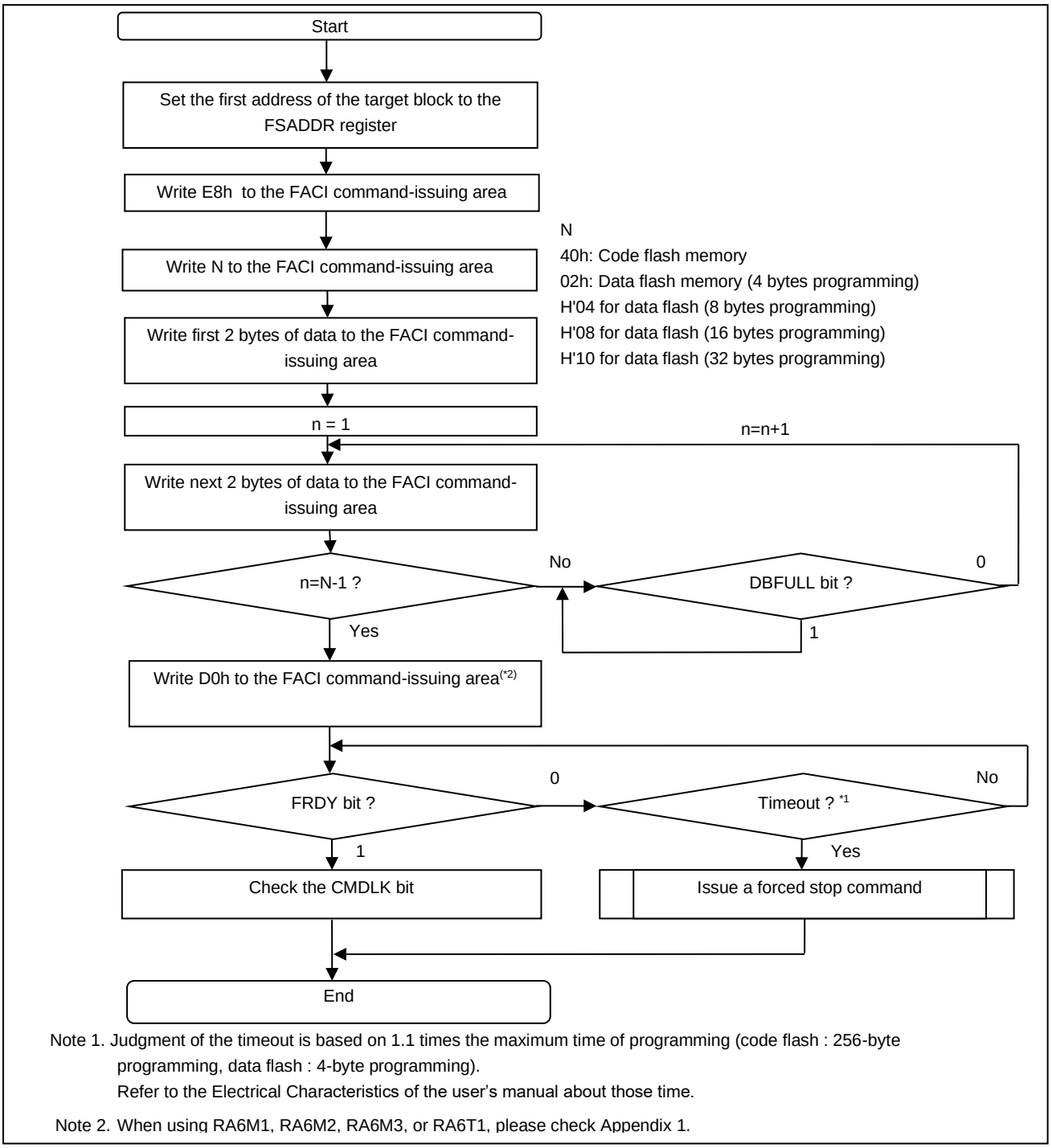
A program command is used for writing to the user area and data area.

Before issuing a program command, set the first address of the target block in the FSADDR register.

Writing D0h to the FACI command-issuing area at the final access of the FACI command-issuing starts the program command processing. If the target area of program command processing contains the area not for writing, write FFFFh to the corresponding area.

Issuing a program command while the FACI internal data buffer is full leads to a wait on the peripheral bus, and this may affect the communications performance of other peripheral IP modules. To avoid the generation of a wait in this way, the DBFULL bit in the FSTATR register should be 0 when an FACI command is issued.

Writing to the data area will not lead to the data buffer becoming full.



Note 1. Judgment of the timeout is based on 1.1 times the maximum time of programming (code flash : 256-byte programming, data flash : 4-byte programming).
Refer to the Electrical Characteristics of the user's manual about those time.

Note 2. When using RA6M1, RA6M2, RA6M3, or RA6T1, please check Appendix 1.

Figure 36. Usage of the Program Command

2.6.3.8 Erase1 Command

"Erase1" command is used for erasing user area or data area. Erase unit is one sector.

Before issuing “Erase1” command, set the first address of target sector to FSADRR register. Writing "H'D0" at 2nd write access of flash sequencer command triggers FACI to start “Erase1” command processing. Completion of command processing can be confirmed by FRDY bit of FSTATR register.

FCPSR registers should be set before issuing "Erase1" command. FCPSR needs to be set when erasure-suspended mode is required to be switched.

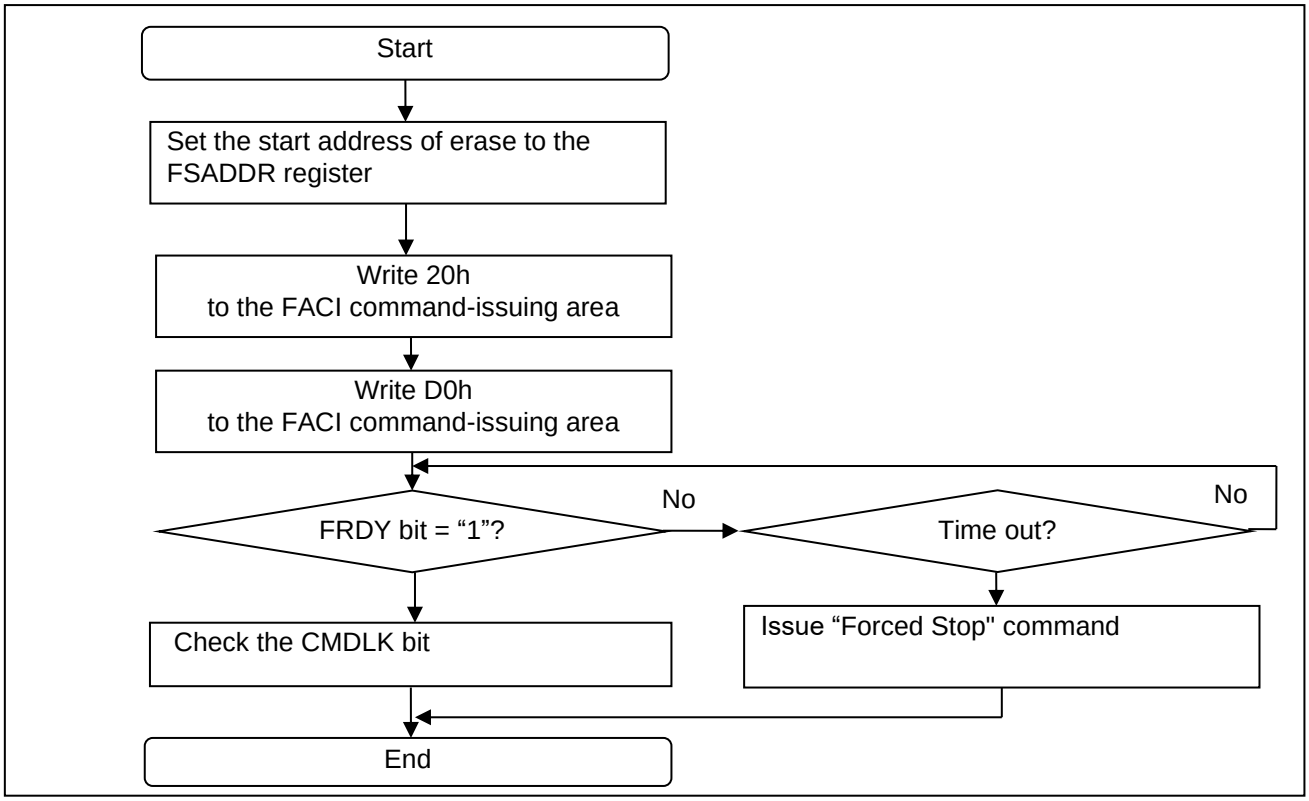


Figure 37. Usage of the Erase1 Command

2.6.3.9 Erase2 Command

"Erase2" command is used for erasing data area. Erase unit is 64, 128 or 256 byte.

Before issuing “Erase2” command, set the start address to FSADRR register and the end address to FEADDR register. Writing "H'D0" at 2nd write access of flash sequencer command triggers FACI to start “Erase2” command processing. Completion of command processing can be confirmed by FRDY bit of FSTATR register.

FCPSR registers should be set before issuing "Erase2" command. FCPSR needs to be set when erasure-suspended mode is required to be switched.

Erase size is specified by both the FSADDR and the FEADDR setting.

The following describes how to set the FSADDR and the FEADDR.

Table 18. Erase Size Setting

Erase Size	FSADDR	FEADDR
64 Byte	FSA0~FSA5 = 0 (64-byte Boundary)	FSADDR + H’3C
128 Byte	FSA0~FSA6 = 0 (128-byte Boundary)	FSADDR + H’7C
256 Byte	FSA0~FSA7 = 0 (256-byte Boundary)	FSADDR + H’FC

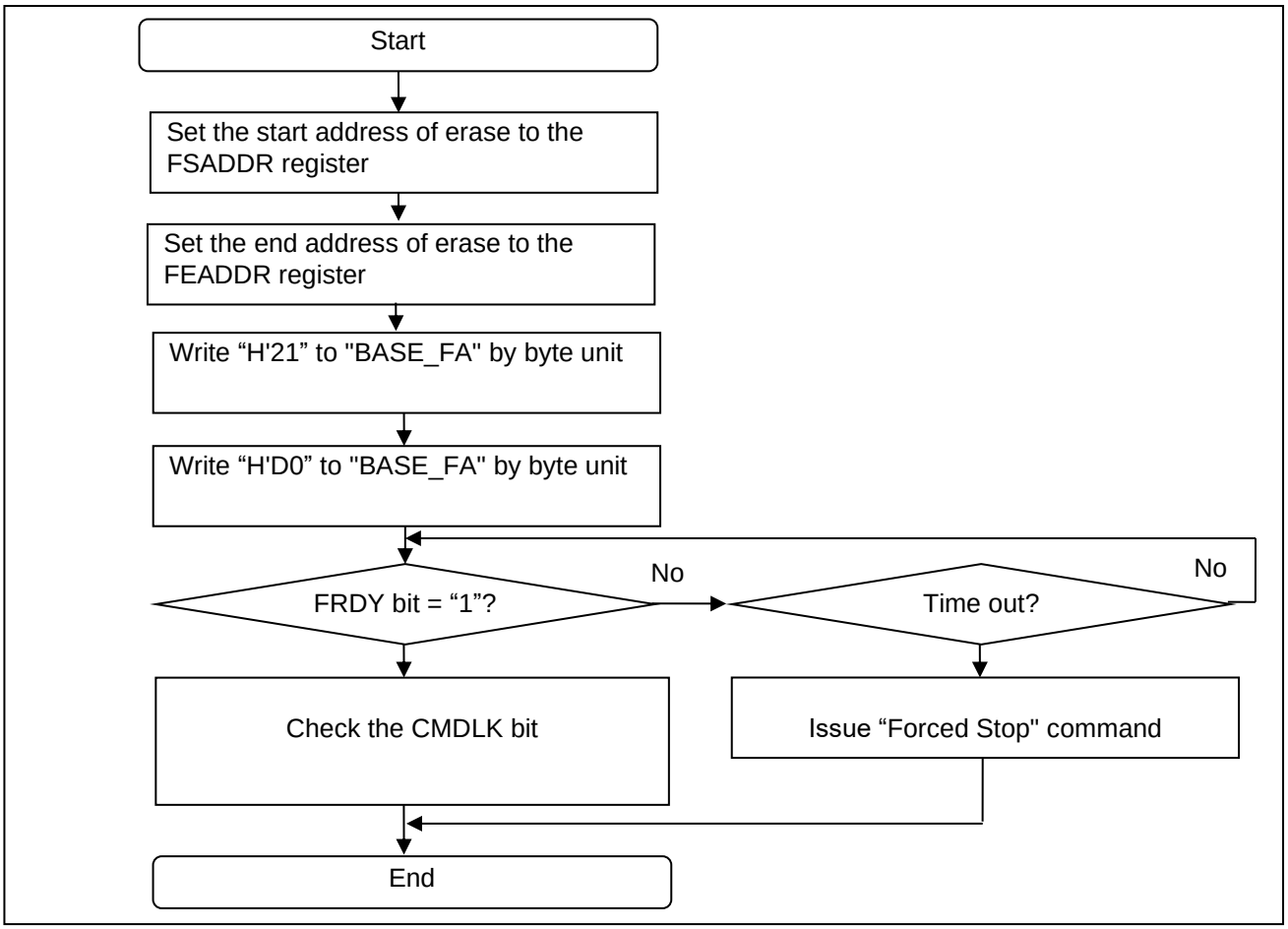


Figure 38. Usage of the Erase2 Command

2.6.3.10 P/E Suspend Command

To suspend programming/erasure, use the P/E suspend command.

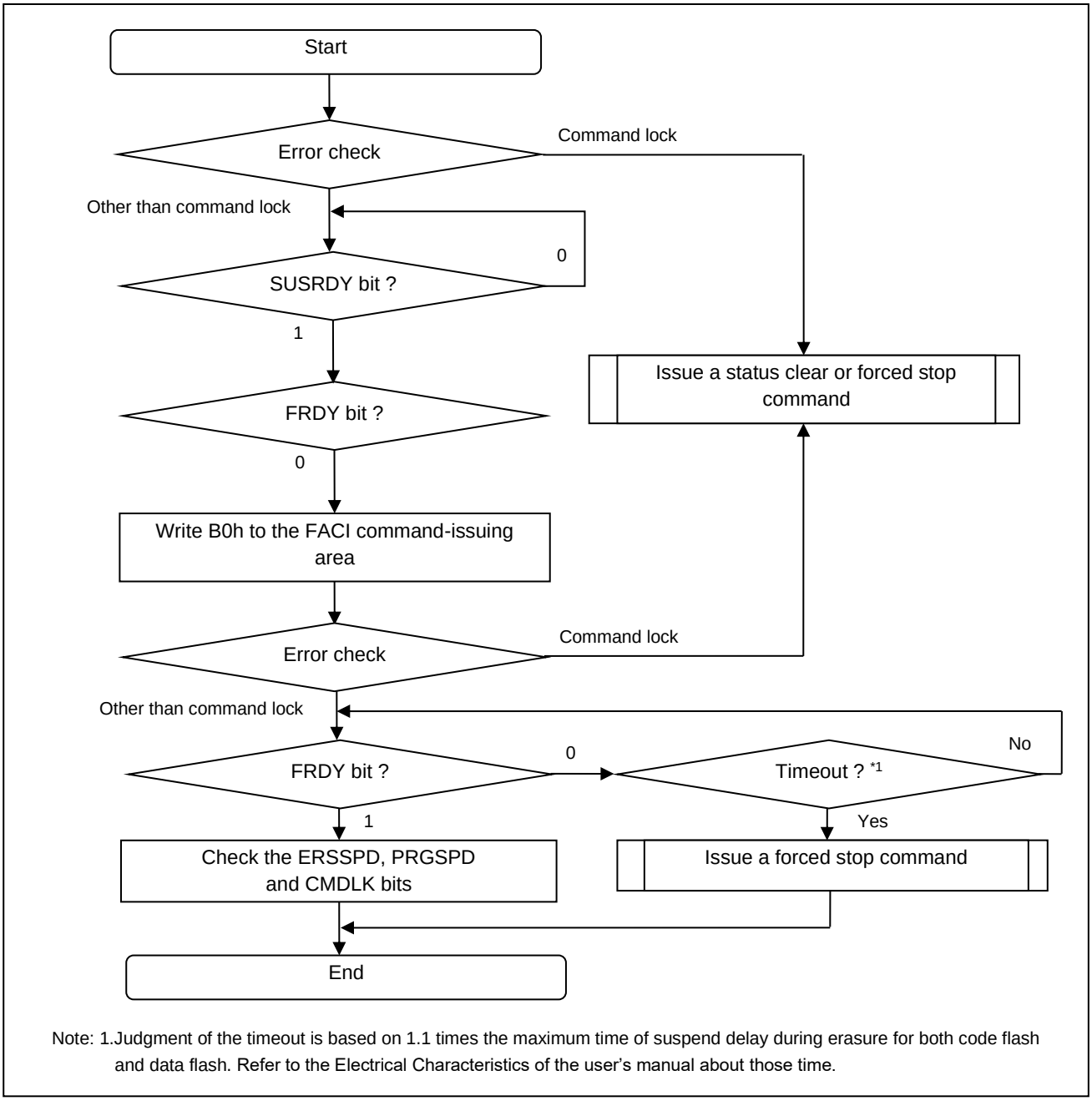
Before issuing a P/E suspend command, check that the CMDLK bit in the FSASTAT register is 0, and the execution of programming/erasure is normally performed. To confirm that the P/E suspend command can be received, also check that the SUSRDY bit in the FSTATR register is 1. After issuing a P/E suspend command, read the CMDLK bit to confirm that no error occurs.

If an error occurs during programming/erasure, the CMDLK bit is set to 1. When programming/erasure processing has finished during the interval from when the SUSRDY bit is checked as 1 to when a P/E suspend command is received, no error occurs and the suspended state is not entered (the FRDY bit in the FSTATR register is 1 and the ERSSPD and PRGSPD bits in FSTATR are 0).

When a P/E suspend command is received and then the programming/erasure suspend processing finishes normally, the flash sequencer enters the suspended state, the FRDY bit is set to 1, and the ERSSPD or PRGSPD bit is 1. After issuing a P/E suspend command, check that the ERSSPD or PRGSPD bit is 1 and the suspended state is entered, and then decide the subsequent flow. If a P/E resume command is issued in the subsequent flow although the suspended state is not entered, an illegal command error occurs and the flash sequencer shifts to the command-locked state (see section 2.8.2, Error Protection).

If the erasure suspended state is entered, programming to blocks other than an erasure target can be performed.

Additionally, the programming and erasure suspended states can shift to read mode by clearing the FENTRYR register.



Note: 1.Judgment of the timeout is based on 1.1 times the maximum time of suspend delay during erasure for both code flash and data flash. Refer to the Electrical Characteristics of the user's manual about those time.

Figure 39. Usage of the P/E Suspend Command

(1) Suspension during Programming

When issuing a P/E suspend command during the flash memory programming, the flash sequencer suspends programming processing. Figure 40 shows the suspend operation of programming. When receiving a programming-related command, the flash sequencer clears the FRDY bit in the FSTATR register to 0 to start programming. If the flash sequencer enters the state in which the P/E suspend command can be received after starting programming, it sets the SUSRDY bit in the FSTATR register to 1. When a P/E suspend command is issued, the flash sequencer receives the command and clears the SUSRDY bit to 0. If the flash sequencer receives a P/E suspend command while a programming pulse is being applied, the flash sequencer continues applying the pulse. After the specified pulse application time, the flash sequencer finishes pulse application, and starts the programming suspend processing and sets the PRGSPD bit in the FSTATR register to 1.

When a suspended processing finishes, the flash sequencer sets the FRDY bit to 1 to enter the programming suspended state. When receiving a P/E resume command in the programming suspended state, the flash sequencer clears the FRDY and PRGSPD bits to 0 and resumes programming.

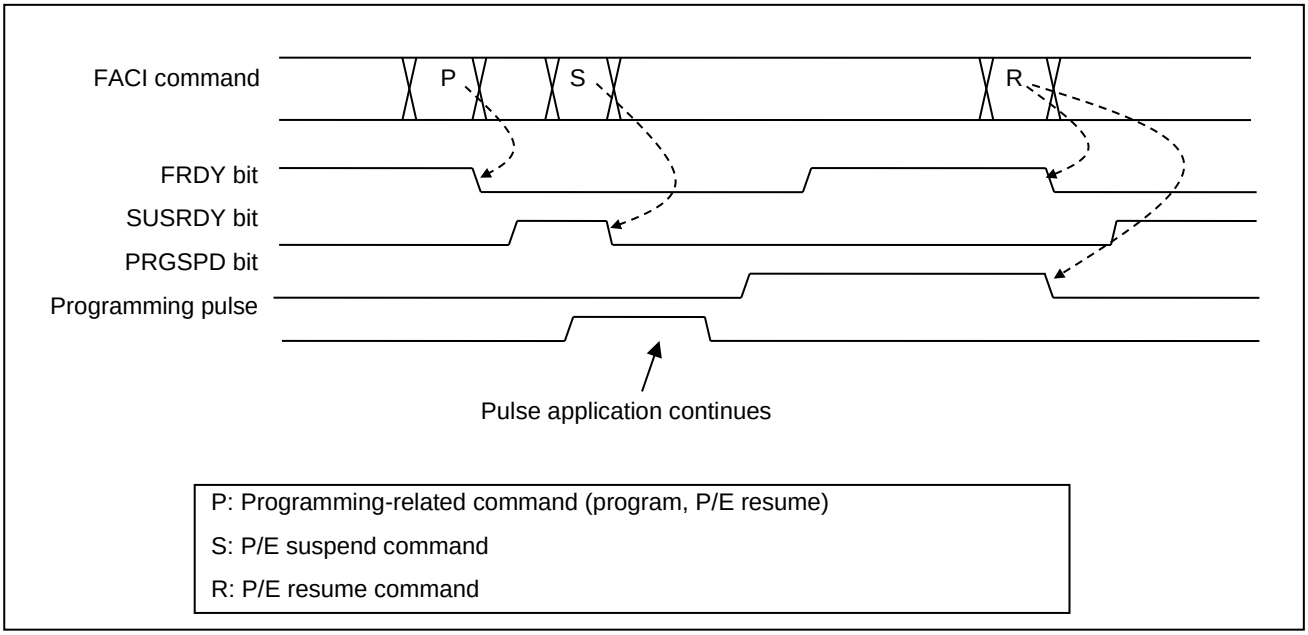


Figure 40. Suspension during Programming

(2) Suspension during Erasure (Suspension Priority Mode)

This flash sequencer has a suspension priority mode for the suspension of erasure. Figure 41 shows the suspend operation of erasure when the erasure suspend mode is set to the suspension priority mode (the ESUSPMD bit in the FCPSR register is 0).

When receiving an erasure-related command, the flash sequencer clears the FRDY bit in the FSTATR register to 0 to start erasure. If the flash sequencer enters the state in which the P/E suspend command can be received after starting erasure, it sets the SUSRDY bit in the FSTATR register to 1. When a P/E suspend command is issued, the flash sequencer receives the command and clears the SUSRDY bit to 0. When receiving a suspend command during erasure, the flash sequencer starts the suspend processing and sets the ERSSPD bit in the FSTATR register to 1 even if it is applying an erasure pulse. When the suspended processing finishes, the flash sequencer sets the FRDY bit to 1 to enter the erasure suspended state. When receiving a P/E resume command in the erasure suspended state, the flash sequencer clears the FRDY and ERSSPD bits to 0 and resumes erasure. Operations of the FRDY, SUSRDY, and ERSSPD bits at the suspension and resumption of erasure are the same, regardless of the erasure suspend mode.

The setting of the erasure-suspend mode affects the control method of erasure pulses. In suspension priority mode, when receiving a P/E suspend command while erasure pulse A that has never been suspended in the past is being applied, the flash sequencer suspends the application of erasure pulse A and enters the erasure suspended state. When receiving a P/E suspend command while reapplying erasure pulse A after erasure is resumed by a P/E resume command, the flash sequencer continues applying erasure pulse A. After the specified pulse application time, the flash sequencer finishes erasure pulse application and enters the erasure suspended state. When the flash sequencer receives a P/E resume command next and erasure pulse B starts to be newly applied, and then the flash sequencer receives a P/E suspend command again, the application of erasure pulse B is suspended. In suspension priority mode, delay due to suspension can be minimized because the application of an erasure pulse is suspended one time per pulse and priority is given to the suspend processing.

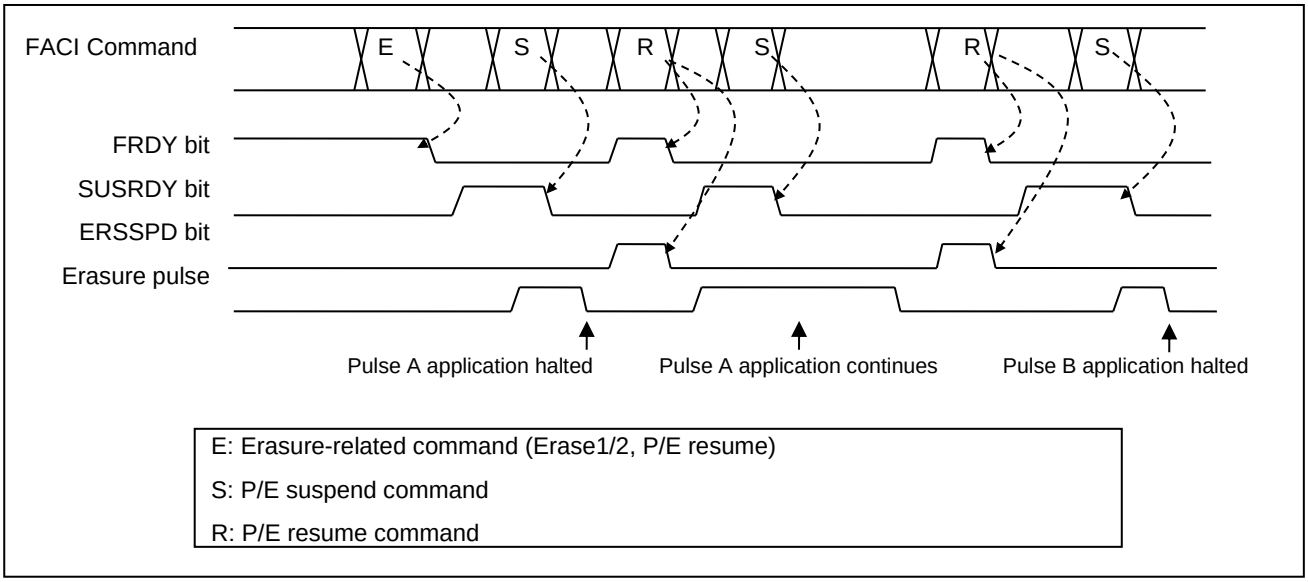


Figure 41. Suspension during Erasure (Suspension Priority Mode)

(3) Suspension during Erasure (Erasure Priority Mode)

This flash sequencer has an erasure priority mode for the suspension of erasure.

Figure 42 shows the suspend operation of erasure when the erasure suspend mode is set to the erasure priority mode (the ESUSPMD bit in the FCPSR register is 1). The control method of erasure pulses in erasure priority mode is the same as that of programming pulses for the programming suspend processing.

If the flash sequencer receives a P/E suspend command while an erasure pulse is being applied, the flash sequencer definitely continues applying the pulse. In this mode, the required time for the whole erasure processing can be reduced as compared with the suspension priority mode because the reapplication of erasure pulses does not occur when a P/E resume command is issued.

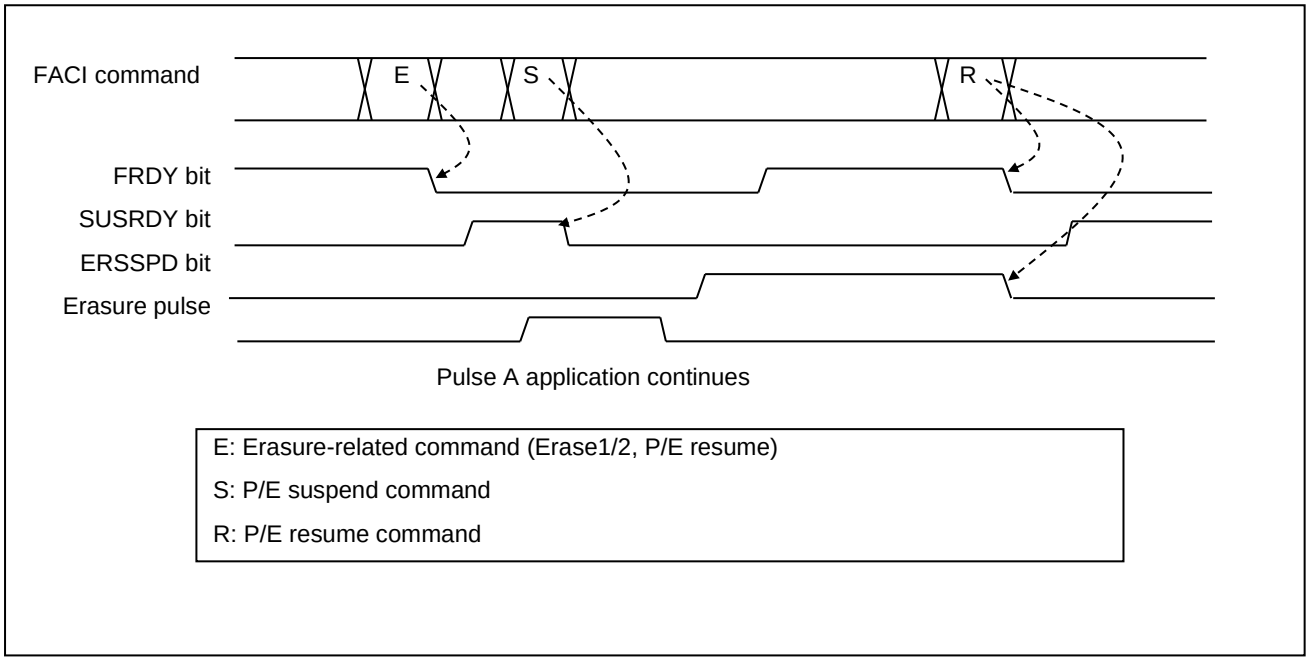


Figure 42. Suspension during Erasure (Erasure Priority Mode)

2.6.3.11 P/E Resume Command

To resume suspended programming or erasure, use the P/E resume command. When the settings of the FENTRYR register are changed during suspension, reset FENTRYR to the value immediately before the P/E suspend command was issued, and then issue a P/E resume command.

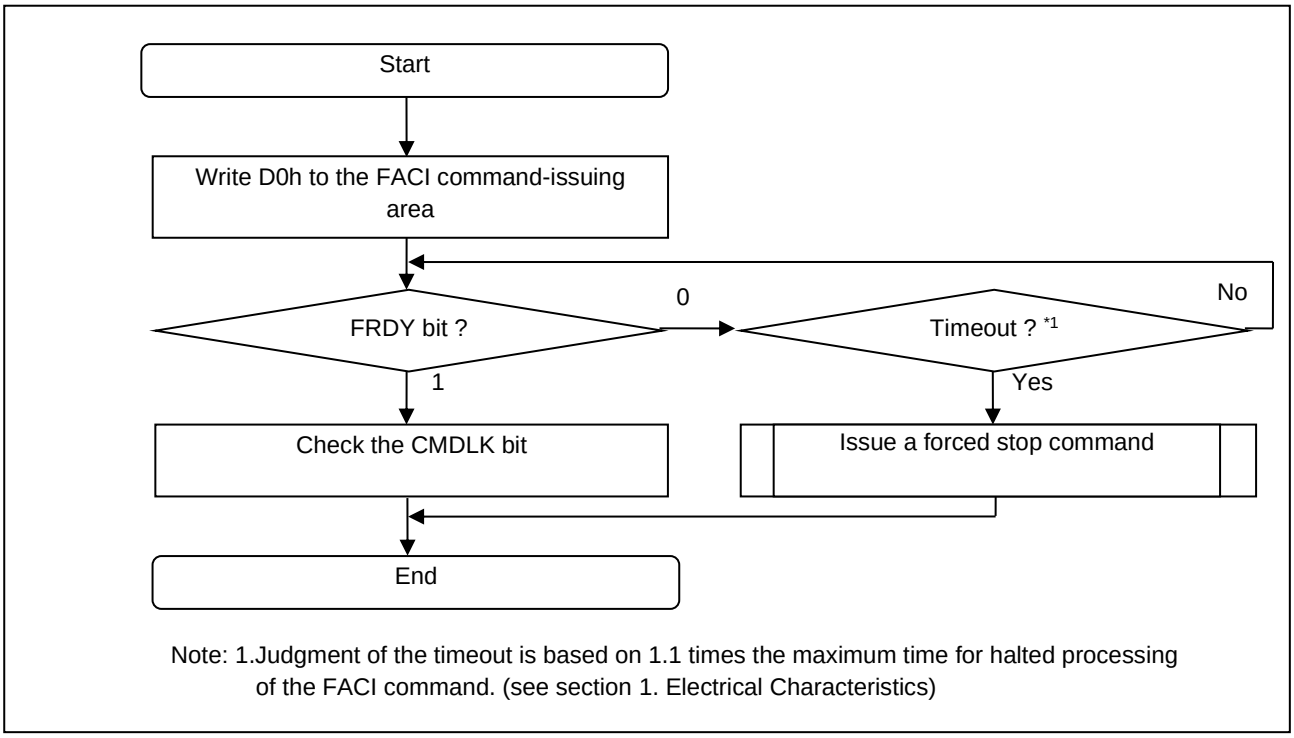


Figure 43. Usage of the P/E Resume Command

2.6.3.12 Status Clear Command

The status clear command is used to clear the command-locked state. To clear the ILGLERR, ERSERR, and PRGERR bits in the FSTATR register in the command-locked state, the status clear command is available.

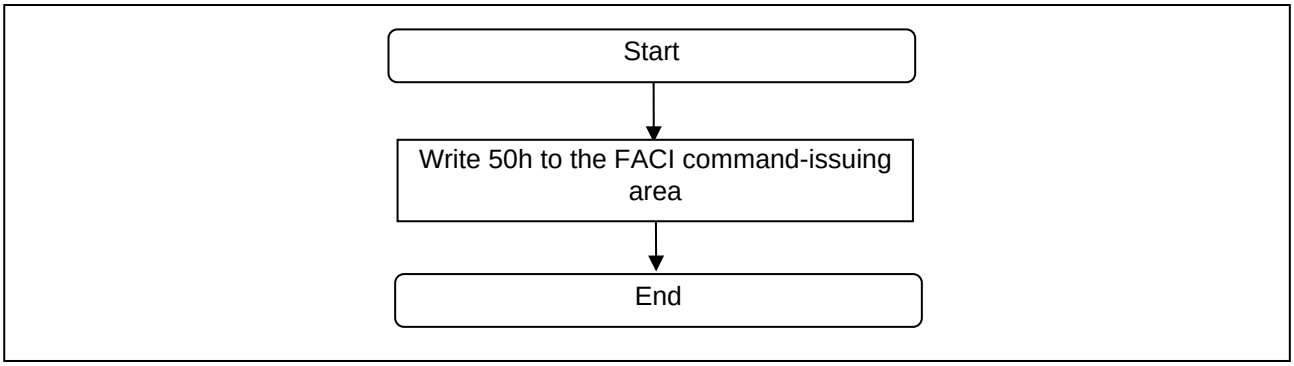


Figure 44. Usage of the Status Clear Command

2.6.3.13 Forced Stop Command

The forced stop command forcibly ends command processing by the flash sequencer. Although this command halts command processing more quickly than the P/E suspension command, values from the programming or erasure that was in progress are not guaranteed. Furthermore, resumption of processing is not possible. Processing of programming or erasure that was halted by the forced stop command is also defined as one round of programming (one “time”).

Executing a forced stop command also initializes part of the FACI, the whole FCU, and the FSTATR. Accordingly, this command can be used in the procedure for recovery from the command-locked state and in processing in response to a time-out of the flash sequencer.

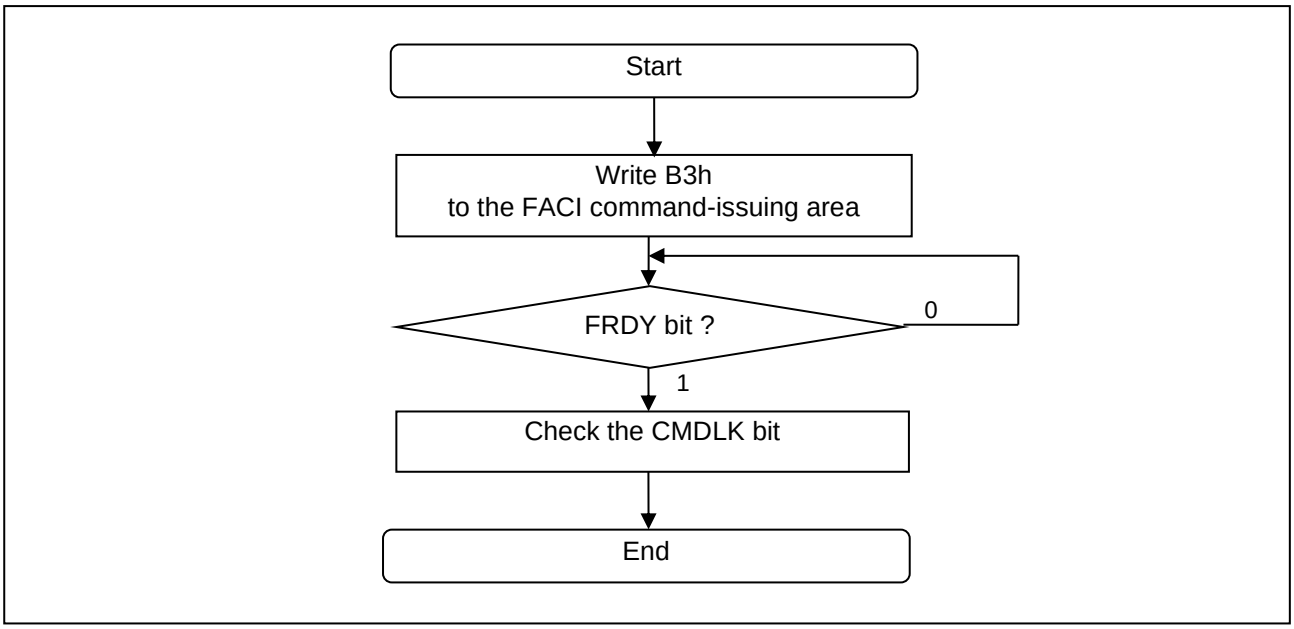


Figure 45. Usage of the Forced Stop Command

2.6.3.14 Blank Check Command

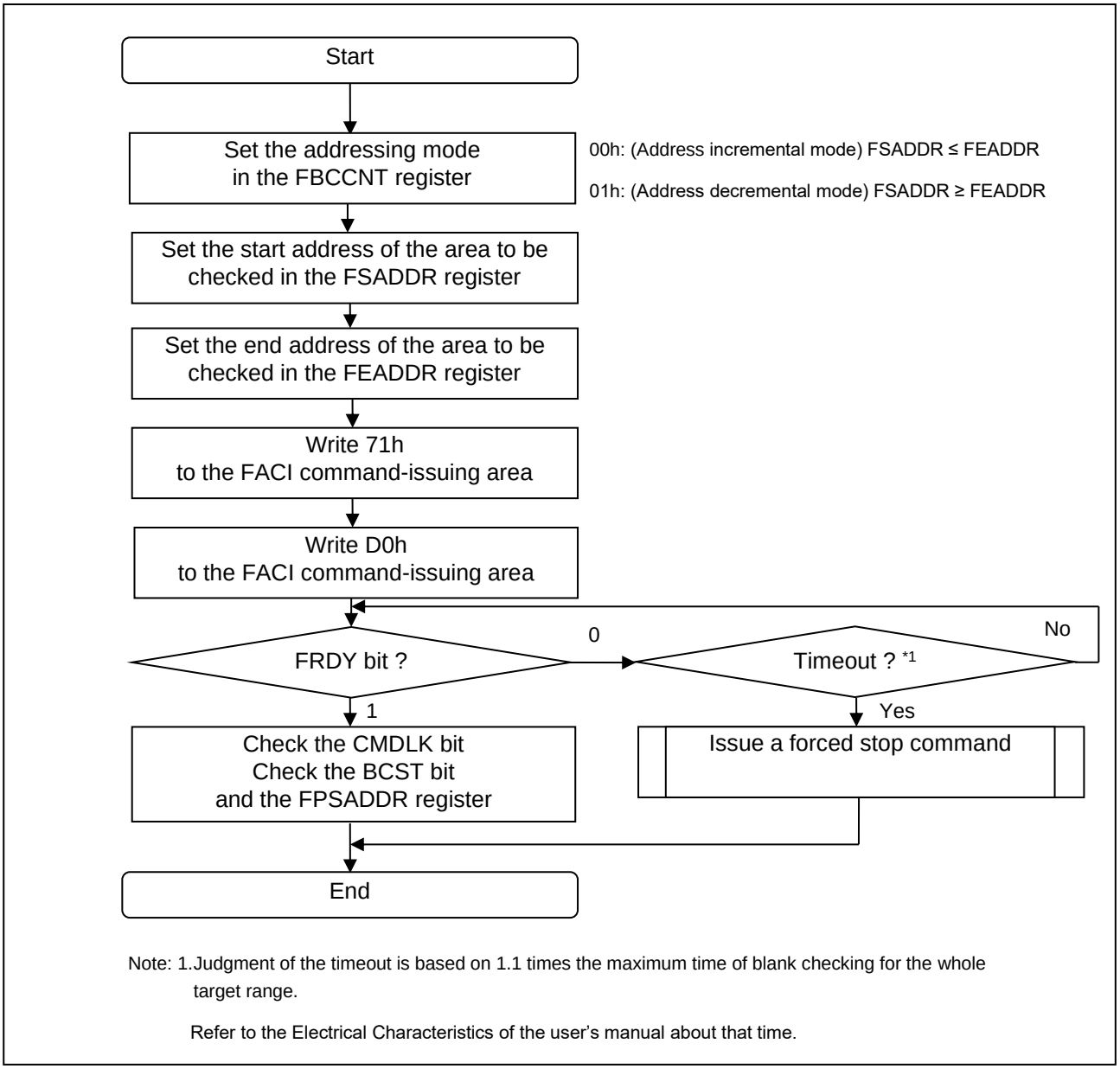
Values read from data flash memory that has been erased but not yet been programming again (that is, in the non-programmed state) are undefined. Use the blank check command when you need to confirm that an area is in the non-programmed state.

Before issuing a blank check command, set addressing mode, start address, and end address of the target area for blank checking to the FBCCNT, FSADDR, and FEADDR registers. When blank checking addressing mode is set to decremental mode (that is, FBCCNT.BCDIR = 1), address specified in FSADDR should be larger than address in FEADDR.

Conversely, address in FSADDR should be smaller than address in FEADDR when blank check addressing mode is set to incremental mode (that is, FBCCNT.BCDIR = 0).

If the settings of the BCDIR bit, FSADDR, and FEADDR are inconsistent, the flash sequencer enters the command-locked state. The size of the target area for blank checking is in the range from 4 bytes to 64 KB and is set in units of 4 bytes.

Write 71h and D0h to the FACI command-issuing area to start blank checking. Completion of processing can be confirmed by the FRDY bit of the FSTATR register. At the end of processing, the result of blank checking is stored in the BCST bit in the FBCSTAT register. If the target area for blank checking includes areas where programming has been completed, the flash sequencer stores the address of the first such area it detects in the FPSADDR register.



Note: 1.Judgment of the timeout is based on 1.1 times the maximum time of blank checking for the whole target range.

Refer to the Electrical Characteristics of the user's manual about that time.

Figure 46. Usage of the Blank Check Command

2.6.3.15 Configuration Set Command

The configuration set command is used to set the ID, security function, safety function. Before issuing a configuration set command, set the specified address in the FSADDR register. Writing D0h to the FACI command-issuing area in the final access for issuing the FACI command starts FACI processing of the configuration set command.

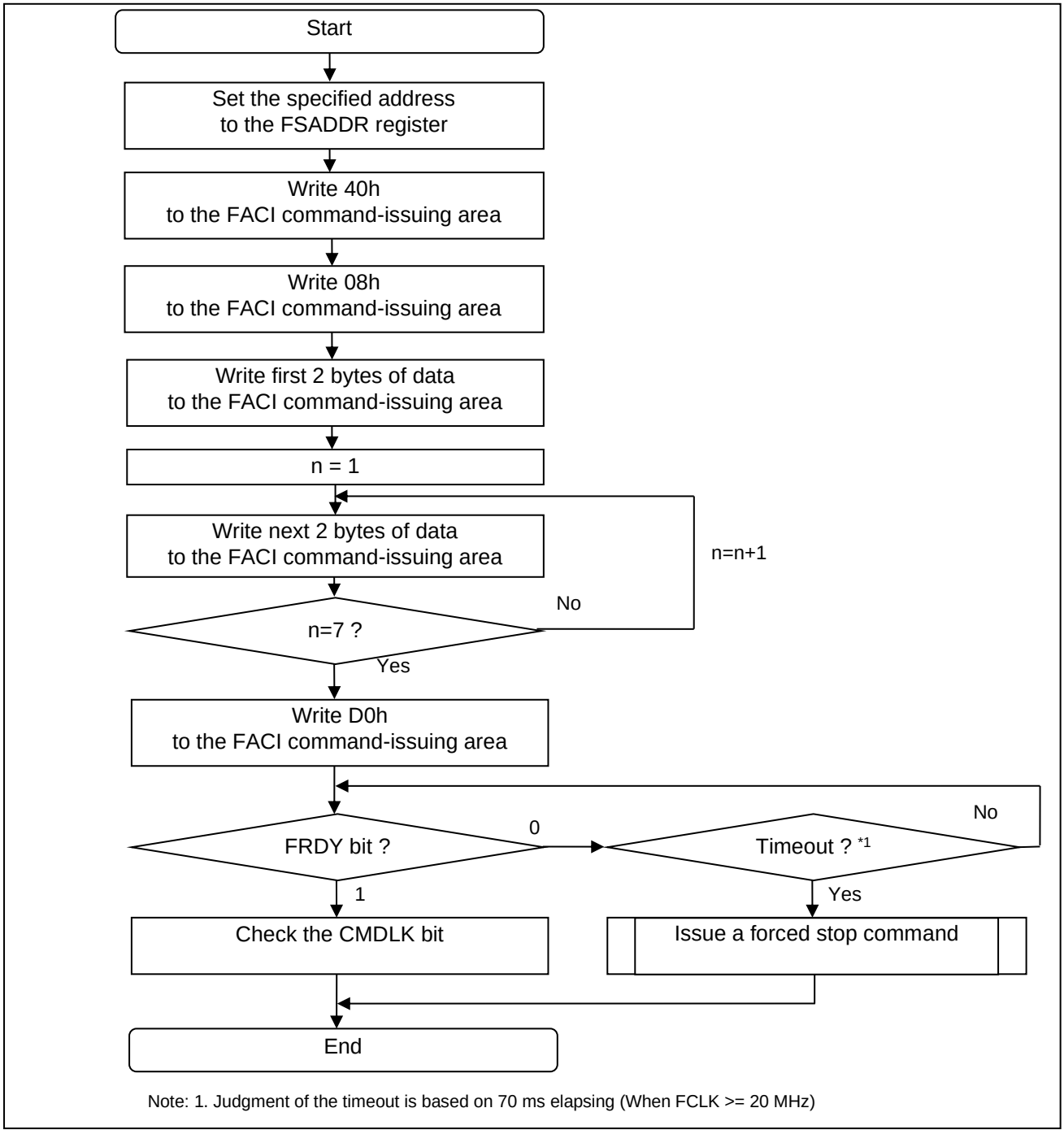


Figure 47. Usage of the Configuration Set Command

The correspondence between the possible target data for configuration setting and the address value set in the FSADDR register is shown in section 2.4.5. Data in other areas can be changed to any value each time the configuration set command is executed.

Table 19. Address Used by Configuration Set Command

Address	Setting Data
0000 A150h	ID for authentication.
0000 A160h	Access Window setting, Start-up Area Select Flag(BTFLG) setting, FSPR bit setting.

Following describes the data setting (configuration bit mapping) for ID.

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
WD1	ID4 [7:0]								ID3 [7:0]							
WD3	ID8 [7:0]								ID7 [7:0]							
WD5	ID12 [7:0]								ID11 [7:0]							
WD7	ID16 [7:0]								ID15 [7:0]							

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
WD0	ID2[7:0]								ID1[7:0]							
WD2	ID6[7:0]								ID5[7:0]							
WD4	ID10[7:0]								ID9[7:0]							
WD6	ID14[7:0]								ID13[7:0]							

Following describes the data setting (configuration bit mapping) to the address of the Access Window and Start-up Area Select Flag.

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
WD1																
WD3	BTFLG					FAWE [10:0]										
WD5																
WD7																

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
WD0																
WD2	FSPR					FAWS [10:0]										
WD4																
WD6																

FSPR, FAWE [10:0], FAWS [10:0], BTFLG bits are capable for setting at the self-programming mode, the serial programming mode and on chip debugger mode.

Once FSPR bit is set to 0, it cannot be changed to 1. It is impossible to push back the not protected state.

The state of FSPR, FAWE [10:0], FAWS [10:0], BTFLG bits can be checked by the FAWMON register.

Note that it please set the current data to the no-updating bits.

Following describes the configuration set command execution only when the set address is “0000_A160h”.

- FSPR bit in the configuration area is “1”.

When the FSPR bit is “0”, issuing the configuration set command at “0000_A160h” address causes to be a command lock state.

Figure 48 shows the configuration area bit map. The boot program must use these bits as hexadecimal data.

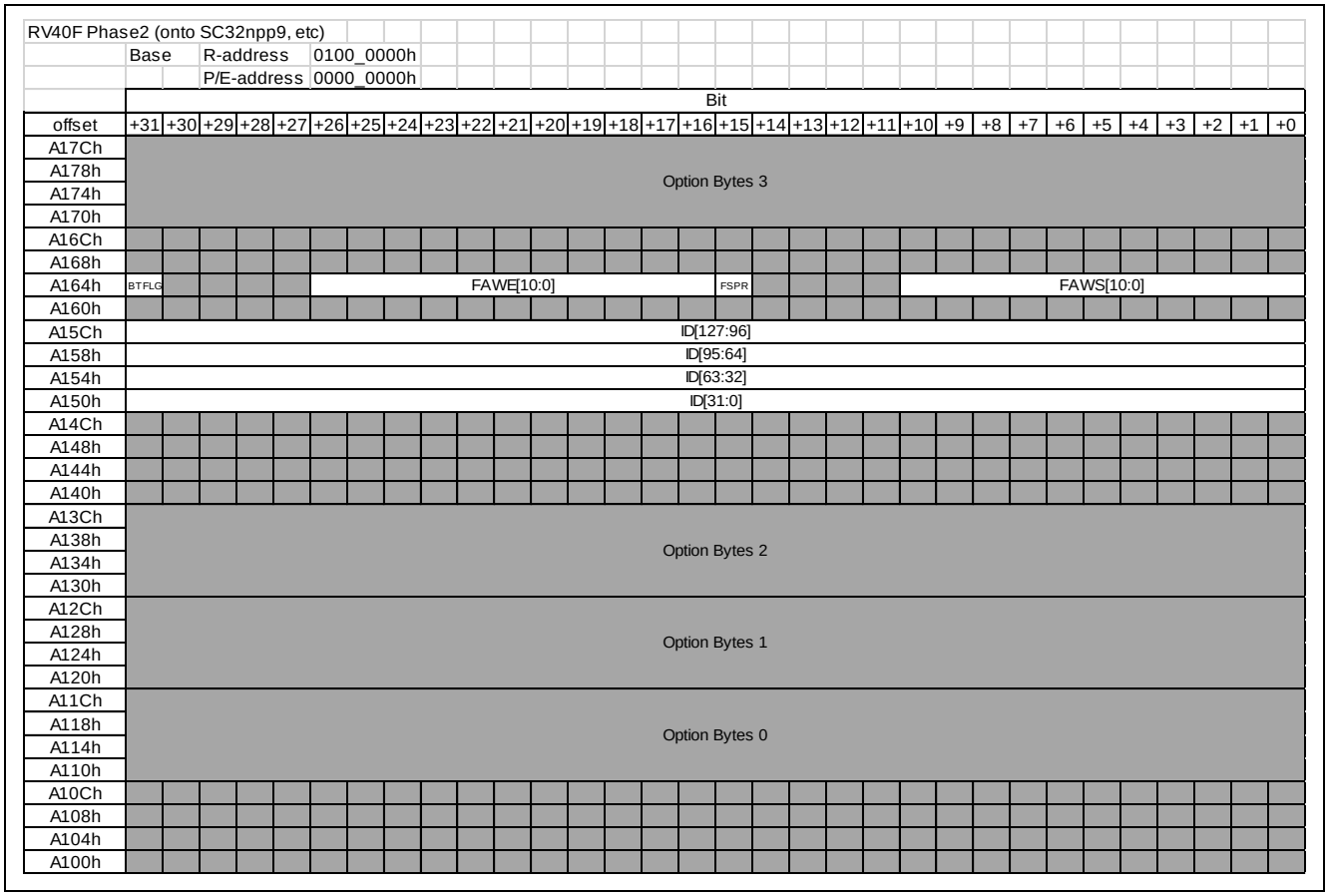


Figure 48. Configuration Area Bit Map

2.7 Security Function

FACI supports following security functions.

- Serial Programming Mode Protection
- Security flag for Access Window / Start-Up Area

2.7.1 Serial Programming Mode Protection

The serial programming mode features the ID authentication.

FACI protects the reception of all flash sequencer commands according to the ID authentication result. When the ID authentication is enabled and passed, FACI validates flash sequencer commands.

2.7.2 Security Flag for Access Window / Start-Up Area

The security flag (FSPR) for the access window and the start-up area is located in the configuration area.

When the FSPR bit is 0, issuing the configuration set command to change the access window or the BTFLG bit causes to be the command-locked state. Also, when the FSPR bit is 0, it is impossible to write the start-up area select bits (SAS [1:0]) in the FSUAC register. The FSPR bit gives the protection in the self-programing mode, the serial programming mode and the OCD mode.

2.8 Safety Function

2.8.1 Software Protection

Software protection disables programming and erasure for the code flash memory through the settings of control registers and access window setting in the user area. If an attempt is made to issue an FACI command against software protection, the flash sequencer enters the command-locked state.

2.8.1.1 Protection through FWEPROR

Unless the FWEPROR.FLWE[1:0] bits are set to 01b, programming cannot proceed in any mode.

2.8.1.2 Protection by FENTRYR

When the FENTRYR register is set to 0000h, the flash sequencer enters read mode. In read mode, FACI commands cannot be accepted. If an attempt is made to issue an FACI command in read mode, the flash sequencer enters the command-locked state.

2.8.1.3 Protection by Access Window

Issuing the program or Erase1 command to the area without the access window causes to be the command-locked state. The access window is only valid at the user mat of FLI. The access window gives the protection in the self-programing mode, the serial programming mode and the OCD mode.

The access window is specified by both the FAWS bits and the FAWE bits.

The following describes how to set the FAWS bits and the FAWE bits.

FAWE = FAWS : the P/E command is allowed to execute at all the user area of FLI.

FAWE > FAWS : the P/E command is only allowed to execute into window from the block pointed by the FAWS bits to the block one lower than block pointed by FAWE bits.

FSWE < FAWS : the P/E command is not allowed to execute at all the user area of FLI.

Example

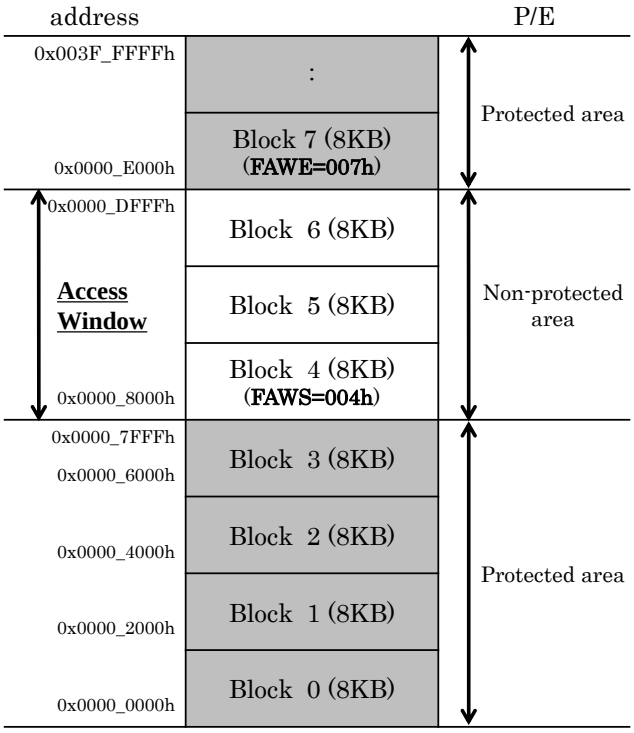


Figure 49. Start Block Address (FAWS) and End Block Address (FAWE) of the Access Window (the access window includes the only block size of 8 KB)

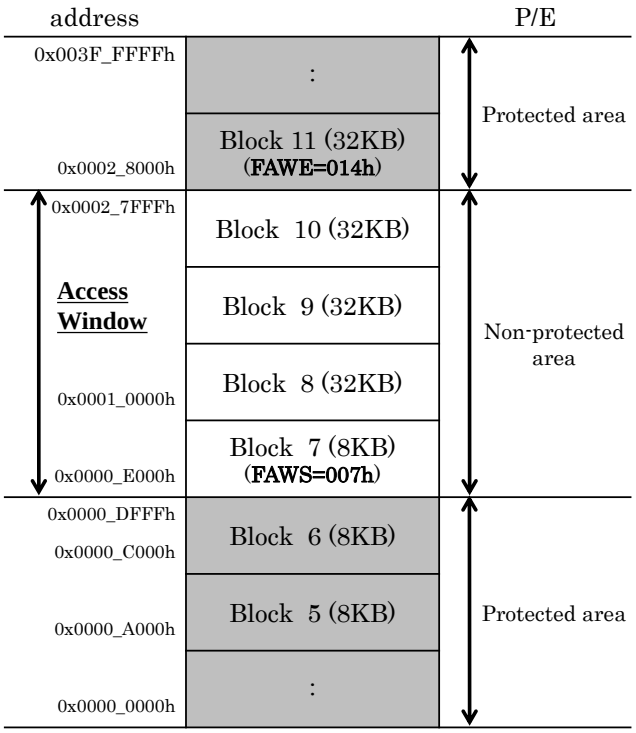


Figure 50. Start Block Address (FAWS) and End Block Address (FAWE) of the Access Window (the access window includes the block size of 8 KB and 32 KB)

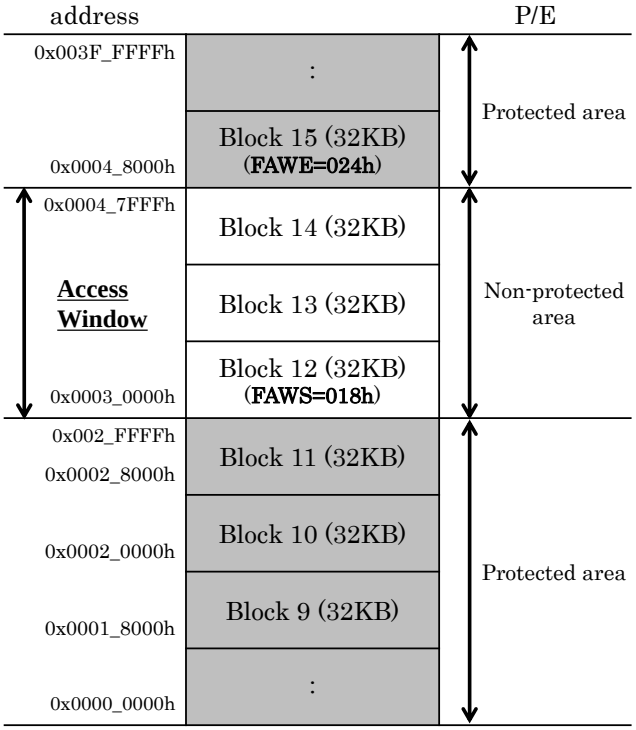


Figure 51. Start Block Address (FAWS) and End Block Address (FAWE) of the Access Window (the access window includes the only block size of 32 KB)

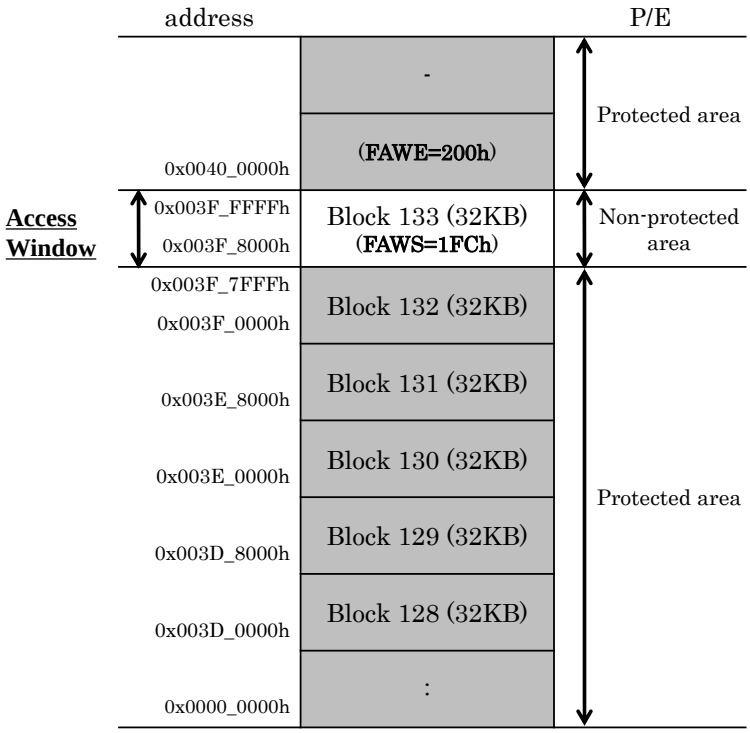


Figure 52. Start Block Address (FAWS) and End Block Address (FAWE) of the Access Window (the access window includes the only final block)

(1) Area Set for Access Window

The area data for the access window is located in the configuration area.

Symbol	Bit Name	Description
FAWE [10:0]	End Block Address of Access Window	These bits do not represent the block number of the access window. The access window is only valid at the user mat of FLI. The end block address for the access window is the next block to the P/E acceptable region defined by the access window. The block address means the first address of the block and consists of the address bits from 13 to 23 ([23:13]). Therefore, when the block is in the 32 KB area, the FAWE [1:0] is “00”.
FAWS [10:0]	Start Block Address of Access Window	These bits do not represent the block number of the access window. The access window is only valid at the user mat of FLI. The block address means the first address of the block and consists of the address bits from 13 to 23 ([23:13]). Therefore, when the block is in the 32 KB area, the FAWS [1:0] is “00”.

2.8.2 Error Protection

Error protection detects the issuing of illegal FACI commands, illegal access, and flash sequencer malfunction. FACI command acceptance is disabled (command-locked state) in response to the detection of these errors. The flash memory cannot be programmed or erased while the flash sequencer is in the command-locked state. For release from the command-locked state, issue a status clear or forced stop command while the CFAE and DFAE bits in the FASTAT register are 0. The status clear command can only be used while the FRDY bit in the FSTATR register is 1. The forced stop command can be used regardless of the value of the FRDY bit. While the CMDLKIE bit in the FAEINT register is 1, a flash access error (FIFERR) interrupt is generated if the flash sequencer enters the command-locked state (the CMDLK bit in the FASTAT register is set to 1).

If the flash sequencer enters the command-locked state in response to a command other than the P/E suspend command during programming or erasure processing, the flash sequencer continues the processing for programming or erasure. In this state, the P/E suspend command cannot be used to suspend the processing for programming or erasure. If a command is issued in the command-locked state, the ILGLERR bit becomes 1 and the other bits retain the values set due to previous error detection.

Table 20 shows error protection types and status bit values after error detection.

Table 20. Error Protection Type

Error Type	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
FENTRYR setting error	The FENTRYR setting is 0081h.	0	1	0	0	1	0	0	0	0	0
	The FENTRYR setting at suspension disagrees with that at resumption.	0	1	0	0	1	0	0	0	0	0
Illegal command error	An undefined size has been specified in the first cycle of command. (Not Byte write)	1	0	0	0	1	0	0	0	0	0
	An undefined code is written in the first access of an FACI command.	1	0	0	0	1	0	0	0	0	0
	The value specified in the last access of the multiple-access FACI command is not D0h.	1	0	0	0	1	0	0	0	0	0
	The value (N) specified in the second write access of an FACI command in the program or configuration set command is wrong.	1	0	0	0	1	0	0	0	0	0
	“Blank check” command has been issued with inconsistent BCDIR, FSADDR, and FEADDR settings (see section 2.4.6, FACI Command End Address Register (FEADDR)).	1	0	0	0	1	0	0	0	0	0/1 *2
	"Erase2" command has been issued with inconsistent FSADDR and FEADDR settings. 1. FSADDR > FEADDR 2. FEADDR is set to reserved data area or unmapped area.	1	0	0	0	1	0	0	0	0	0/1 *2
	An FACI command not acceptable in each mode has been issued (see Table 17).	1	0	0	0	1	0	0	0	0	0
	An FACI command has been issued when command acceptance conditions are not satisfied (see Table 18).	1	0	0	0	1	0/1	0/1	0/1	0/1	0/1

Error Type	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
	A program or a erase1 command has been issued against the area protected by the access window.	1	0	0	0	1	0	0	0	0	0
	A program command has been issued against the erase area in erase suspend.	1	0	0	0	1	0	0	0	0	0
Erase error	An error occurs during erasure.	0	0	0	0	0	1	0	0	0	0
Program error	An error occurs during programming.	0	0	0	0	0	0	1	0	0	0
Code flash access error	An FACI command has been issued to the reserved portion of the user area in code flash P/E mode (see section 2.4.2, Flash Access Status Register (FASTAT)).	0	0	0	0	1	0	0	0	1	0
Data flash access violation	“Program” or “Erase1” command has been issued to reserved data area or unmapped area in data flash P/E mode.	0	0	0	0	1	0	0	0	0	1
	“Erase2” command has been issued to reserved data area or unmapped area in data flash P/E mode. (FSADDR is set to reserved data area or unmapped area.)	1	0	0	0	1	0	0	0	0	1
	“Blank Check” command has been issued to reserved data area or unmapped area in data flash P/E mode. (FSADDR is set to reserved data area or unmapped area.)	1	0	0	0	1	0	0	0	0	1
Security error	Flash sequencer command has been issued when ID authentication was failed at the Serial Programming Mode.	0	0	1	0	1	0	0	0	0	0
	A configuration set command for the access window setting and the BTFLG bit setting has been issued when the FSPR bit is 0 (see section 2.6.3.15).	0	0	1	0	1	0	0	0	0	0
Others	The FACI command-issuing area has been accessed in read mode.	0	0	0	1	1	0	0	0	0	0
	The FACI command-issuing area has been read in code flash P/E mode or data flash P/E mode.	0	0	0	1	1	0	0	0	0	0
Flash write erase protection error	A flash memory write protection error has been detected by the setting of the FWEPROR register[*1] during command processing by the flash sequencer.	0	0	0	0	0	0/1	0/1	1	0	0

Note 1. For details on the FWEPROR register, see section 2.4.1, Flash P/E Protect Register (FWEPROR).
Note 2. DFAE value depend on FSADDR setting.

2.8.3 Boot Program Protection

2.8.3.1 Start-Up Area Select

The start-up area select function allows the customer to safely update the boot program. The size of the start-up area is 8K bytes, and the start-up area is located at the user area. FACI controls the address of the start-up area according to the start-up area select flag (BTFLG) that is located at the configuration area or the FSUAC register. The start-up area is allowed to be locked by the FSPR bit.

Reference: Figure 53

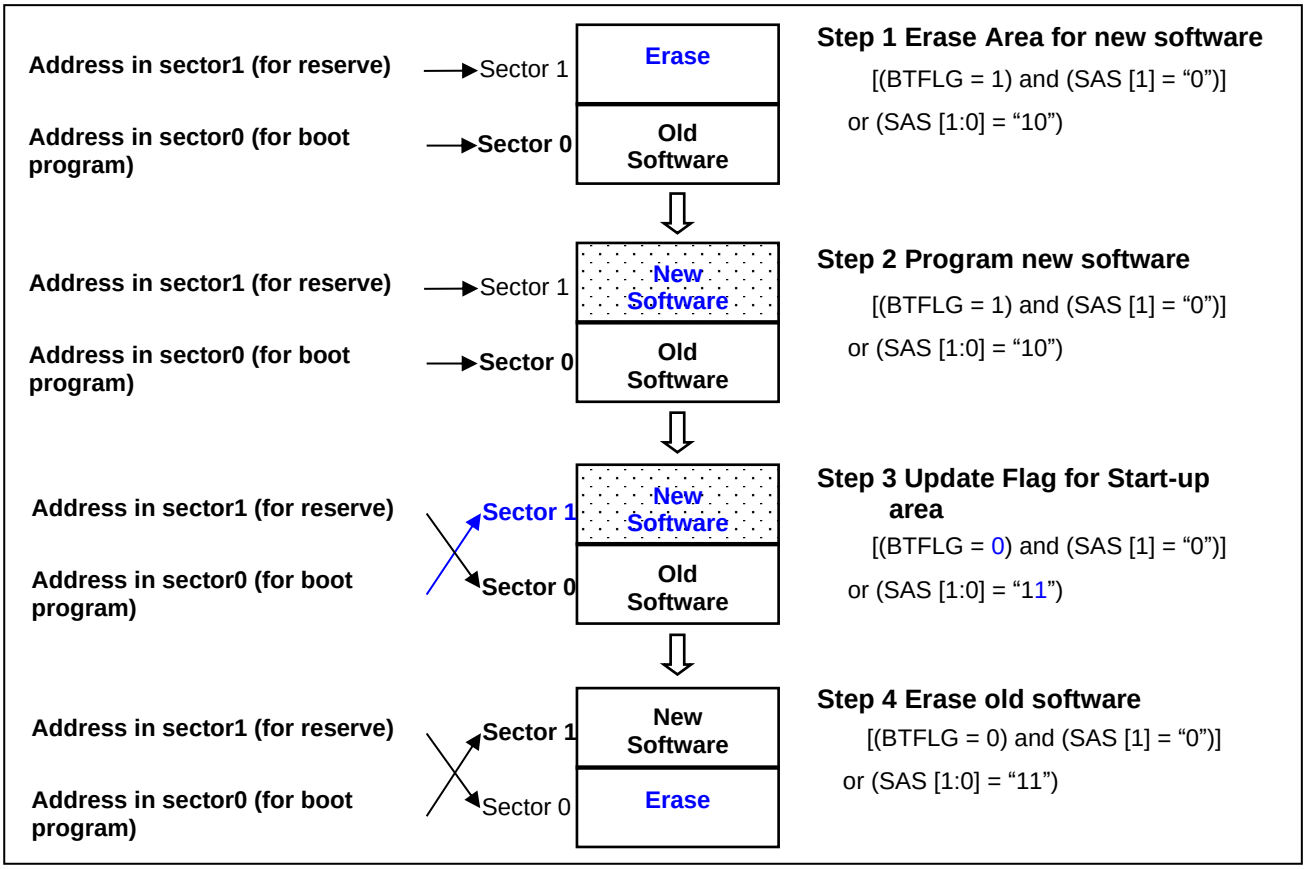


Figure 53. Start-up Area Update Procedure

(1) Set for Start-Up Area Select Flag

The flag for the start-up area select is located in the configuration area.

Symbol	Bit Name	Description
BTFLG	Flag of Start-Up Area Select for Boot Swap	This bit sets whether the address of the start-up area is exchanged or not. 0: The start-up area is the alternate area (block 1) 1: The start-up area is the default area (block 0)

2.9 Electrical Characteristics of FACI command

2.9.1 AC Characteristics

Conditions : VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, 2.7 ≤ VREFH/VREFH0 ≤ AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = AVSS_USBHS = VSS1_USBHS = VSS2_USBHS = PVSS_USBHS = 0 V, Ta = Topr

Item	Min.	Typ.	Max.	Unit	Conditions
FACI command setup time	-	-	100	us	FCLK=20 MHz
FACI command processing time	-	-	0	tFcyc *1	For other than programming of code flash memory
			90	tFcyc *1	For programming of code flash memory

Note: 1. tFcyc means the cycle of FCLK.

2.10 Usage Notes

2.10.1 Reading Areas Where Programming or Erasure was Interrupted

When programming or erasure of an area of flash memory is interrupted, the data stored in the area become undefined. To avoid undefined data that are read out becoming the source of faulty operation, take care not to fetch instructions or read data from areas where programming or erasure was interrupted.

2.10.2 Prohibition of Additional Writing

Writing to a given area twice is not possible. If you want to overwrite data in an area of flash memory after writing to the area has been completed, erase the area first.

2.10.3 Resets during Programming and Erasure

In the case of a reset due to the signal on the RES# pin during programming and erasure, wait for tRESW once the operating voltage is within the range stipulated in the electrical characteristics after assertion of the reset signal before releasing the device from the reset state.

2.10.4 Allocation of Vectors for Interrupts and Other Exceptions during Programming and Erasure

Generation of an interrupt or other exception during programming or erasure may lead to fetching of the vector from the code flash memory. If this does not satisfy the conditions for using background operation, set the address for vector fetching to an address that is not in the code flash memory.

2.10.5 Abnormal Termination of Programming and Erasure

Even if programming/erasure ends abnormally due to the generation of a reset by the RES# pin, the programming/erasure state of the flash memory with undefined data cannot be verified or checked. For the area where programming/erasure ends abnormally, the blank check function cannot judge whether the area is erased successfully or not. Erase the area again to prove that the corresponding area is completely erased before using.

2.10.6 Items Prohibited during Programming and Erasure

Do not perform the following operations during programming and erasure.

- Have the operating voltage from the power supply go beyond the allowed range.
- Change the frequency of the peripheral clock.

Appendix 1 : Notes on Self-Programming of the Flash Memory

Regarding RA6M1, RA6M2, RA6M3, RA6T1, the following points should be noted.

1. Point to Note

When issuing a program command, writing of WD64 (in the user area) or WDN (in the data area) starts the program processing before the final value of the command, 0xD0, is written.
Therefore, if an interrupt occurs after WD64 or WDN has been written, the FSTATR.FRDY flag may become 1 regardless of 0xD0 not having been written. If an FACI command is issued in the interrupt handler, or if a subsequent FACI command is issued using an FRDY interrupt, writing the first byte of the FACI command may cause an illegal command error.

2. Workaround

When issuing a program command (from writing of 0xE8 to writing of 0xD0), disable interrupts that may trigger FACI commands.
If an interrupt occurs during the issuing of an FACI command and another FACI command is issued in the interrupt handler, the latter FACI command is either ignored or recognized as an illegal command, and normal operation thus cannot be expected. We recommend disabling such interrupts during the issuing of FACI commands as well as program commands.

3. Supplementary Note

When an illegal command error as described in 1. Point to Note occurs, the MCU can usually be returned to normal operation by reissuing the FACI command after general error handling. However, the MCU cannot be returned to normal operation if all of the following conditions are met. In such cases, work around the problem by the method described in 2. Workaround.

(a) A program command was issued during the suspension of erasure.
(b) An interrupt was accepted between the writing of WD64 or WDN and the writing of 0xD0 in the above program command.
(c) An FACI command issued in the handler for the above interrupt.
(d) A status clear command is used to handle an illegal command error.

Note that if the first FACI command issued in the interrupt handler described in (c) is a P/E resume command, the first 0xD0 byte is recognized as the final data of the program command, and an illegal command error will thus not occur, nor will resumption.

Website and Support

Visit the following vanity URLs to learn about key elements of the RA family, download components and related documentation, and get support.

RA Product Information	www.renesas.com/ra
RA Product Support Forum	www.renesas.com/ra/forum
RA Flexible Software Package	www.renesas.com/FSP
Renesas Support	www.renesas.com/support

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar *02*, 2020	—	First release document
1.10	Oct *20*, 2021	1, 2, 4, 8, 24, 25, 26, 28, 55	Addition of RA4W1 and RA6T1
1.20	Jul. 30, 2022	1) 1, 2, 4-8, 14, 19, 21, 23, 25, 28, 32, 34, 51, 54, 2) 75, 83, 102	Correction of Errors 1) Flash Type of RA2A1 : single to double 2) Program Command behavior

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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