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Renesas Electronics Corporation

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M16C/62A Group

External Buses

1. Abstract

The following article introduces external bus.

2. Introduction

The explanation of this issue is M16C/62A Group.

3. External Buses

3.1 Overview of External Buses

Memory and I/O external expansion can be connected to microcomputer easily by using external buses. When memory expansion mode or microprocessor mode is selected for processor mode, some of the pins function as the address bus, the data bus, and as control signals and this makes the external buses be able to operate.

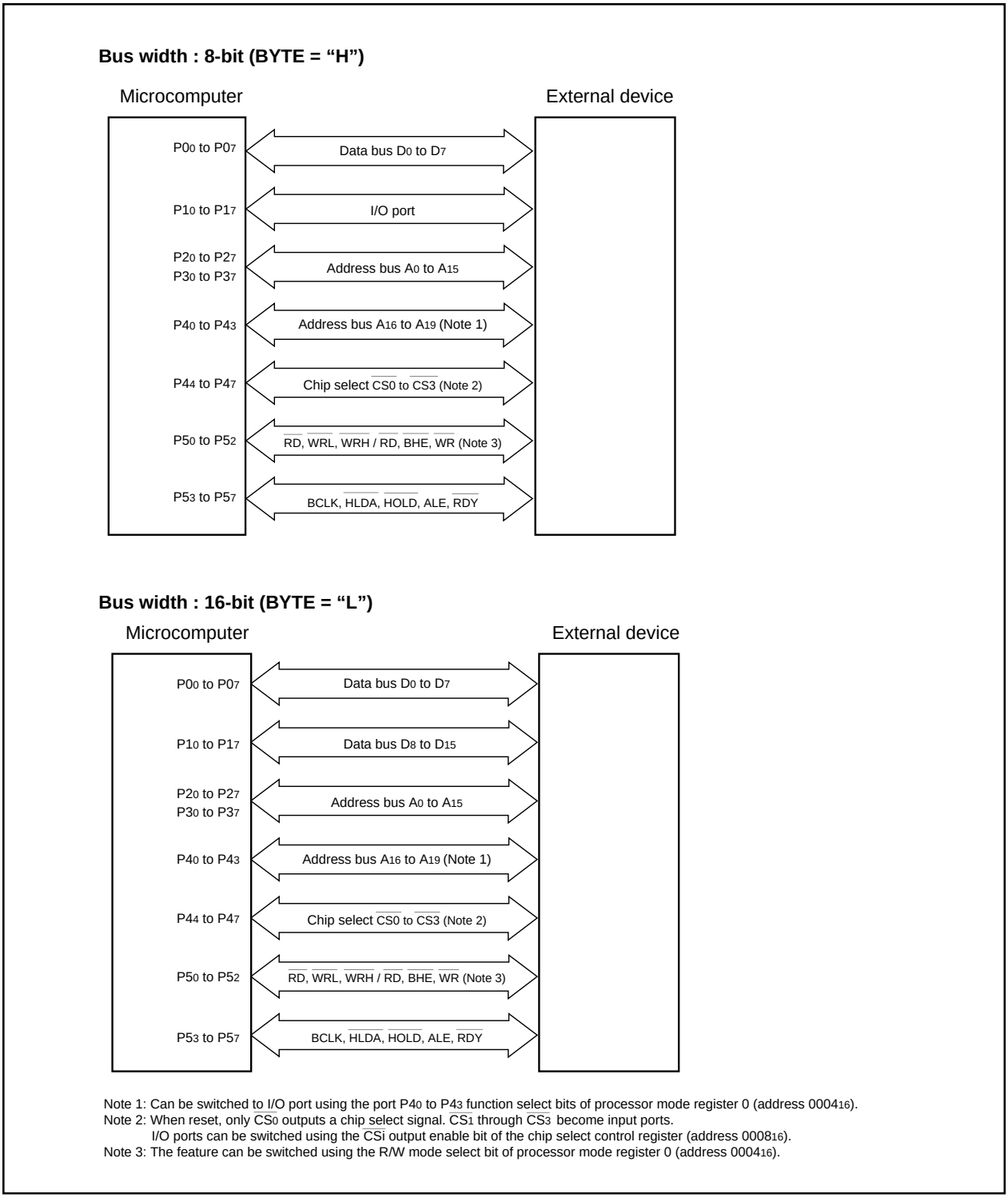
When accessing an external area, 8-bit data bus width or 16-bit data bus width can be selected, based on the BYTE pin level. 16-bit width is used to access an internal area, regardless of the level of the BYTE pin. Fix the BYTE pin either to “H” or “L” level. 8-bit and 16-bit data bus widths cannot be used together in an external area.

3.2 Data Access

3.2.1 Data Bus Width

If the voltage level input to the BYTE pin is “H”, the external data bus width becomes 8 bits, and P1$_0$ (/D$_8$) through P1$_7$ (/D$_{15}$) can be used as I/O ports (Figure 3.2.1).

If the voltage level input to the BYTE pin is “L”, the external data bus width becomes 16 bits, and P1$_0$ (/D$_8$) through P1$_7$ (/D$_{15}$) operate as a data bus (D$_8$ through D$_{15}$) (Figure 3.2.1).

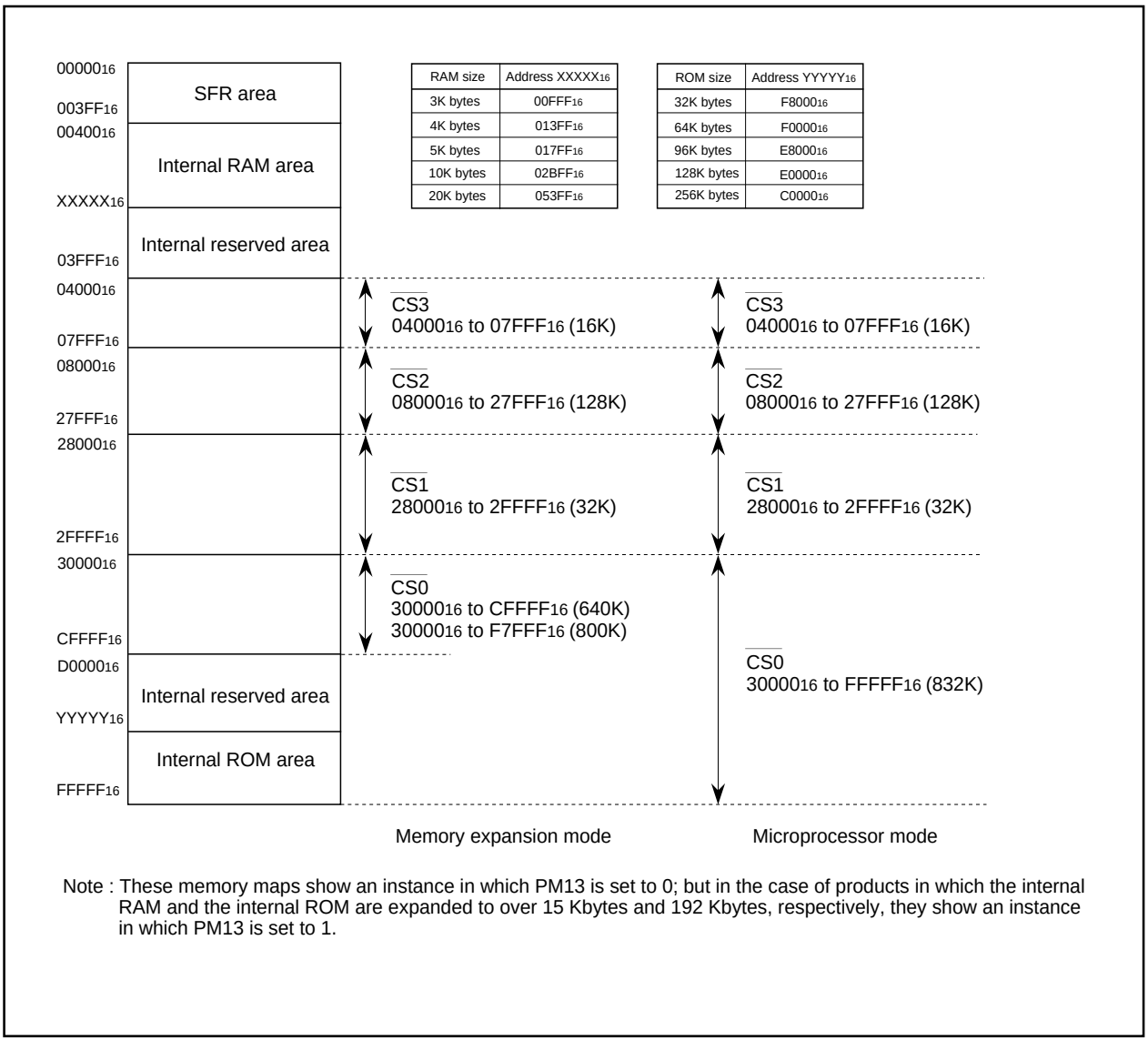


Note 1: Can be switched to I/O port using the port P4$_0$ to P4$_3$ function select bits of processor mode register 0 (address 0004$_{16}$).
Note 2: When reset, only CS$_0$ outputs a chip select signal. CS$_1$ through CS$_3$ become input ports.
I/O ports can be switched using the CS$_i$ output enable bit of the chip select control register (address 0008$_{16}$).
Note 3: The feature can be switched using the R/W mode select bit of processor mode register 0 (address 0004$_{16}$).

Figure 3.2.1. Level of BYTE pin and external data bus width

3.2.2 Chip Selects and Address Bus

Chip selects (P44/$\overline{CS0}$ through P47/$\overline{CS3}$) are output in areas resulting from dividing a 1-M byte memory space into four. To use the chip select, the chip select output must be enabled by setting the chip select control register. Figure 3.2.2 shows addresses in which chip selects become active ("L"). Since the extent of the internal area and the external area in memory expansion mode is different from those in microprocessor mode, there is a difference between areas for which $\overline{CS0}$ is output. When an internal ROM/RAM area is being accessed, no chip select is output, and the address bus does not change (the address of the external area that was accessed previously is held).



Note : These memory maps show an instance in which PM13 is set to 0; but in the case of products in which the internal RAM and the internal ROM are expanded to over 15 Kbytes and 192 Kbytes, respectively, they show an instance in which PM13 is set to 1.

Figure 3.2.2. Addresses in which chip selects turn active ("L")

Chip select control register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol: CSR
Address: 0008₁₆
When reset: 01₁₆

Bit symbol	Bit name	Function	R	W
CS0	$\overline{CS0}$ output enable bit	0 : Chip select output disabled (Normal port pin) 1 : Chip select output enabled	O	O
CS1	$\overline{CS1}$ output enable bit		O	O
CS2	$\overline{CS2}$ output enable bit		O	O
CS3	$\overline{CS3}$ output enable bit		O	O
CS0W	$\overline{CS0}$ wait bit	0 : Wait state inserted 1 : No wait state	O	O
CS1W	$\overline{CS1}$ wait bit		O	O
CS2W	$\overline{CS2}$ wait bit		O	O
CS3W	$\overline{CS3}$ wait bit		O	O

Figure 3.2.3. Chip select control register

3.2.3 Bus Types

The M16C/62A Group has two types of buses: a separate bus where separate pins are used for address output and data input/output and a multiplexed bus where pins are time- multiplexed and switched between address output and data input/output to save the number of pins used.
A separate bus is used to access devices such as ROM and RAM which have separate buses. The areas accessed via separate buses can be allocated for programs and data.
A multiplexed bus is used to access devices such as ASSPs which have multiplexed buses. The areas accessed via a multiplexed bus can only be allocated for data. Programs cannot be located in these areas.

The area accessed via a multiplex bus can be selected from three types of area $\overline{CS2}$ area, $\overline{CS1}$ area, and entire space by setting the multiplexed bus select bits (bits 4 and 5) of the processor mode register 0 (address 0004₁₆). However, the entire space cannot be selected when operating in the microprocessor mode.
Areas not accessed via multiplexed bus are accessed through separate buses.

When accessing an area set for access via a multiplexed bus the BYTE pin is “H” level, the data bus D_0 to D_7 is multiplexed with address bus A_0 to A_7.
If the BYTE pin is “L” level, the data bus D_0 to D_7 is multiplexed with address bus A_1 to A_8. In either case, the bus is switched between data and address separated only in time.
In the latter case, however, the addresses of connected devices are mapped into even addresses (every other addresses) of the M16C/62A. Therefore, be sure to access the M16C/62A's even addresses in length of bytes when accessing a connected device.

3.2.4 R/W Modes

The read/write signal that is output when accessing an external area can be selected between the $\overline{RD}$/$\overline{BHE}$/$\overline{WR}$ and the $\overline{RD}$/$\overline{WRH}$/$\overline{WRL}$ modes by setting the R/W mode select bit (bit 2) of the processor mode register 0 (address 0004₁₆). Use the $\overline{RD}$/$\overline{BHE}$/$\overline{WR}$ mode to access a 16-bit wide RAM and the $\overline{RD}$/$\overline{WRH}$/$\overline{WRL}$ mode to access an 8-bit wide RAM.
When the M16C/62A is reset, the $\overline{RD}$/$\overline{BHE}$/$\overline{WR}$ mode is selected by default. To switch over the R/W mode, change the $\overline{RD}$/$\overline{BHE}$/$\overline{WR}$ to the $\overline{RD}$/$\overline{WRH}$/$\overline{WRL}$ mode before accessing an external RAM.
Refer to the connection examples of $\overline{RD}$/$\overline{BHE}$/$\overline{WR}$ and $\overline{RD}$/$\overline{WRH}$/$\overline{WRL}$ shown in Section 3.3, "Connection Examples."

3.3 Connection Examples

3.3.1 16-bit Memory to 16-bit Width Data Bus Connection Example

Figure 3.3.1 shows an example of connecting M5M51016BTP (SRAM). In this diagram, when reset the microcomputer starts operating in single-chip mode. Change this mode to memory expansion mode in a program.

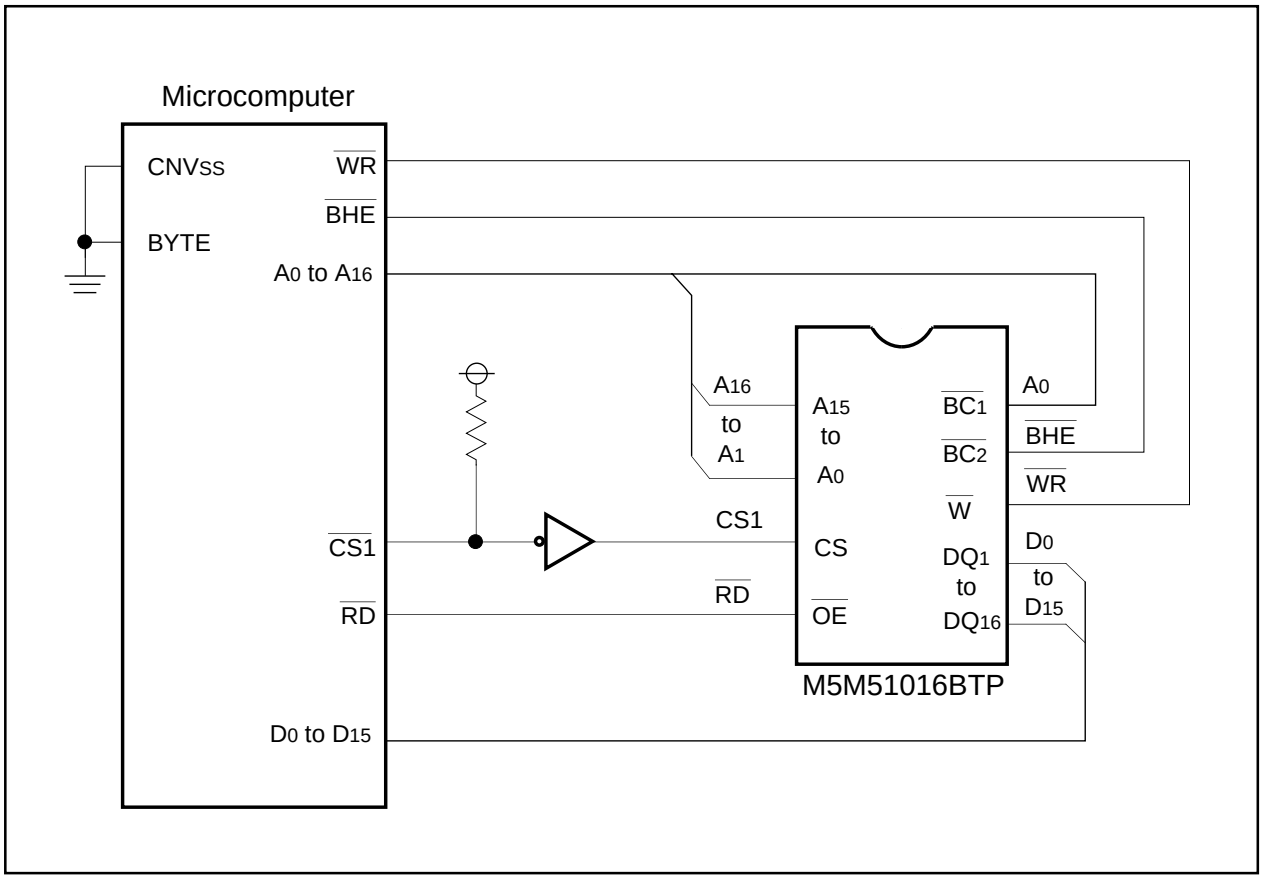


Figure 3.3.1. Example of connecting M5M51016BTP

3.3.2 8-bit Memory to 16-bit Width Data Bus Connection Example

Figure 3.3.2 shows an example of connecting two M5M5278's (SRAM) to a 16-bit data bus.In this diagram, when reset the microcomputer starts operating in single-chip mode. Change this mode to memory expansion mode in a program.

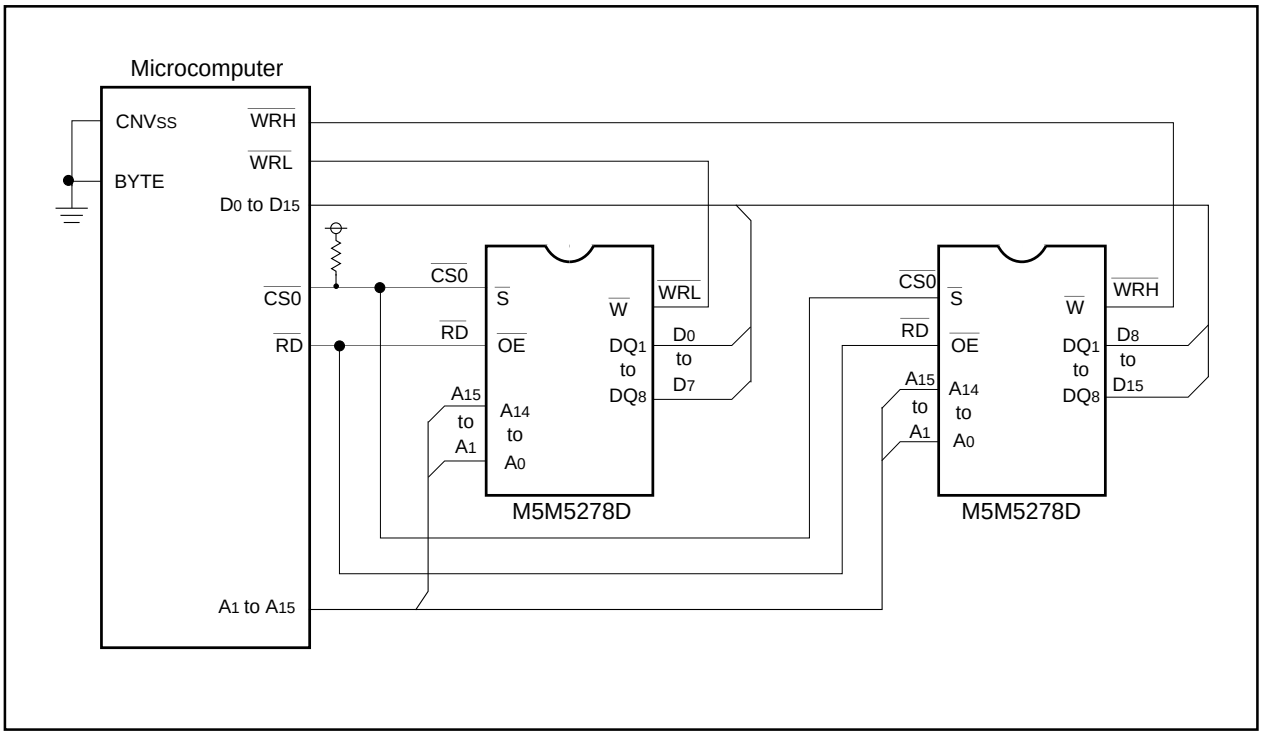


Figure 3.3.2. Example of connecting two M5M5278's to a 16-bit data bus

Figure 3.3.3 shows how to connect two Am29LV008B (flash memory). In 16-bit bus mode, the $\overline{BHE}$/$\overline{WRH}$ pin functions as $\overline{BHE}$. When connecting 8-bit flash memory chips to the 16-bit bus, make sure the microcomputer's $\overline{WRL}$ pin is connected to the $\overline{WR}$ pins on both flash memory chips, and that data is written to the flash memory in units of 16 bits beginning with an even address.

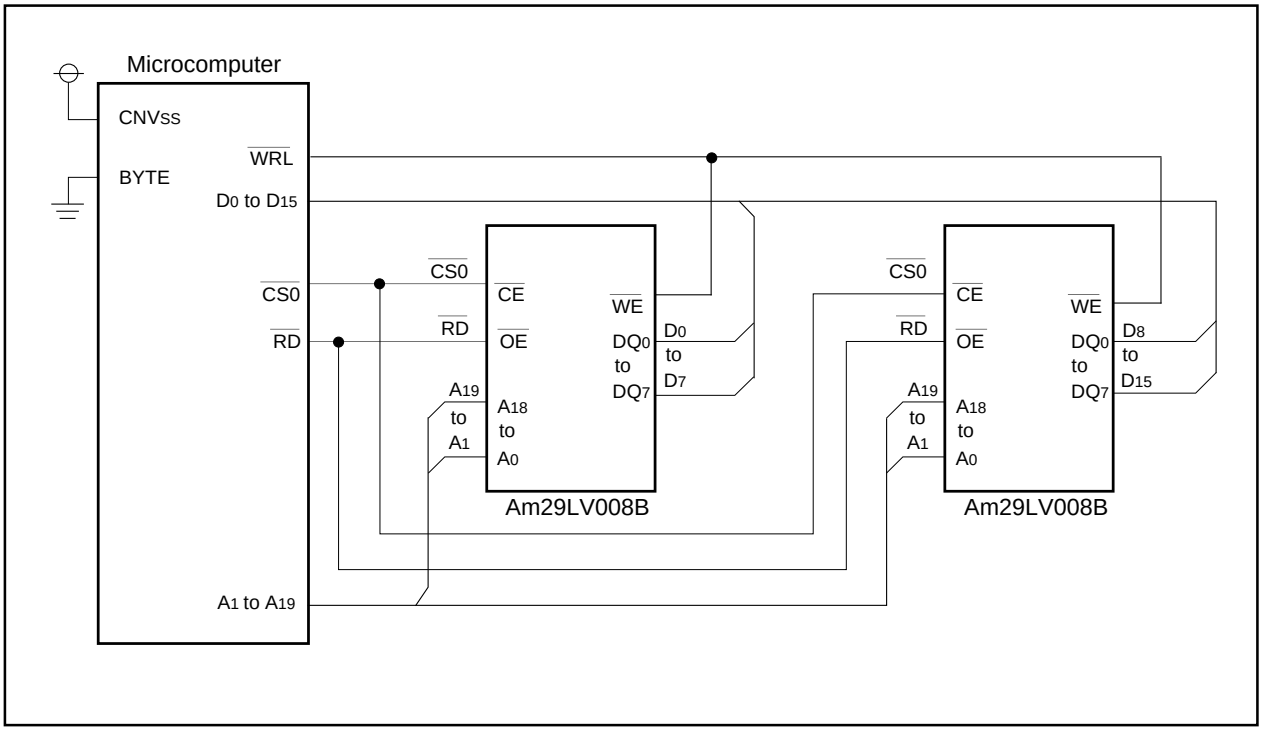


Figure 3.3.3. Example of connecting two Am29LV008B's to a 16-bit data bus

3.3.3 8-bit Memory to 8-bit Width Data Bus Connection Example

Figure 3.3.4 shows an example of connecting two M5M5278's (SRAM) to an 8-bit data bus. In this diagram, when reset the microcomputer starts operating in single-chip mode. Change this mode to memory expansion mode in a program.

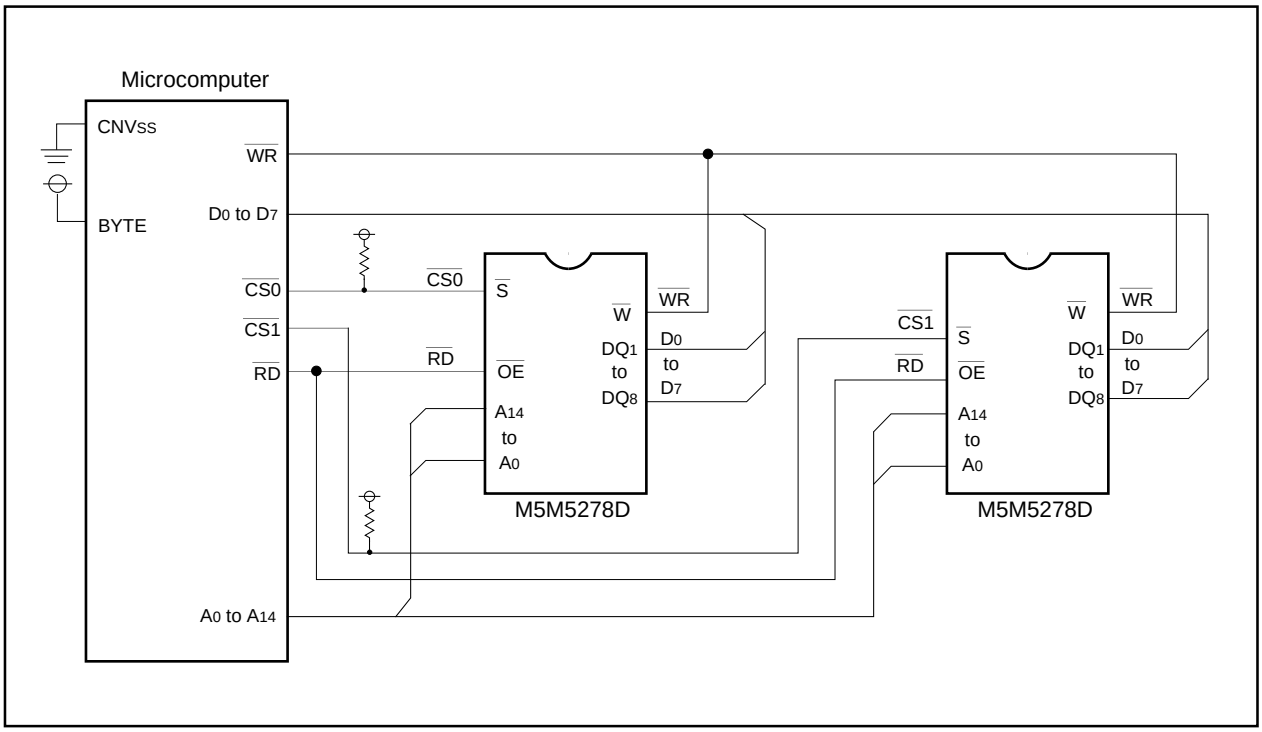


Figure 3.3.4. Example of connecting two M5M5278's to an 8-bit data bus

3.3.4 Two 8-bit and 16-Bit Memory to 16-Bit Width Data Bus Connection Example

Figure 3.3.5 shows an example of connecting M5M28F102 (16-bit flash memory) and two M5M5278's (8-bit SRAM) to a 16-bit data bus.

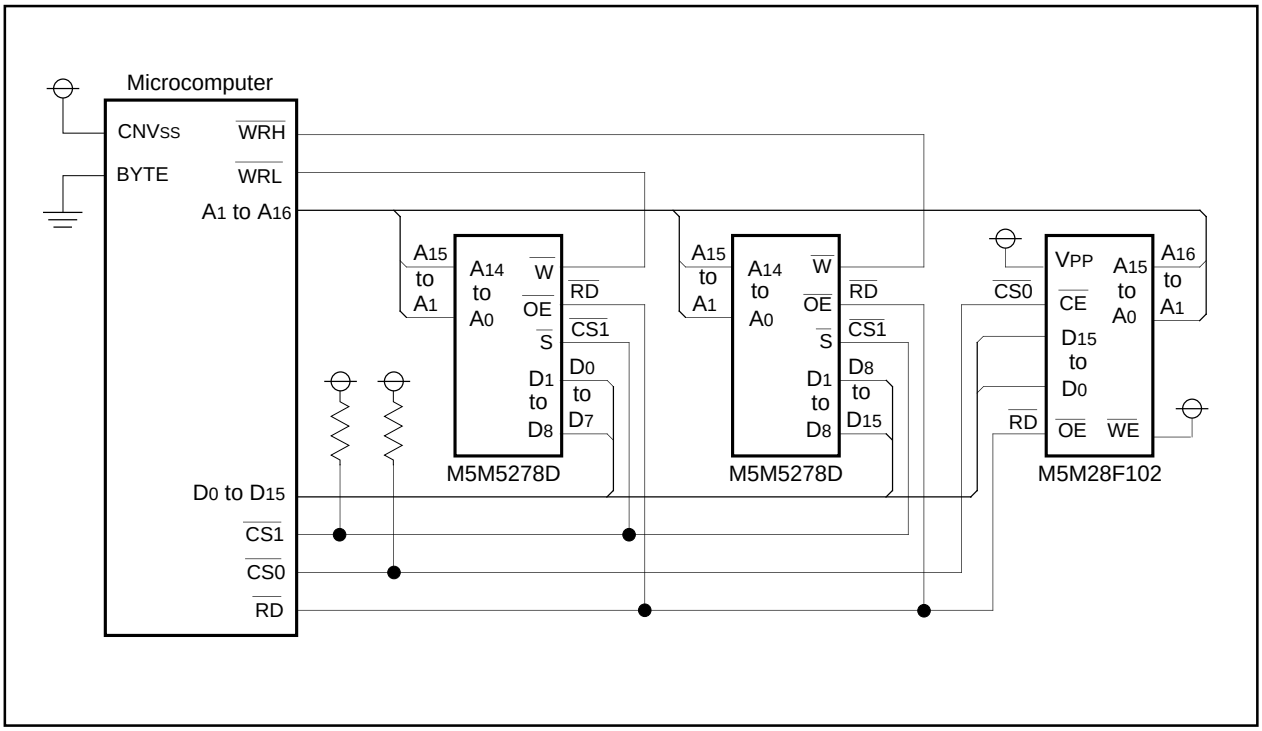


Figure 3.3.5. Example of connection of two 8-bit memories and one 16-bit memory to 16-bit width data bus

3.3.5 Chip Selects and Address Bus

When there are insufficient chip select signals, it is necessary to generate chip selects externally. Figure 3.3.6 shows an example of a connection in which the $\overline{CS2}$ (128K bytes) area is divided into four 32K byte areas.

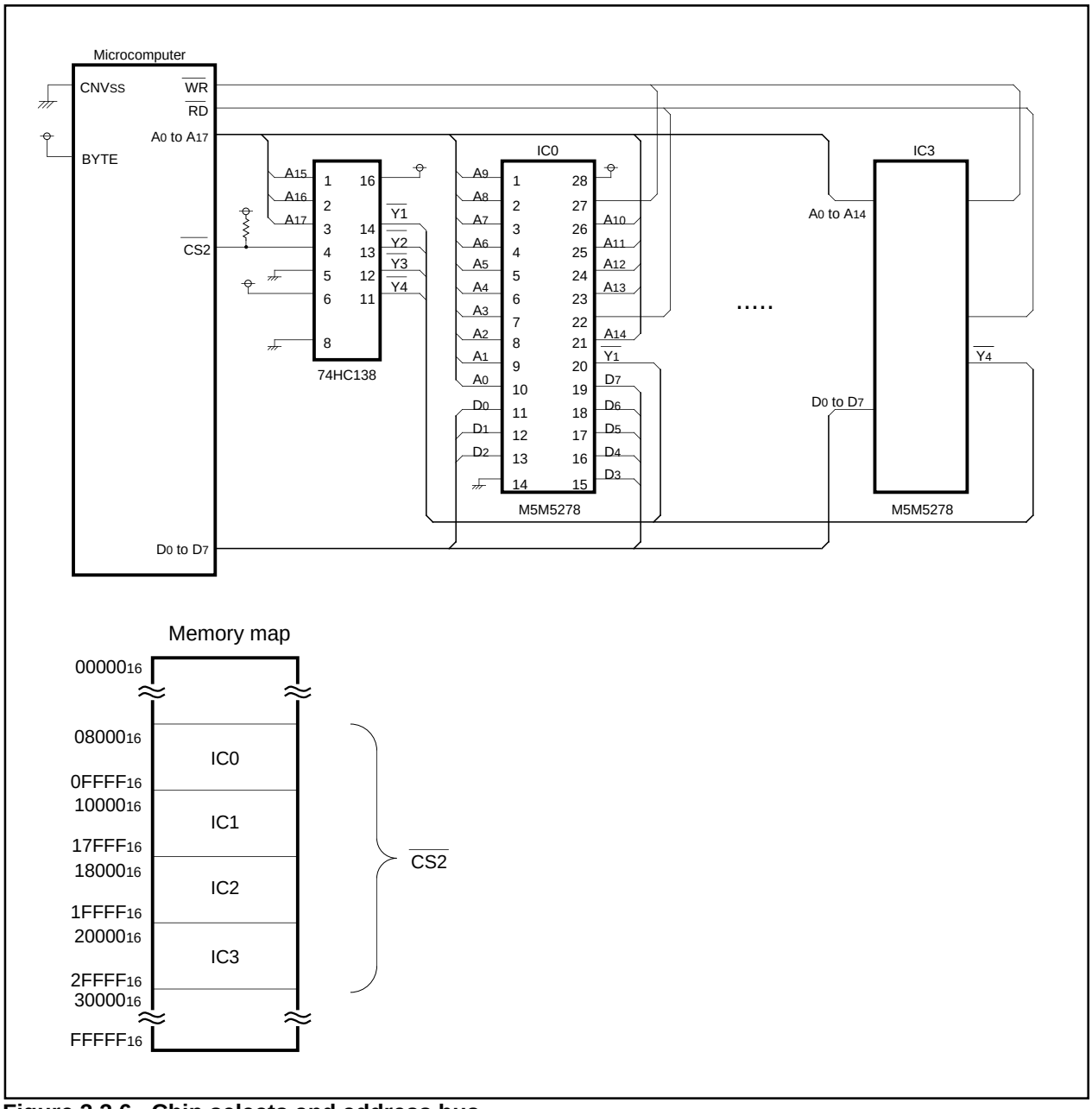


Figure 3.3.6. Chip selects and address bus

3.4 Connectable Memories

3.4.1 Operation Frequency and Access Time

Connectable memories depend upon the BCLK frequency f(BCLK). The frequency of f(BCLK) is equal to that of the BCLK , and is contingent on the oscillator's frequency and on the settings in the system clock select bits (bit 6 of address 0006_{16}, and bits 6 and 7 of address 0007_{16}).
The following are the conditional equations for the connections. Meet these conditions minimally. Figures 3.4.1 and 3.4.2 show the relation between the frequency of BCLK and memory.

(1) Read cycle time (tCR)/write cycle time (tCW)

Read cycle time (tCR) and write cycle time (tCW) must satisfy the following conditional expressions:

- **With the Wait option cleared**
  tCR < 10^9/f(BCLK) and tCW < 10^9/f(BCLK)
- **With the Wait option selected**
  tCR < 2 X 10^9/f(BCLK) and tCW < 2 X 10^9/f(BCLK)

(2) Address access time [ta(A)]

Address access time [ta(A)] must satisfy the following conditional expressions:

(a) Vcc = 5V

- **With the Wait option cleared**
  ta(A) < 10^9/f(BCLK) – 65(ns)*
- **With the Wait option selected**
  ta(A) < 2 X 10^9/f(BCLK) – 65(ns)*

* 65(ns) = td(BCLK – AD) + tsu(DB – RD) – th(BCLK – RD)
= (address output delay time) + (data input setup time) – (RD signal output hold time)

(b) Vcc = 3V

- **With the Wait option cleared**
  ta(A) < 10^9/f(BCLK) – 140(ns)*
- **With the Wait option selected**
  ta(A) < 2 X10^9/f(BCLK) – 140(ns)*

* 140(ns) = td(BCLK-AD) + tsu(DB – RD) – th(BCLK – RD)
= (address output delay time) + (data input setup time) – (RD signal output hold time)

(3) Chip select access time [ta(S)]

Chip select access time [ta(S)] must satisfy the following conditional expressions:

(a) Vcc = 5V

- **With the Wait option cleared**
  ta(S) < 10^9/f(BCLK) – 65(ns)*
- **With the Wait option selected**
  ta(S) < 2 X10^9/f(BCLK) – 65(ns)*

* 65(ns) = td(BCLK – CS) + tsu(DB – RD) – th(BCLK – RD)
= (chip select output delay time) + (data input setup time) – (RD signal output hold time)

(b) Vcc = 3V

- **With the Wait option cleared**

  ta(S) < 10^9/f(BCLK) – 140(ns)*

- **With the Wait option selected**

  ta(S) < 2 X10^9/f(BCLK) – 140(ns)*

* 140(ns) = td(BCLK – CS) + tsu(DB – RD) – th(BCLK – RD)
= (chip select output delay time) + (data input setup time) – (RD signal output hold time)

(4) Output enable time [ta(OE)]

Output enable time [ta(OE)] must satisfy the following conditional expressions:

(a) Vcc = 5V

- **With the Wait option cleared**

  ta(OE) < 10^9/(f(BCLK) X 2) – 45(ns) = tac1(RD-DB)

- **With the Wait option selected**

  ta(OE) < 3 X 10^9/(f(BCLK) X 2) – 45(ns) = tac2(RD-DB)

(b) Vcc = 3V

- **With the Wait option cleared**

  ta(OE) < 10^9/(f(BCLK) X 2) – 90(ns) = tac1(RD-DB)

- **With the Wait option selected**

  ta(OE) < 3X10^9/(f(BCLK) X 2) – 90(ns) = tac2(RD-DB)

(5) Data setup time [tsu(D)]

Data setup time [tsu(D)] must satisfy the following conditional expressions:

(a) Vcc = 5V

- **With the Wait option cleared**

  tsu(D) < 10^9/(f(BCLK) X 2) – 40(ns)*

- **With the Wait option selected**

  tsu(D) < 10^9/f(BCLK) – 40(ns)*

* 40(ns) = td(BCLK – DB) – th(BCLK – WR)
= (data output delay time) – (WR signal output hold time)

(b) Vcc = 3V

- **With the Wait option cleared**

  tsu(D) < 10^9/(f(BCLK) X 2) – 80(ns)*

- **With the Wait option selected**

  tsu(D) < 10^9/f(BCLK) – 80(ns)*

* 80(ns) = td(BCLK – DB) – th(BCLK – WR)
= (data output delay time) – (WR signal output hold time)

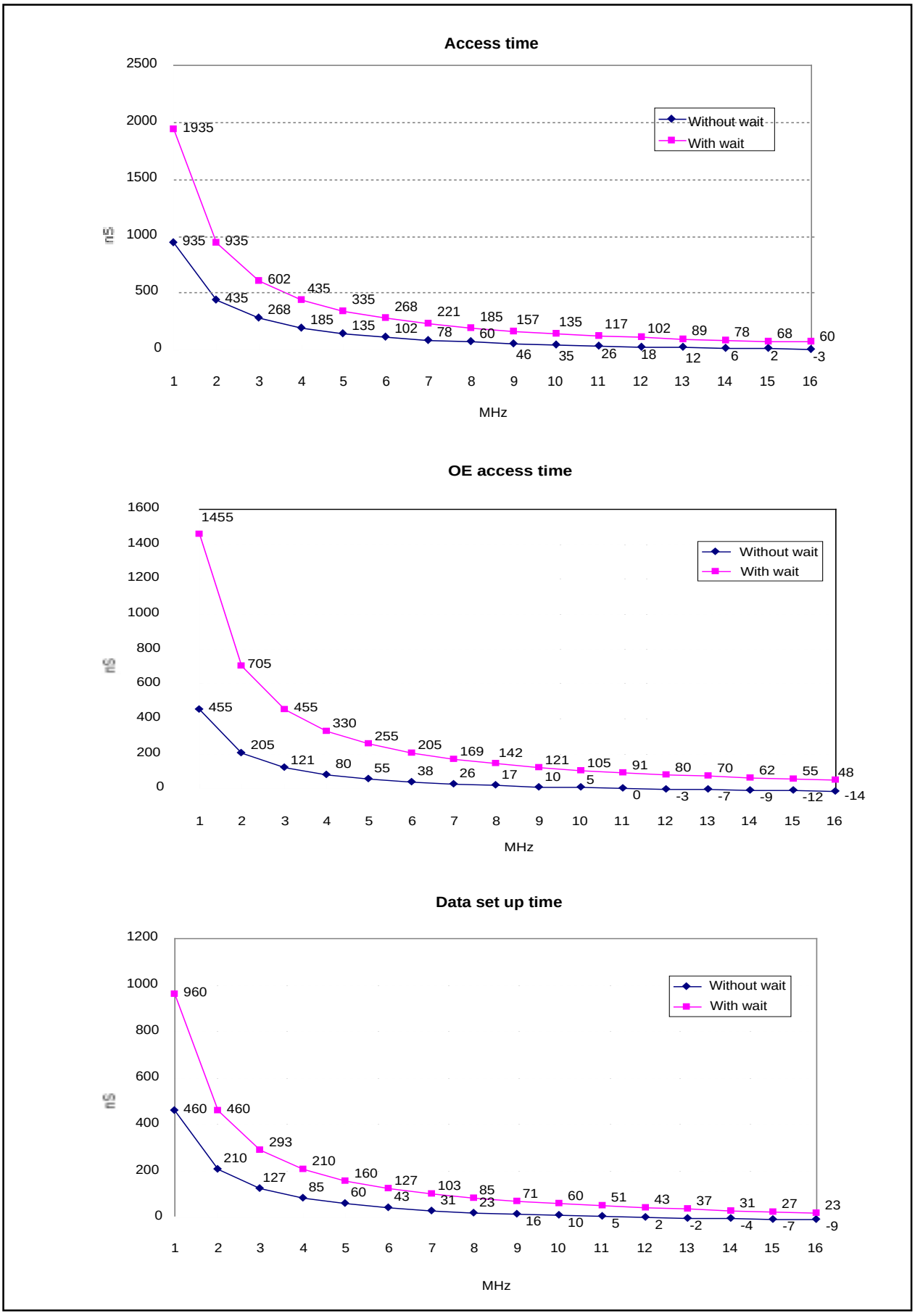


Figure 3.4.1. Relation between the frequency of BCLK and memory (Vcc = 5V)

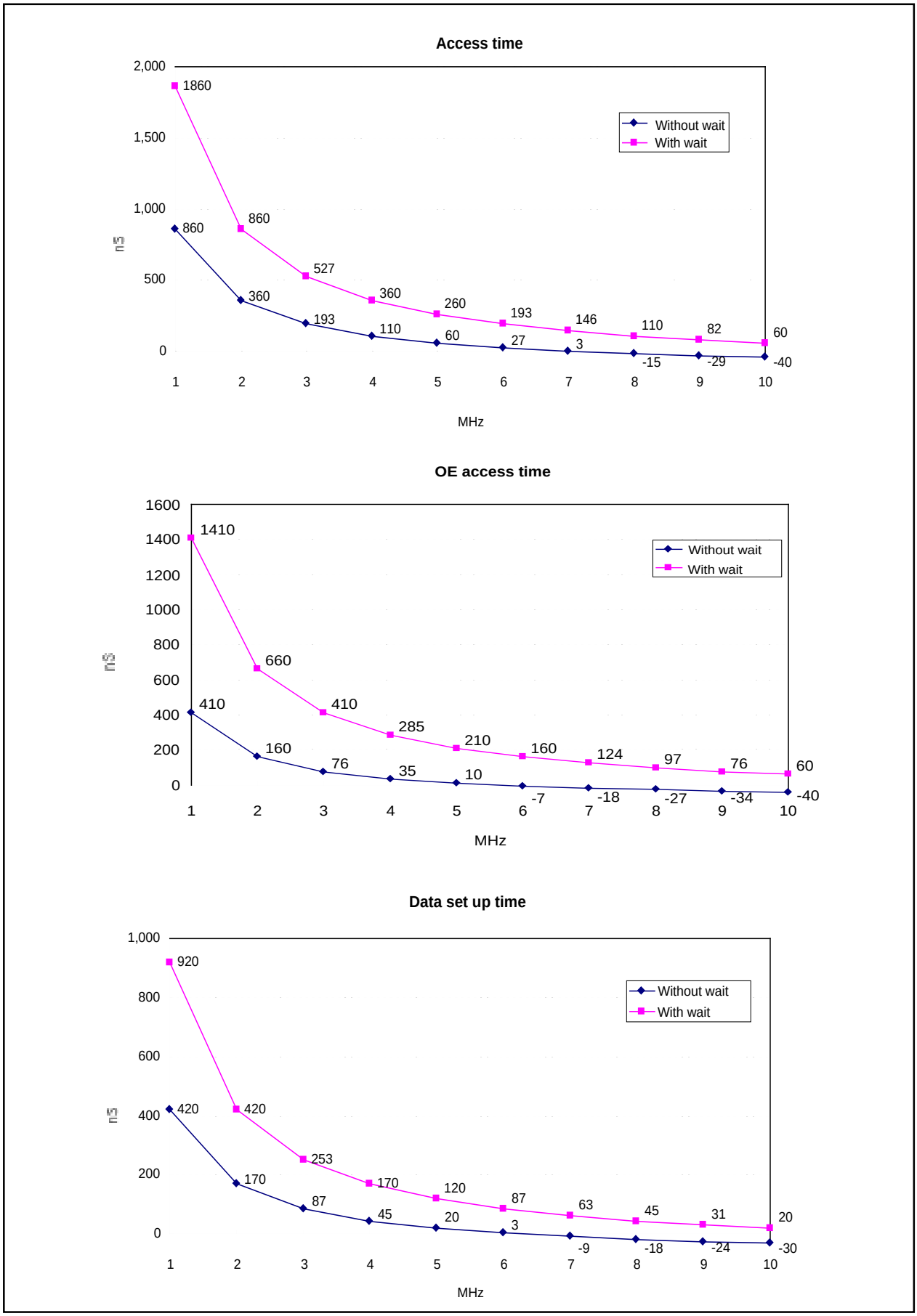


Figure 3.4.2. Relation between the frequency of BCLK and memory (Vcc = 3V)

3.4.2 Connecting Low-Speed Memory

To connect memory with long access time [ta(A)], either decrease the frequency of BCLK or set a software wait. Using the $\overline{RDY}$ feature allows you to connect memory having the timing that precludes connection though you set software wait.

(1) Using software wait

Set software wait by using either of bit 7 (PM17) of processor mode register 1 or bits 4 through 7 (CS0W through CS3W) of the chip select control register. With software wait set, if an address space is accessed in which a separate bus is selected, the bus cycle results in two cycles of BCLK; if an address space is accessed in which a multiplex bus is selected, the bus cycle results in three cycles of BCLK.

If bit 7 (PM17) of processor mode register 1 is set to “Wait selected”, the microcomputer accesses every area with this option in effect. If bit 7 (PM17) of processor mode register 1 is set to “Wait cleared”, the Wait option can be either selected or cleared, chip select by chip select, by setting bits 4 through 7 (CS0W through CS3W) of the chip select control register. Figures 3.4.3 through 3.4.5 show relation of processor mode and the wait bit (PM17, CSiW).

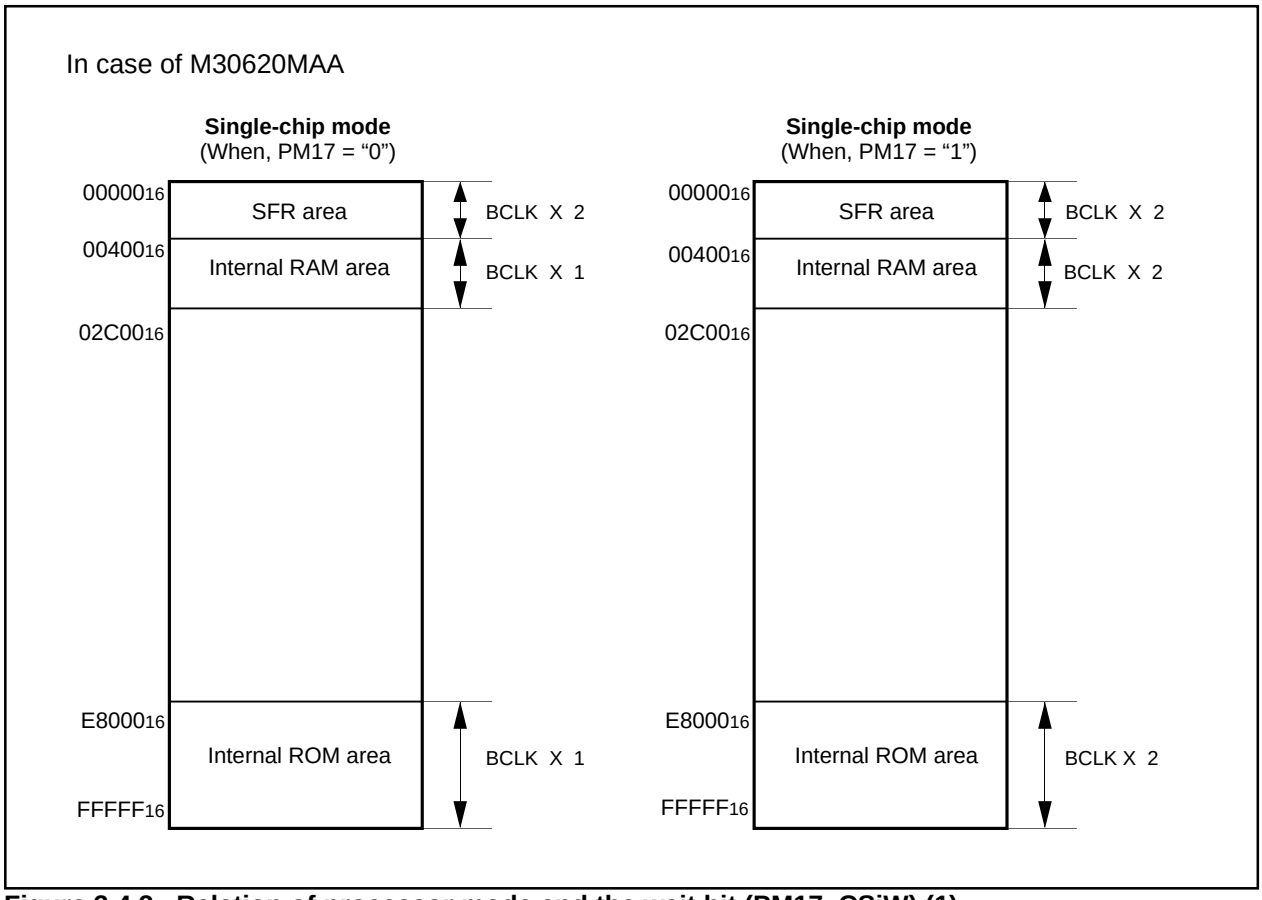
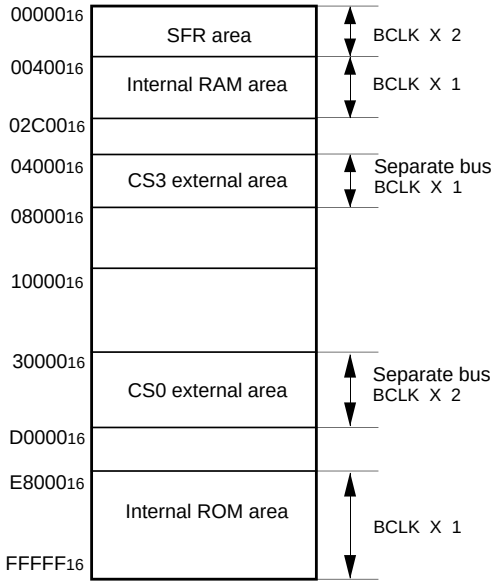


Figure 3.4.3. Relation of processor mode and the wait bit (PM17, CSiW) (1)

In case of M30620MAA

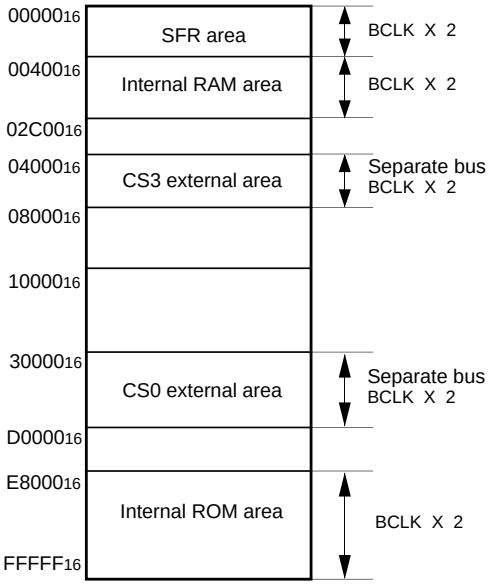
Memory expansion mode

When,
PM17 = “0”
PM04, PM05 = “00”
CS0 = “1”
CS3 = “1”
CS0W = “0”
CS3W = “1”



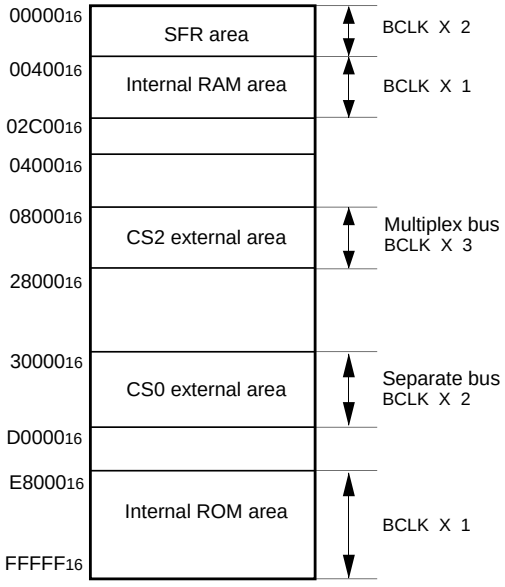
Memory expansion mode

When,
PM17 = “1”
PM04, PM05 = “00”
CS0 = “1”
CS3 = “1”
CS0W = “0”
CS3W = “1”



Memory expansion mode

When,
PM17 = “0”
PM04, PM05 = “10”
CS0 = “1”
CS2 = “1”
CS0W = “0”
CS2W = “0”



Memory expansion mode

When,
PM17 = “1”
PM04, PM05 = “10”
CS0 = “1”
CS2 = “1”
CS0W = “0”
CS2W = “0”

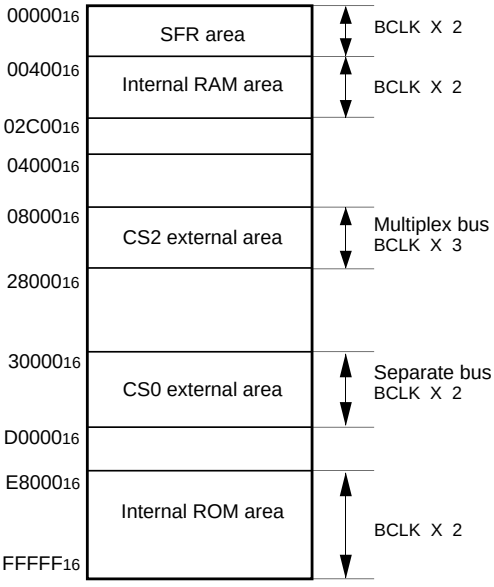


Figure 3.4.4. Relation of processor mode and the wait bit (PM17, CSiW) (2)

In case of M30620MAA

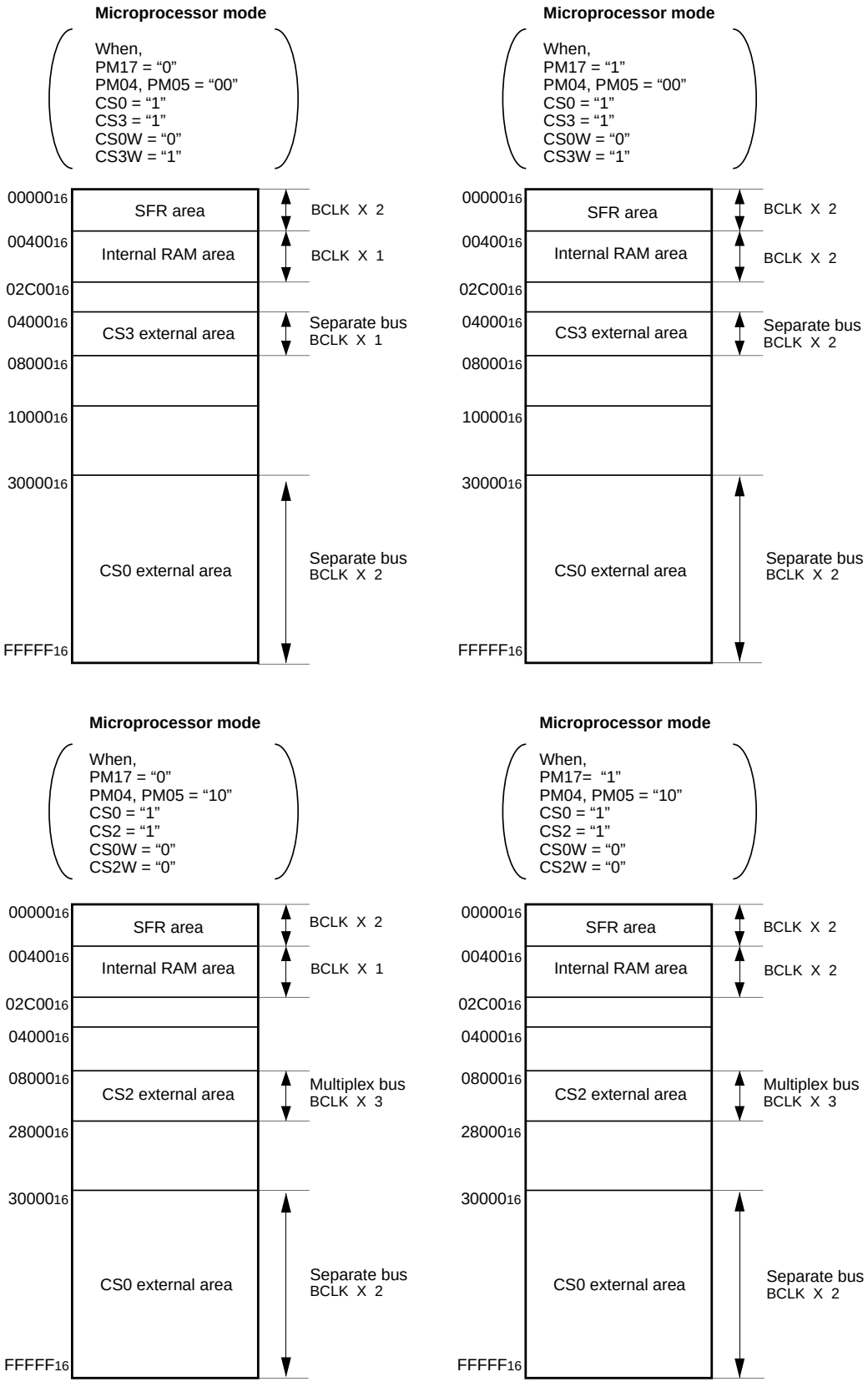


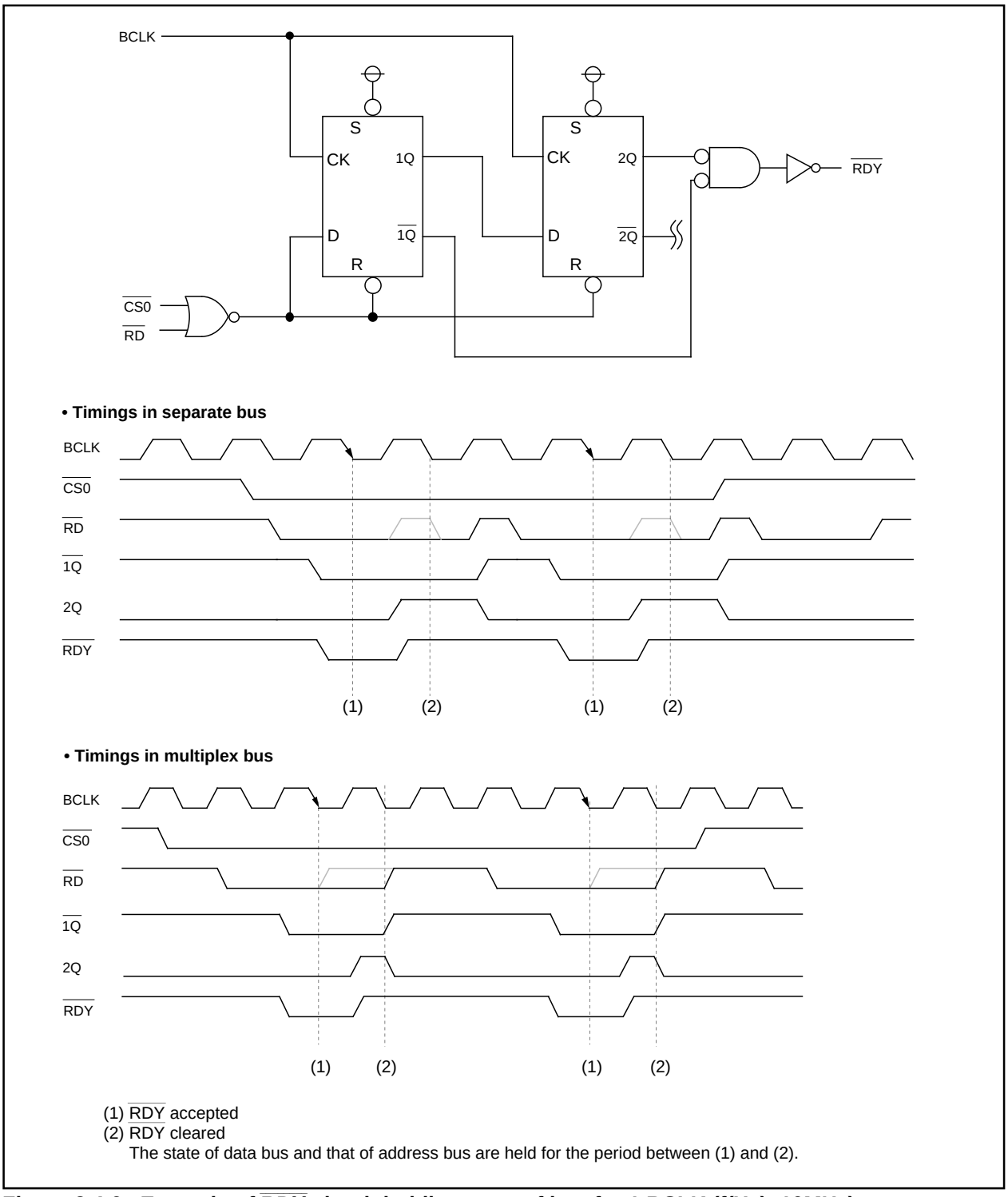
Figure 3.4.5. Relation of processor mode and the wait bit (PM17, CSiW) (3)

(2) $\overline{\text{RDY}}$ function usage

To use the $\overline{\text{RDY}}$ function, set a software wait.

The $\overline{\text{RDY}}$ function operates when the BCLK signal falls with the $\overline{\text{RDY}}$ pin at "L"; the bus does not vary for 1 BCLK, and the state at that moment is held.

The $\overline{\text{RDY}}$ function holds the state of bus for the period in which the $\overline{\text{RDY}}$ pin is at "L", and releases it when the BCLK signal falls with the $\overline{\text{RDY}}$ pin at "H". Figure 3.4.6 shows an example of $\overline{\text{RDY}}$ circuit (f(X_{IN})=10MHz) that holds the state of bus for 1 BCLK.



(1) $\overline{\text{RDY}}$ accepted
(2) $\overline{\text{RDY}}$ cleared
The state of data bus and that of address bus are held for the period between (1) and (2).

Figure 3.4.6. Example of $\overline{\text{RDY}}$ circuit holding state of bus for 1 BCLK (f(X_{IN})=10MHz)

3.4.3 Connectable Memories

Connectable memories and their maximum frequencies are given here;
M16C/62A group maximum frequency is
16MHz (without the wait) for Vcc=5V,
10MHz (with the one wait) for Vcc=3V

(1) Flash memories (Read only mode)

(a) 3V without wait

Maximum frequency (MHz)	Model No.
3.57	M5M29GB/T160BVP-80

(b) 3V with wait

Maximum frequency (MHz)	Model No.
8.33	M5M29GB/T160BVP-80

(2) SRAM

(a) 3V without wait

Maximum frequency (MHz)	Model No.
5.12	M5M54R08AJ-12 M5M54R16AJ,ATP-12

(b) 3V with wait

Maximum frequency (MHz)	Model No.
10.0	M5M54R08AJ-12 M5M54R16AJ,ATP-12

3.5 Releasing an External Bus ($\overline{\text{HOLD}}$ input and $\overline{\text{HLDA}}$ output)

The Hold feature is to relinquish the address bus, the data bus, and the control bus on M16C/62A side in line with the Hold request from the bus master other than M16C/62A when the two or more bus masters share the address bus, the data bus, and the control bus. The Hold feature is effective only in memory expansion mode and microprocessor mode.

The sequence of using the Hold feature may be:

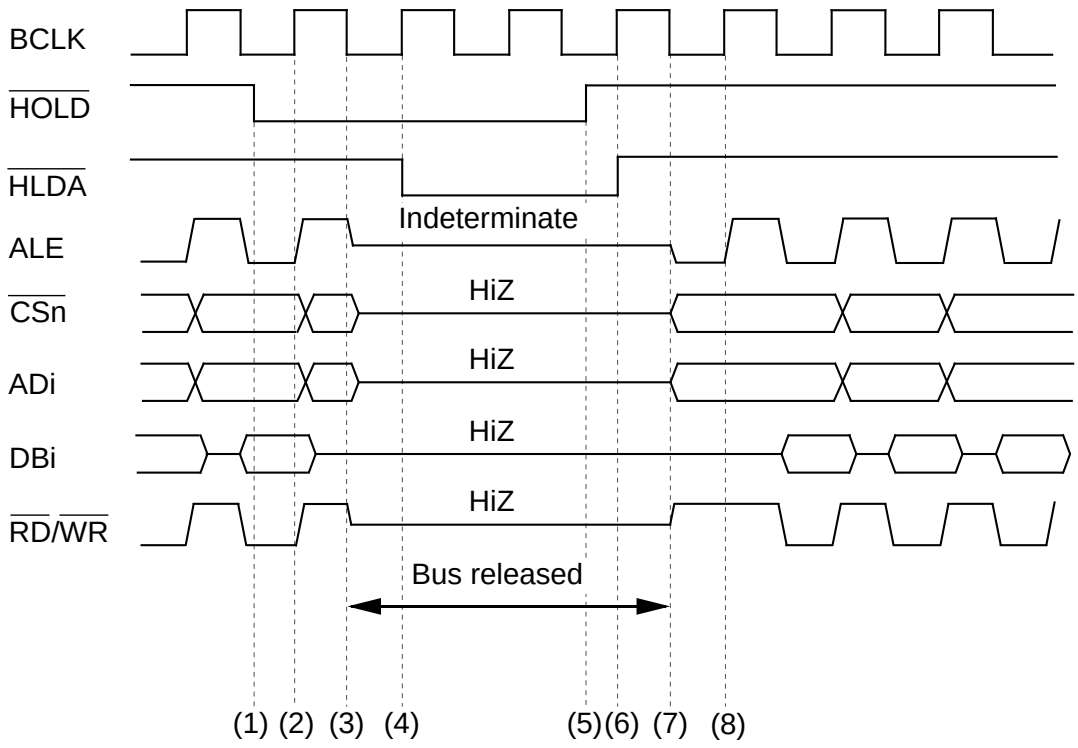
1. The external bus master turns the input level of the $\overline{\text{HOLD}}$ terminal to “L”.
2. When M16C/62A becomes ready to relinquish buses, each bus becomes high-impedance state at the falling edge of BCLK.
3. The $\overline{\text{HLDA}}$ terminal becomes “L” at the rising edge of the next BCLK.
4. The external bus master uses a bus.
5. When the external bus master finishes using a bus, the external bus master returns the input level of the $\overline{\text{HOLD}}$ terminal to “H”.
6. The output from $\overline{\text{HLDA}}$ terminal becomes “H” at the rising edge of the next BCLK.
7. Each bus returns from the high-impedance state to the former state at the falling edge of the next BCLK.

As given above, each bus invariably gets in the high-impedance state while the $\overline{\text{HLDA}}$ output is “L”. Also, M16C/62A does not relinquish buses during a bus cycle. That is, if a Hold request comes in during a bus cycle, the $\overline{\text{HLDA}}$ output become “L” after that bus cycle finishes.

In the Hold state, the state of each terminal becomes as follows.

- **Address bus A_0 to A_{19}**
  High-impedance state. The case in which A_{16} to A_{19} are used as ports $P4_0$ to $P4_3$ (64K byte address space) and the case in which A_9 to A_{19} are used as ports $P3_1$ to $P3_7$ and $P4_0$ to $P4_3$ (multiplex for the whole area) in microprocessor mode and in memory expansion mode too fall under this category.
- **Data bus D_0 to D_{15}**
  High-impedance state. The case in which D_8 to D_{15} are used as ports $P1_0$ to $P1_7$ (8-bit external bus width) and the case in which D_0 to D_{15} are used as ports $P0_0$ to $P0_7$ and $P1_0$ to $P1_7$ (multiplex for the whole area) in microprocessor mode and in memory expansion mode too fall under this category.
- **$\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, $\overline{\text{BHE}}$**
  High-impedance state.
- **ALE**
  An internal clock signal having the same phase as BCLK is output.
- **$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$**
  High-impedance state. The case in which ports are selected by the chip selection control register too falls under this category.

Figure. 3.5.1 shows an example of relinquishing external buses.



(1) An “L” level is input to the HOLD pin.
(2) HOLD is detected.
(3) The CPU releases the bus.
(4) An “L” is output to the HLDA pin.
(5) An “H” is input to the HOLD pin.
(6) An “H” is output to the HLDA pin.
(7) The CPU not releases the bus.
(8) The CPU resumes using the bus.

Figure 3.5.1. Example of releasing the external bus

3.6 Precautions for External Bus

The external ROM version can operate only in the microprocessor mode, so be sure to perform the following:

• Connect the CNVSS pin to Vcc.

4. Reference

Data Sheet
M16C/62A group data sheet Rev.B1
(Use the latest version on the Home page: http://www.renesas.com/)

User's Manual
M16C/62A group user's manual Rev.1.0
(Use the latest version on the Home page: http://www.renesas.com/)

5. Web-site and contact for support

Renesas Technology Corporation Semiconductor Home page
http://www.renesas.com/

E-mail Support
E-mail: support_apl@renesas.com

REVISION HISTORY

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