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H8SX Series

Enhancement with the Bit-Manipulation Instruction

Introduction

As well as having an architecture that is upward-compatible with each CPU of the H8/300, H8/300H, and H8S series, so as to inherit a full complement of peripheral functions, the H8SX microcomputer series has a maximum operating frequency of 50 MHz and uses a 32-bit H8SX core CPU as well as an on-chip multiplier/divider to improve performance.

This H8SX series Application Note provides information you may be need during software and hardware design. This is a basic edition that provides operation examples that each use a single H8SX series on-chip peripheral function.

Although the operation of each program, circuit, and other aspects covered by this application note has been checked, make sure that you conduct your own operation checks before actually using the H8SX series.

Contents

1. Overview

The H8SX series has an architecture that is upward-compatible with each CPU of the H8/300, H8/300H, and H8S series. Furthermore, in addition its instruction set has been enhanced to improve CPU performance. The enhancement of the instruction set has greatly improved coding efficiency compared to the conventional series. This coding efficiency leads to benefits such as a reduction in the amount of ROM required to store programs, as well as the shortening of each instruction fetch cycle. This application note describes the "enhancement with the bit-manipulation instruction", which is an enhanced instruction set item.

2. Configuration

The "enhancement with the bit-manipulation instruction" is described below. The conventional H8/300, H8/300H, and H8S series have no dedicated instruction for the assignment of bit-defined variables. With the H8SX series, however, a bit-manipulation instruction is added to enable the efficient assignment of bit-defined variables. For example, to assign the three low-order bits of a bit-defined variable to the three high-order bits of another defined variable with the conventional H8S series, masking and shifting of the variables is necessary, resulting in a large program size and long processing time. The addition of the bit-manipulation instruction means that this operation can be performed with only one instruction.

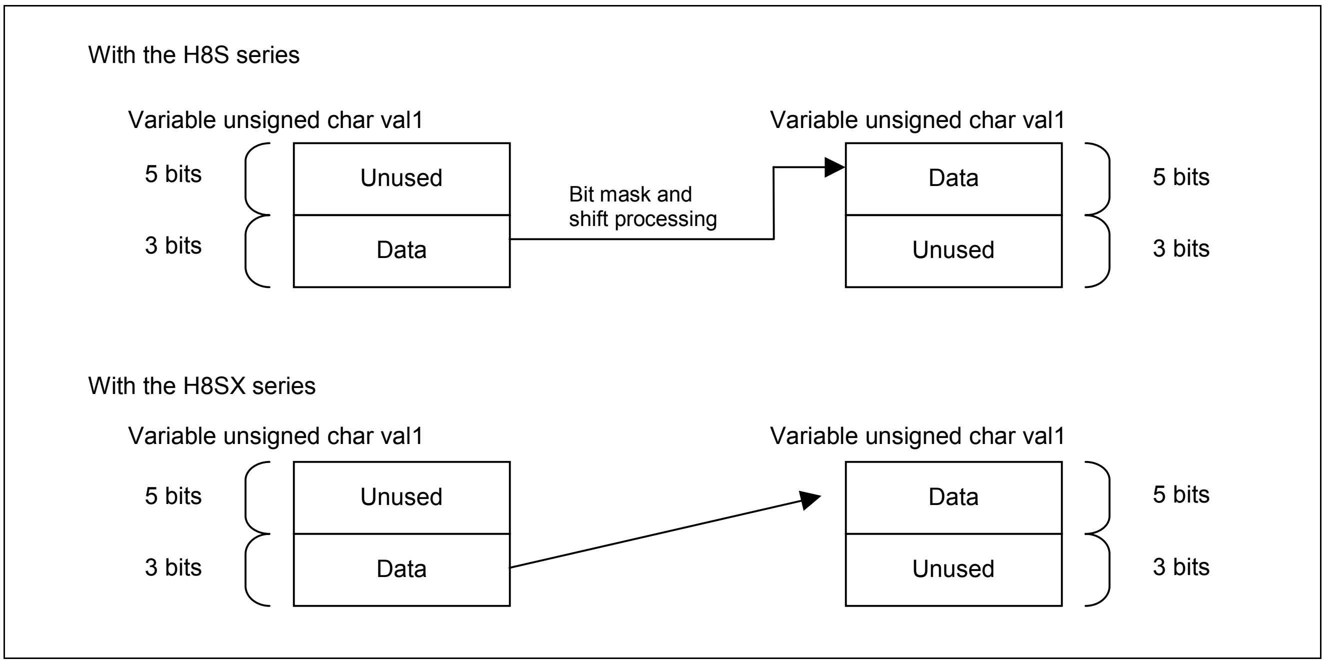


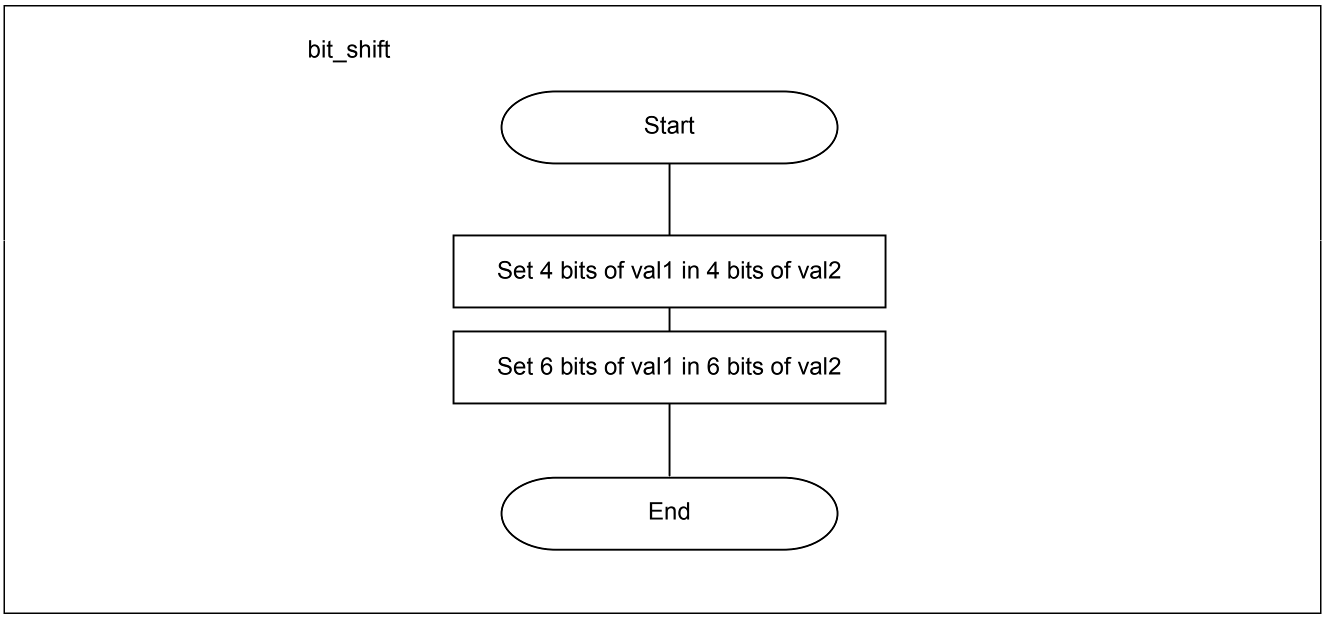
Figure 1 Enhancement with the Bit-Manipulation Instruction

3. Sample Program

3.1 Flowchart

The sample program shown below is very simple, and will allow you to understand the descriptions of "enhancement with the bit-manipulation instruction", an enhanced instruction set item.

As a comparison with the H8S series, the results of compilation are shown. This example is for reference only, because the instruction code length generated in the compilation of an application-level program greatly depends on the source program and compile conditions.



3.2 Program Listing

```
/*************************************************************/
/* Include File                                              */
/*************************************************************/
#include <machine.h>

/*************************************************************/
/* Function Prototype                                        */
/*************************************************************/
void bit_shift(void);

/*************************************************************/
/* RAM allocation                                            */
/*************************************************************/
struct
{
   unsigned long tmp1 :4;
   unsigned long bit27:1;
   unsigned long bit26:1;
   unsigned long bit25:1;
   unsigned long bit24:1;
   unsigned long bit23:1;
   unsigned long bit22:1;
   unsigned long bit21:1;
   unsigned long bit20:1;
   unsigned long bit19:1;
   unsigned long bit18:1;
   unsigned long bit17:1;
   unsigned long bit16:1;
   unsigned long bit15:1;
   unsigned long bit14:1;
   unsigned long bit13:1;
   unsigned long bit12:1;
   unsigned long bit11:1;
   unsigned long bit10:1;
   unsigned long bit9 :1;
   unsigned long bit8 :1;
   unsigned long bit7 :1;
   unsigned long bit6 :1;
   unsigned long tmp2 :6;
}val1;
struct
{
   unsigned short bit15:1;
   unsigned short bit14:1;
   unsigned short bit13:1;
   unsigned short tmp3 :4;
   unsigned short bit8 :1;
   unsigned short tmp4 :6;
   unsigned short bit1 :1;
   unsigned short bit0 :1;
}val2;
```

```
/*****************************************************************/
/* Function Definition(Main Program)                            */
/*****************************************************************/
void bit_shift(void)
{
   val1.tmp1 = 0x0F;
   val1.tmp2 = 0x3A;

   val2.tmp3 = val1.tmp1;
   val2.tmp4 = val1.tmp2;
}
```

3.3 Comparison of the H8S Series with the H8SX Series

The result of compilation (assembly code) with the H8S series is shown below.

```
P                                                ; section
  00000000 _bit_shift:                           ; function: bit_shift
  00000000     STM.L       (ER2-ER3),@-SP
  00000004     MOV.L       #_val1,ER3
  0000000A     MOV.L       @ER3,ER0
  0000000E     AND.L       #-6,ER0
  00000014     OR.L        #-268435398,ER0
  0000001A     MOV.L       ER0,@ER3
  0000001E     MOV.W       #4,R1
  00000022     JSR         @$BFUL$3:24
  00000026     MOV.W       R0,R1
  00000028     MOV.L       #_val2,ER0
  0000002E     MOV.W       #772,R2
  00000032     JSR         @$BFINI$3:24
  00000036     MOV.B       @(3:16,ER3),R0L
  0000003A     AND.B       #63,R0L
  0000003C     EXTU.W      R0
  0000003E     EXTU.L      ER0
  00000040     MOV.W       R0,R1
  00000042     MOV.L       #_val2,ER0
  00000048     MOV.W       #2054,R2
  0000004C     JSR         @$BFINI$3:24
  00000050     LDM.L       @SP+,(ER2-ER3)
  00000054     RTS

B                                                ; section
  00000000 _val1:                                ; static: val1
  00000000     .RES.W      2
  00000004 _val2:                                ; static: val2
  00000004     .RES.W      1
```

The result of compilation (assembly code) with the H8SX series is shown below.

```
P                                                ; section
  00000000 _bit_shift:                           ; function: bit_shift
  00000000     PUSH.W      R2
  00000002     MOV.B       #15:8,R0L
```

```
  00000004      BFST        R0L,#240,@_val1:32
  0000000C      MOV.B       #58:8,R0L
  0000000E      BFST        R0L,#63,@_val1+3:32
  00000016      BFLD        #240,@_val1:32,R0L
  0000001E      EXTU.L      #2,ER0
  00000020      MOV.W       R0,R1
  00000022      MOV.B       @_val2:32,R0H
  00000028      MOV.B       R1L,R0L
  0000002A      SHLL.B      R0L
  0000002C      AND.B       #30:8,R0L
  0000002E      AND.B       #225:8,R0H
  00000030      OR.B        R0L,R0H
  00000032      MOV.B       R0H,@_val2:32
  00000038      BFLD        #63,@_val1+3:32,R0L
  00000040      EXTU.L      #2,ER0
  00000042      MOV.B       @_val2+1:32,R2H
  00000048      MOV.B       R0L,R2L
  0000004A      SHLL.B      #2,R2L
  0000004C      AND.B       #3:8,R2H
  0000004E      OR.B        R2L,R2H
  00000050      MOV.B       R2H,@_val2+1:32
  00000056      POP.W       R2
  00000058      RTS

B                                                   ; section
  00000000 _val1:                                   ; static: val1
  00000000      .RES.W      2
  00000004 _val2:                                   ; static: val2
  00000004      .RES.W      1
```

Table 1 lists the results of compilation with the H8S series, while Table 2 lists the results obtained with the H8SX series.

Table 1 Results of Compilation (H8S Series)

H8S series		Instruction length In bytes	Instruction length Total	Execution state count State count	Execution state count Total
MOV.L	#_val1,ER3	6	50*	3	35*
MOV.L	@ER3,ER0	4		4	
AND.L	#-6,ER0	6		3	
OR.L	#-268435398,ER0	6		3	
MOV.L	ER0,@ER3	4		4	
MOV.W	#4,R1	4		2	
JSR	@$BFUL$3:24	4		5	
MOV.W	R0,R1	2		1	
MOV.L	#_val2,ER0	6		3	
MOV.W	#772,R2	4		2	
JSR	@$BFINI$3:24	4		5	

* The number of size states for the standard library BFUL and BFN2 are not included.

Table 2 Results of Compilation (H8SX Series)

H8SX series		Instruction length In bytes	Instruction length Total	Execution state count State count	Execution state count Total
BFLD	#240,@_val1:32,R0L	8	34	2	15
EXTU.L	#2,ER0	2		5	
MOV.W	R0,R1	2		1	
MOV.B	@_val2:32,R0H	6		1	
MOV.B	R1L,R0L	2		1	
SHLL.B	R0L	2		1	
AND.B	#30:8,R0L	2		1	
AND.B	#225:8,R0H	2		1	
OR.B	R0L,R0H	2		1	
MOV.B	R0H,@_val2:32	6		1	

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sept.19.03	—	First edition issued