RX65N/RX651 Group, RX230/RX231 Group

Difference Between RX65N Group and RX231 Group

Introduction

This application note is intended as a reference for confirming the points of difference between the I/O registers of the RX65N Group and RX231 Group.

Unless specifically otherwise noted, the information in this application note applies to the 176-/177-pin package version of the RX65N Group and the 100-pin package version and chip version B of the RX231 Group. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the user's manuals of the products in question.

Target Devices

RX65N Group and RX231 Group

Contents

1. Comparison of Functions of RX65N Group and RX231 Group

A comparison of the functions of the RX65N Group and RX231 Group is provided below. For details of the functions, see section 2, Comparative Overview of Functions and section 5, Reference Documents.

Table 1.1 is a Comparison of Functions of RX65N and RX231.

Table 1.1 Comparison of Functions of RX65N and RX231

Function	RX231	RX65N Code Flash 1.0 MB or less	RX65N Code Flash more than 1.5 MB
CPU	▲		
Operating Modes	●		
Address Space	▲		
Reset	●		
Option-Setting Memory	●/▲		
Voltage Detection Circuit (LVDAb): RX231, (LVDA): RX65N	●/■		
Clock Generation Circuit	●/▲/■		
Clock Frequency Accuracy Measurement Circuit (CAC)	○		
Low Power Consumption	●/▲		
Battery Backup Function	■		
Register Write Protection Function	▲/■		
Exception Handling	○		
Interrupt Controller (ICUb): RX231, (ICUB): RX65N	●/■		
Buses	●		
Memory-Protection Unit (MPU)	○		
DMA Controller (DMACA): RX231, (DMACAa): RX65N	▲		
EXDMA Controller (EXDMACa)	×	○*2	
Data Transfer Controller (DTCa): RX231, (DTCb): RX65N	●		
Event Link Controller (ELC)	▲		
I/O Ports	●/▲/■		
Multi-Function Pin Controller (MPC)	●		
Multi-Function Timer Pulse Unit 2 (MTU2a)	○	×	
Multi-Function Timer Pulse Unit 3 (MTU3a)	×	○	
Port Output Enable 2 (POE2a)	○	×	
Port Output Enable 3 (POE3a)	×	○	
16-Bit Timer Pulse Unit (TPUa)	●		
Programmable Pulse Generator (PPG)	×	○*2	
8-Bit Timer (TMR)	●		
Compare Match Timer (CMT)	○		
Compare Match Timer W (CMTW)	×	○	
Realtime Clock (RTCe): RX231, (RTCd): RX65N	●		
Low-Power Timer (LPT)	○	×	
Watchdog Timer (WDTA)	●		
Independent Watchdog Timer (IWDTa)	●		
Ethernet Controller (ETHERC)	×	○*2	
DMA Controller for the Ethernet Controller (EDMACa)	×	○*2	
USB 2.0 Host/Function Module (USBd): RX231 USB 2.0 FS Host/Function Module (USBb): RX65N	●/■		

Function		RX231	RX65N Code Flash 1.0 MB or less	RX65N Code Flash more than 1.5 MB
Serial Communications Interface (SCIg, SCIh): RX231, (SCIg, SCIi, SCIh): RX65N		●		
IrDA Interface		○	×	
I²C-bus Interface (RIICa)		▲		
CAN Module (RSCAN): RX231, (CAN): RX65N		●/▲/■*2		
Serial Sound Interface (SSI)		○	×	
Serial Peripheral Interface (RSPIa): RX231, (RSPIc): RX65N		▲		
Quad Serial Peripheral Interface (QSPI)		×	○	
CRC Calculator (CRC): RX231, (CRCA): RX65N		●		
SD Host Interface (SDHIa): RX231, (SDHI): RX65N		●		
SD Slave Interface (SDSI)		×	○*2	
MultiMediaCard Interface (MMCIF)		×	○*2	
Parallel Data Capture Unit (PDC)		×	○*2 *3	
Boundary Scan		×	○	
Security function	TSIP-lite	○	×	×
	TSIP	×	×	○
	AESa	○*1	○	○*1
	RNGa	○*1	○	○*1
Capacitive Touch Sensing Unit (CTSU)		○	×	
12-Bit A/D Converter (S12ADE): RX231, (S12ADFa): RX65N		●/▲/■		
12-Bit D/A Converter (R12DAA): RX231, (R12DAa): RX65N		●		
Temperature Sensor (TEMPSA): RX231, (TEMPS): RX65N		●		
Comparator B (CMPBa)		○	×	
Data Operation Circuit (DOC)		○		
RAM		●/▲		
Standby RAM		×	○	
Flash Memory (Code Flash)		●/▲/■		
Flash Memory (Data Flash)		○	×	○
Graphic LCD Controller (GLCDC)		×		○*2
2D Drawing Engine (DRW2D)		×		○*2
Package		▲		

Notes: ○: Function implemeznted, ×: Function not implemented, ●: Differences exist due to added functionality, ▲: Differences exist due to change in functionality, ■: Differences exist due to removal of functionality.

1. Implemented within Trusted Secure IP (TSIP) module.
2. Not implemented on 64-pin version.
3. Not implemented on 100-pin version.

2. Comparative Overview of Functions

2.1 CPU

Table 2.1 shows a Comparative Listing of CPU Specifications.

Table 2.1 Comparative Listing of CPU Specifications

Item	RX231	RX65N
CPU	• Maximum operating frequency: 54 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4 GB linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • Basic instructions: 75 • Floating-point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4 GB linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • Basic instructions: 75 • Floating-point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
FPU	• Single precision (32-bit) floating-point numeric values • Data types and exceptions in conformance with the IEEE 754 standard	• Single precision (32-bit) floating-point numeric values • Data types and exceptions in conformance with the IEEE 754 standard

2.2 Operating Modes

Table 2.2 shows a Comparative Listing of Operating Modes Specifications, and Table 2.3 shows a Comparative Listing of Operating Mode Registers.

Table 2.2 Comparative Listing of Operating Modes Specifications

Item	RX231	RX65N
Operating modes specified by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI interface)	Boot mode (SCI interface)
	Boot mode (USB interface)	Boot mode (USB interface)
	—	Boot mode (FINE interface)
Operating modes specified by register settings	Single-chip mode	Single-chip mode
	On-chip ROM disabled extended mode	On-chip ROM disabled extended mode
	On-chip ROM enabled extended mode	On-chip ROM enabled extended mode

Table 2.3 Comparative Listing of Operating Mode Registers

Register	Bit	RX231	RX65N
SYSCR1	SBYRAME	—	Standby RAM Enable

2.3 Address Space

Table 2.4 is a Comparative Memory Map of Single-Chip Mode, Table 2.5 is a Comparative Memory Map of On-Chip ROM Enabled Extended Mode, and Table 2.6 is a Comparative Memory Map of On-Chip ROM Disabled Extended Mode.

Table 2.4 Comparative Memory Map of Single-Chip Mode

Start Address	RX231	RX65N
0000 0000h	RAM	On-chip RAM
0001 0000h	Reserved area	
0004 0000h		Reserved area
0008 0000h	Peripheral I/O registers	Peripheral I/O registers
000A 4000h		Standby RAM
000A 6000h		Peripheral I/O registers
0010 0000h	On-chip ROM (E2 data flash)	On-chip ROM (data flash memory)
0010 2000h	Reserved area	
0010 8000h		Reserved area
007E 0000h		FACI command issuing area
007F 0004h		Reserved area
007F C000h	Peripheral I/O registers	Peripheral I/O registers
007F C500h	Reserved area	
007F FC00h	Peripheral I/O registers	
0080 0000h	Reserved area	On-chip expansion RAM
0086 0000h		Reserved area
FE7F 5D00h		On-chip ROM (option-setting memory)
FE7F 5D80h		Reserved area
FE7F 7D70h		On-chip ROM (read only)
FE7F 7DA0h		Reserved area
FFE0 0000h		On-chip ROM (code flash memory)
FFF8 0000h	On-chip ROM (program ROM) (read only)	

Table 2.5 Comparative Memory Map of On-Chip ROM Enabled Extended Mode

Start Address	RX231	RX65N
0000 0000h	RAM	On-chip RAM
0001 0000h	Reserved area	
0004 0000h		Reserved area
0008 0000h	Peripheral I/O registers	Peripheral I/O registers
000A 4000h		Standby RAM
000A 6000h		Peripheral I/O registers
0010 0000h	On-chip ROM (E2 data flash)	On-chip ROM (data flash memory)
0010 2000h	Reserved area	
0010 8000h		Reserved area
007E 0000h		FACI command issuing area
007F 0004h		Reserved area
007F C000h	Peripheral I/O registers	Peripheral I/O registers
007F C500h	Reserved area	
007F FC00h	Peripheral I/O registers	
0080 0000h	Reserved area	On-chip expansion RAM
0086 0000h		Reserved area
0100 0000h		CS7 (16 MB)
0200 0000h		CS6 (16 MB)
0300 0000h		CS5 (16 MB)
0400 0000h		CS4 (16 MB)
0500 0000h	CS3 (16 MB)	CS3 (16 MB)
0600 0000h	CS2 (16 MB)	CS2 (16 MB)
0700 0000h	CS1 (16 MB)	CS1 (16 MB)
0800 0000h	Reserved area	SDCS (128 MB)
1000 0000h		Reserved area
FE7F 5D00h		On-chip ROM (option-setting memory)
FE7F 5D80h		Reserved area
FE7F 7D70h		On-chip ROM (read only)
FE7F 7DA0h		Reserved area
FFE0 0000h		On-chip ROM (code flash memory)
FFF8 0000h	On-chip ROM (program ROM) (read only)	

Note: Areas enclosed in thick-bordered boxes are in the external address space (CS area and SDRAM area).

Table 2.6 Comparative Memory Map of On-Chip ROM Disabled Extended Mode

Start Address	RX231	RX65N
0000 0000h	RAM	On-chip RAM
0001 0000h	Reserved area	
0004 0000h		Reserved area
0008 0000h	Peripheral I/O registers	Peripheral I/O registers
000A 4000h		Standby RAM
000A 6000h		Peripheral I/O registers
0010 0000h	Reserved area	Reserved area
0080 0000h		On-chip expansion RAM
0086 0000h		Reserved area
0100 0000h		CS7 (16 MB)
0200 0000h		CS6 (16 MB)
0300 0000h		CS5 (16 MB)
0400 0000h		CS4 (16 MB)
0500 0000h	CS3 (16 MB)	CS3 (16 MB)
0600 0000h	CS2 (16 MB)	CS2 (16 MB)
0700 0000h	CS1 (16 MB)	CS1 (16 MB)
0800 0000h	Reserved area	SDCS (128 MB)
1000 0000h		Reserved area
FF00 0000h	CS0 (16 MB)	CS0 (16 MB)

Note: Areas enclosed in thick-bordered boxes are in the external address space (CS area and SDRAM area).

2.4 Reset

Table 2.7 shows a Comparative Listing of Reset Specifications, and Table 2.8 shows a Comparative Listing of Reset Registers.

Table 2.7 Comparative Listing of Reset Specifications

Item	RX231	RX65N
Reset Name	RES# pin reset	RES# pin reset
	Power-on reset	Power-on reset
	Voltage monitoring 0 reset	Voltage monitoring 0 reset
	Voltage monitoring 1 reset	Voltage monitoring 1 reset
	Voltage monitoring 2 reset	Voltage monitoring 2 reset
	—	Deep software standby reset
	Independent watchdog timer reset	Independent watchdog timer reset
	Watchdog timer reset	Watchdog timer reset
	Software reset	Software reset

Table 2.8 Comparative Listing of Reset Registers

Register	Bit	RX231	RX65N
RSTSR0	DPSRSTF	—	Deep Software Standby Reset Flag

2.5 Option-Setting Memory

Table 2.9 shows a Comparative Listing of Option-Setting Memory Registers.

Table 2.9 Comparative Listing of Option-Setting Memory Registers

Register	Bit	RX231 (OFSM)	RX65N (OFSM)
SPCC	—	—	Serial Programmer Command Control Register
OSIS	—	—	OCD/Serial Programmer ID Setting Register
OFS0	IWDTTOPS[1:0]	IWDT Timeout Period Select b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh)	IWDT Timeout Period Select b3 b2 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh)
	IWDTRSTIRQS	IWDT Reset Interrupt Request Select 0: Non-maskable interrupt request is enabled 1: Reset is enabled	IWDT Reset Interrupt Request Select 0: Non-maskable interrupt request or plain interrupt request is enabled 1: Reset is enabled
	IWDTSLCSTP	IWDT Sleep Mode Count Stop Control 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, or deep sleep mode	IWDT Sleep Mode Count Stop Control 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, deep software standby, or all-module clock stop mode
	WDTRSTIRQS	WDT Reset Interrupt Request Select 0: Non-maskable interrupt request is enabled 1: Reset is enabled	WDT Reset Interrupt Request Select 0: Non-maskable interrupt request or plain interrupt request is enabled 1: Reset is enabled
OFS1	VDSEL[1:0]	Voltage Detection 0 Level Select b1 b0 0 0: 3.84 V is selected 0 1: 2.82 V is selected 1 0: 2.51 V is selected 1 1: 1.90 V is selected	Voltage Detection 0 Level Select b1 b0 0 0: Reserved 0 1: Selects 2.94 V 1 0: Selects 2.87 V 1 1: Selects 2.80 V
	FASTSTUP	Power-On Fast Startup Time	—
MDE	BANKMD[2:0]	—	Bank Mode Select*1
TMEF	—	—	TM Enable
TMINF	—	—	TM Identification Data Register
BANKSEL	—	—	Bank Select Register*1

Register	Bit	RX231 (OFSM)	RX65N (OFSM)
FAW	—	—	Flash Access Window Setting Register
ROMCODE	—	—	ROM Code Protection Register

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

2.6 Voltage Detection Circuit

Table 2.10 shows a Comparative Listing of Voltage Detection Circuit Specifications, and Table 2.11 shows a Comparative Listing of Voltage Detection Circuit Registers.

Table 2.10 Comparative Listing of Voltage Detection Circuit Specifications

Item		RX231 (LVDAb)			RX65N (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	Voltage drops past Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2	Voltage drops past Vdet0	Voltage rises or drops past Vdet1	Voltage rises or drops past Vdet2
				Input voltages to VCC and the CMPA2 pin can be switched using the LVCMPCR.EXVCCINP2 bit			—
	Detection voltage	Voltage selectable from four levels using OFS1	Voltage selectable from 14 levels using the LVDLVLR.LVD1LVL[3:0] bits	Voltage selectable from four levels using the LVDLVLR.LVD2LVL[1:0] bits	Selectable from among three different levels by using OFS1.VDSEL[1:0] bits	Selectable from among three different levels by using LVDLVLR.LVD1LVL[3:0] bits	Selectable from among three different levels by using LVDLVLR.LVD2LVL[3:0] bits
	Monitor flag	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection		LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC or the CMPA2 pin CPU restart timing selectable: after specified time with VCC or the CMPA2 pin > Vdet2 or after specified time with Vdet2 > VCC or the CMPA2 pin	Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC

Item		RX231 (LVDAb)			RX65N (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Voltage detection processing	Interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Non-maskable or maskable interrupt is selectable	Non-maskable or maskable interrupt is selectable		Non-maskable interrupt or maskable interrupt selectable	Non-maskable interrupt or maskable interrupt selectable
			Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC or the CMPA2 pin and VCC or the CMPA2 pin > Vdet2 or either		Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either
Digital filter	Enable/ disable switching	—	—	—	—	Available	Available
	Sampling time	—	—	—	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event link function		—	Available Vdet1 passage detection event output	Available Vdet2 passage detection event output	—	Available Output of event signals on detection of Vdet1 crossings	Available Output of event signals on detection of Vdet2 crossings

Table 2.11 Comparative Listing of Voltage Detection Circuit Registers

Register	Bit	RX231 (LVDAb)	RX65N (LVDA)
LVD1CR1	LVD1IDTSEL [1:0]	Voltage Monitoring 1 Interrupt ELC Event Generation Condition Select	Voltage Monitoring 1 Interrupt Generation Condition Select
LVD2CR1	LVD2IDTSEL [1:0]	Voltage Monitoring 2 Interrupt ELC Event Generation Condition Select b1 b0 0 0: When VCC or the CMPA2 pin ≥ Vdet2 (rise) is detected 0 1: When VCC or the CMPA2 pin < Vdet2 (drop) is detected 1 0: When drop and rise are detected 1 1: Setting prohibited	Voltage Monitoring 2 Interrupt Generation Condition Select b1 b0 0 0: When VCC ≥ Vdet2 (rise) is detected 0 1: When VCC < Vdet2 (drop) is detected 1 0: When drop and rise are detected 1 1: Settings prohibited
LVD2SR	LVD2MON	Voltage Monitoring 2 Signal Monitor Flag 0: VCC or the CMPA2 pin < Vdet2 1: VCC or the CMPA2 pin ≥ Vdet2 or LVD2MON is disabled	Voltage Monitoring 2 Signal Monitor Flag 0: VCC < Vdet2 1: VCC ≥ Vdet2 or LVD2MON is disabled
LVCMPCR	EXVCCINP2	Voltage Detection 2 Comparison Voltage External Input Select	—

Register	Bit	RX231 (LVDAb)	RX65N (LVDA)
LVDLVLR	LVD1LVL[3:0]	Voltage Detection 1 Level Select (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.14 V 0 0 1 0: 4.02 V 0 0 1 1: 3.84 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V 1 0 0 1: 2.58 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Settings other than those listed above are prohibited	Voltage Detection 1 Level Select (Standard voltage during drop in voltage) b3 b0 1 0 0 1: 2.99 V (Vdet1_1) 1 0 1 0: 2.92 V (Vdet1_2) 1 0 1 1: 2.85 V (Vdet1_3) Settings other than above are prohibited
		The Value after reset is different	
	LVD2LVL[1:0]: RX231 LVD2LVL[3:0]: RX65N	Voltage Detection 2 Level Select (Standard voltage during drop in voltage) b5 b4 0 0: 4.29 V 0 1: 4.14 V 1 0: 4.02 V 1 1: 3.84 V	Voltage Detection 2 Level Select (Standard voltage during drop in voltage) b7 b4 1 0 0 1: 2.99 V (Vdet1_1) 1 0 1 0: 2.92 V (Vdet1_2) 1 0 1 1: 2.85 V (Vdet1_3) Settings other than above are prohibited.
		The Value after reset is different	
LVD1CR0	LVD1DFDIS	—	Voltage Monitoring 1 Digital Filter Disable Mode Select
	LVD1FSAMP [1:0]	—	Sampling Clock Select
LVD2CR0	LVD2DFDIS	—	Voltage Monitoring 2 Digital Filter Disable Mode Select
	LVD2FSAMP [1:0]	—	Sampling Clock Select
	LVD2RN	Voltage Monitoring 2 Reset Negate Select 0: Negation follows a stabilization time (tLVD2) after VCC or the CMPA2 pin > Vdet2 is detected. 1: Negation follows a stabilization time (tLVD2) after assertion of the voltage monitoring 2 reset.	Voltage Monitoring 2 Reset Negate Select 0: Negation follows a stabilization time (tLVD2) after VCC > Vdet2 is detected. 1: Negation follows a stabilization time (tLVD2) after assertion of the LVD2 reset.

2.7 Clock Generation Circuit

Table 2.12 shows a Comparative Listing of Clock Generation Circuit Specifications, and Table 2.13 shows a Comparative Listing of Clock Generation Circuit Registers.

Table 2.12 Comparative Listing of Clock Generation Circuit Specifications

Item	RX231	RX65N
Uses	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the MTU2. • Generates the peripheral module clock (PCLKB) to be supplied to peripheral modules. • Generates the peripheral module clock (PCLKD) to be supplied to S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the USB clock (UCLK) to be supplied to the USB. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANCLK) to be supplied to the CAN. • Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated low-speed clock (IWDTCLK) to be supplied to the IWDT. • Generates the SSI clock (SSISCK) to be supplied to the SSI. • Generates the LPT clock (LPTCLK) to be supplied to the LPT.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, RSPI, SCIi, MTU3, and AES. • Generates the peripheral module clock (PCLKB) to be supplied to peripheral modules. • Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD: unit 1) to be supplied to S12AD. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM. • Generates the USB clock (UCLK) to be supplied to the USBb. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.

Item	RX231	RX65N
Operating frequencies	• ICLK: 54 MHz (max.) • PCLKA: 54 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 54 MHz (max.) • FCLK: 1 to 32 MHz (for programming and erasing the ROM and E2 data flash) 32 MHz (max.) (for reading from the E2 data flash) • BCLK: 32 MHz (max.) • BCLK pin output: 16 MHz (max.) • UCLK: 48 MHz • CACCLK: Same frequency as each oscillator • CANCLK: 20 MHz (max.) • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • SSISCK: 20 MHz (max.) • LPTCLK: The same frequency as that of the selected oscillator	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz (max.) • FCLK: 4 MHz to 60 MHz (when programming or erasing the code flash memory or data flash memory)*1 60 MHz (max.) (for reading from the Data flash memory)*1 • BCLK: 120 MHz (max.) • BCLK pin output: 60 MHz (max.) • SDCLK pin output: 60 MHz (max.) • UCLK: 48 MHz (max.) • CACCLK: Same as the clock from respective oscillators • CANMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)
Main clock oscillator	• Resonator frequency: 1 to 20 MHz (VCC ≥ 2.4 V), 1 to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU output can be forcedly driven to high-impedance. • Drive capacity switching function	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pin: EXTAL, XTAL • Oscillation stop detection function: When an oscillation stop is detected with the main clock, the system clock source is switched to LOCO, and MTU3 output can be forcedly driven to the high-impedance. • Drive capacity switching function
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal • Connection pin: XCIN, XCOUT • Drive capacity switching function	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pin: XCIN, XCOUT • Drive capacity switching function

Item	RX231	RX65N
PLL frequency synthesizer	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 13.5 (increments of 0.5) • VCO oscillation frequency: 24 to 54 MHz (VCC ≥ 2.4 V)	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz
USB-dedicated PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4, 6, 8, and 12 MHz • Frequency multiplication ratio: Selectable from 4, 6, 8, and 12 • VCO oscillation frequency: 48 MHz (VCC ≥ 2.4 V)	—
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 and 54 MHz	• Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 120 kHz
JTAG external clock input (TCK)	—	Input clock frequency: 10 MHz (max.)
Control of output on BCLK pin	—	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable
Control of output on SDCLK pin	—	SDCLK clock output or high output is selectable
Event link function (output)	—	Detection of stopping of the main clock oscillator
Event link function (input)	—	Switching of the clock source to the low-speed on-chip oscillator

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

Table 2.13 Comparative Listing of Clock Generation Circuit Registers

Register	Bit	RX231	RX65N
SCKCR	PCKD[3:0]	Peripheral Module Clock D (PCLKD) Select The Value after reset is different.	
	PCKC[3:0]	—	Peripheral Module Clock C (PCLKC) Select
	PCKB[3:0]	Peripheral Module Clock B (PCLKB) Select The Value after reset is different.	
	PCKA[3:0]	Peripheral Module Clock A (PCLKA) Select The Value after reset is different.	
	BCK[3:0]	External Bus Clock (BCLK) Select The Value after reset is different.	
	PSTOP0	—	SDCLK Pin Output Control
SCKCR	ICK[3:0]	System Clock (ICLK) Select The Value after reset is different.	
	FCK[3:0]	Flash-IF Clock (FCLK) Select The Value after reset is different.	
ROMWT	—	—	ROM Wait Cycle Setting Register
SCKCR2	—	—	System Clock Control Register 2
PLLCR	PLIDIV[1:0]	PLL Input Frequency Division Ratio Select b1 b0 0 0: ×1 0 1: ×1/2 1 0: ×1/4 1 1: Setting prohibited	PLL Input Frequency Division Ratio Select b1 b0 0 0: ×1 0 1: ×1/2 1 0: ×1/3 1 1: Setting prohibited
	PLLSRCSEL	—	PLL Clock Source Select
	STC[5:0]	Frequency Multiplication Factor Select b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 : : : 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13 0 1 1 0 1 0: ×13.5 Settings other than above are prohibited.	Frequency Multiplication Factor Select b13 b8 0 1 0 0 1 1: ×10.0 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11.0 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12.0 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13.0 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14.0 : : : 1 1 1 0 0 1: ×29.0 1 1 1 0 1 0: ×29.5 1 1 1 0 1 1: ×30.0 Settings other than above are prohibited.
		The Value after reset is different.	
UPLLCR	—	USB-dedicated PLL Control Register	—

Register	Bit	RX231	RX65N
UPLLCR2	—	USB-dedicated PLL Control Register 2	—
HOCOCR2	HCFRQ[1:0]	HOCO Frequency Setting b1 b0 0 0: 32 MHz 1 1: 54 MHz Settings other than above are prohibited.	HOCO Frequency Setting b1 b0 0 0: 16 MHz 0 1: 18 MHz 1 0: 20 MHz Settings other than above are prohibited.
OSCOVFSR	MOOVF	Main Clock Oscillation Stabilization Flag 0: Main clock is stopped 1: Oscillation is stable and the clock can be used as the system clock	Main Clock Oscillation Stabilization Flag 0: MOSTP = 1 (stopping the main clock oscillator) or oscillation of the main clock has not yet become stable 1: Oscillation of the main clock is stable so the clock is available for use as the system clock
	SOOVF	—	Sub-Clock Oscillation Stabilization Flag
	ILCOVF	—	IWDT-Dedicated Clock Oscillation Stabilization Flag
	UPLOVF	USB-Dedicated PLL Clock Oscillation Stabilization Flag	—
MOSCWTCR	MSTS[4:0]: RX231 MSTS[7:0]: RX65N	Main Clock Oscillator Wait Time (b4 to b0)	Main Clock Oscillator Wait Time (b7 to b0)
		The Value after reset is different.	
SOSCWTCR	—	—	Sub-Clock Oscillator Wait Control Register
CKOCR	—	CLKOUT Output Control Register	—
MOFCR	MOFXIN	—	Main Clock Oscillator Forced Oscillation
	MODRV2 [1:0]	—	Main Clock Oscillator Driving Ability 2 Switching
	MODRV21	Main Clock Oscillator Drive Capability Switch	—
HOCOPCR	—	—	High-Speed On-Chip Oscillator Power Supply Control Register
MEMWAIT	—	Memory Wait Cycle Setting Register	—
LOCOTRR	—	Low-Speed On-Chip Oscillator Trimming Register	—
ILOCOTRR	—	IWDT-Dedicated On-Chip Oscillator Trimming Register	—
HOCOTRRn	—	High-Speed On-Chip Oscillator Trimming Register n (n = 0, 3)	—

2.8 Low Power Consumption

Table 2.14 shows a Comparative Listing of Low Power Consumption Specifications, Table 2.15 is a Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.16 is a Comparative Listing of Low Power Consumption Registers.

Table 2.14 Comparative Listing of Low Power Consumption Specifications

Item	RX231	RX65N
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), high speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), external bus clock (BCLK), and FlashIF clock (FCLK).	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).
BCLK output control function	—	BCLK output or high-level output can be selected.
SDCLK output control function	—	SDCLK output or high-level output can be selected.
Module-stop function	Each peripheral module can be stopped independently by the module stop control register.	Functions can be stopped independently for each peripheral module.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • Deep sleep mode • Software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Three operating power control modes are available — High-speed operating mode — Middle-speed operating mode — Low-speed operating mode	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage range. • Three operating power control modes — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2 There is no difference in power consumption when the same conditions (frequency and voltage) are set in low-speed operating modes 1 and 2.

Table 2.15 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX231	RX65N
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	USB-dedicated PLL	Operation possible	—
	CPU	Stopped (retained)	Stopped (retained)
	RAM (0000 0000h to 0000 FFFFh): RX231 RAM, expansion RAM: RX65N	Operation possible (retained)	Operation possible (retained)
	DMAC	Operation possible	—
	DTC	Operation possible	—
	Standby RAM	—	Operation possible (retained)
	Flash memory	Operation	Operation
	USB FS Host/Function module (USBb)	—	Operation possible
	Watchdog timer (WDT: RX231, WDTA: RX65N)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Low-power timer (LPT)	Operation possible	—
	8-bit timer (unit 0, unit 1) (TMR)	—	Operation possible
	Port output enable (POE)	—	Operation possible
	Voltage detection circuit (LVD: RX231, LVDA: RX65N)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	RTCOUT output	Operation possible	—
	CLKOUT output	Operation possible	—
	Comparator B	Operation possible	—

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX231	RX65N
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	USB-dedicated PLL	Stopped	—
	CPU	Stopped (retained)	Stopped (retained)
	RAM (0000 0000h to 0000 FFFFh): RX231 RAM, expansion RAM: RX65N	Stopped (retained)	Stopped (retained)
	DMAC	Stopped (retained)	—
	DTC	Stopped (retained)	—
	Standby RAM	—	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB FS Host/Function module (USBb)	—	Stopped
	Watchdog timer (WDT: RX231, WDTA: RX65N)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Low-power timer (LPT)	Operation possible	—
	8-bit timer (unit 0, unit 1) (TMR)	—	Stopped (retained)
	Port output enable (POE)	—	Stopped (retained)
	Voltage detection circuit (LVD: RX231, LVDA: RX65N)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
	RTCOUT output	Operation possible	—
	CLKOUT output	Operation possible	—
	Comparator B	Operation possible	—

Notes: "Operation possible" means that whether the state is operating or stopped is controlled by the control register setting.
"Stopped (retained)" means that internal register values are retained and internal operations are suspended.
"Stopped (undefined)" means that internal register values are undefined and power is not supplied to the internal circuit.

Table 2.16 Comparative Listing of Low Power Consumption Registers

Register	Bit	RX231	RX65N
SBYCR	OPE	Output Port Enable 0: In software standby mode, the address bus and bus control signals are set to the high-impedance state 1: In software standby mode, the address bus and bus control signals retain the output state	Output Port Enable 0: In software standby mode or deep software standby mode, the address bus and bus control signals are set to the high-impedance state 1: In software standby mode or deep software standby mode, the address bus and bus control signals retain the output state
	SSBY	Software Standby 0: Set entry to sleep mode or deep sleep mode after the WAIT instruction is executed 1: Set entry to software standby mode after the WAIT instruction is executed	Software Standby 0: Shifts to sleep mode or all-module clock stop mode after the WAIT instruction is executed 1: Shifts to software standby mode after the WAIT instruction is executed
MSTPCRA	MSTPA0	—	Compare Match Timer W (Unit 1) Module Stop
	MSTPA1	—	Compare Match Timer W (Unit 0) Module Stop
	MSTPA9	Multifunction Timer Pulse Unit 2 Module Stop Target module: MTU2 (MTU0 to MTU5)	Multifunction Timer Pulse Unit 3 Module Stop Target module: MTU3 (MTU0 to MTU8)
	MSTPA10	—	Programmable Pulse Generator (Unit 1) Module Stop
	MSTPA11	—	Programmable Pulse Generator (Unit 0) Module Stop
	MSTPA16	—	12-bit A/D Converter (Unit 1) Module Stop
	MSTPA24	—	Module Stop A24
	MSTPA27	—	Module Stop A27
	MSTPA29	—	EXDMA Controller Module Stop
	ACSE	—	All-Module Clock Stop Mode Enable
MSTPCRB	MSTPB0	RCAN0 Module Stop Target module: RCAN0	CAN Module 0 Module Stop Target module: CAN0
	MSTPB1	—	CAN Module 1 Module Stop
	MSTPB8	—	Temperature Sensor Module Stop
	MSTPB10	Comparator B Module Stop	—
	MSTPB15	—	Ethernet Controller and Ethernet Controller DMA Controller (Channel 0) Modules Stop
	MSTPB16	—	Serial Peripheral Interface 1 Module Stop
	MSTPB20	—	I^2C Bus Interface 1 Module Stop*1

Register	Bit	RX231	RX65N
MSTPCRB	MSTPB22	—	Parallel Data Capture Unit Module Stop
	MSTPB24	—	Serial Communication Interface 7 Module Stop
	MSTPB27	—	Serial Communication Interface 4 Module Stop
	MSTPB28	—	Serial Communication Interface 3 Module Stop
	MSTPB29	—	Serial Communication Interface 2 Module Stop
MSTPCRC	MSTPC2	—	Expansion RAM Module Stop*1
	MSTPC7	—	Standby RAM Module Stop
	MSTPC17	—	I^2C Bus Interface 2 Module Stop
	MSTPC20	IrDA Module Stop	—
	MSTPC22	—	Serial Peripheral Interface 2 Module Stop
	MSTPC23	—	Quad Serial Peripheral Interface Module Stop
	MSTPC24	—	Serial Communications Interface 11 Module Stop
	MSTPC25	—	Serial Communications Interface 10 Module Stop
	MSTPC28	—	2D drawing engine Module Stop*1
	MSTPC29	—	Graphic-LCD controller Module Stop*1
	DSLPE	Deep Sleep Mode Enable	—
MSTPCRD	MSTPD0	—	Module Stop D0
	MSTPD1	—	Module Stop D1
	MSTPD2	—	Module Stop D2
	MSTPD3	—	Module Stop D3
	MSTPD4	—	Module Stop D4
	MSTPD5	—	Module Stop D5
	MSTPD6	—	Module Stop D6
	MSTPD7	—	Module Stop D7
	MSTPD10	Touch Sensor Control Unit Module Stop	—
	MSTPD13	—	SD Slave Interface Module Stop
	MSTPD15	Serial Sound Interface Module Stop	—
	MSTPD21	—	MMC Host Interface Module Stop
	MSTPD27	—	Trusted Secure IP Module Stop*1
	MSTPD31	Security Function	—

Register	Bit	RX231	RX65N
OPCCR	OPCM[2:0]	Operating Power Control Mode Select b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode Settings other than above are prohibited.	Operating Power Control Mode Select b2 b0 0 0 0: High-speed operating mode 1 1 0: Low-speed operating mode 1 1 1 1: Low-speed operating mode 2 Settings other than above are prohibited.
		The Value after reset is different.	
SOPCCR	—	Sub Operating Power Control Register	—
RSTCKCR	RSTCKSEL [2:0]	Sleep Mode Return Clock Source Select b2 b0 0 0 0: LOCO is selected 0 0 1: HOCO is selected 0 1 0: Main clock oscillator is selected Settings other than above are prohibited when the RSTCKEN bit is 1.	Sleep Mode Return Clock Source Select b2 b0 0 0 1: HOCO is selected 0 1 0: Main clock oscillator is selected Settings other than above are prohibited while the RSTCKEN bit is 1.
DPSBYCR	—	—	Deep Standby Control Register
DPSIER0	—	—	Deep Standby Interrupt Enable Register 0
DPSIER1	—	—	Deep Standby Interrupt Enable Register 1
DPSIER2	—	—	Deep Standby Interrupt Enable Register 2
DPSIER3	—	—	Deep Standby Interrupt Enable Register 3
DPSIFR0	—	—	Deep Standby Interrupt Flag Register 0
DPSIFR1	—	—	Deep Standby Interrupt Flag Register 1
DPSIFR2	—	—	Deep Standby Interrupt Flag Register 2
DPSIFR3	—	—	Deep Standby Interrupt Flag Register 3
DPSIEGR0	—	—	Deep Standby Interrupt Edge Register 0
DPSIEGR1	—	—	Deep Standby Interrupt Edge Register 1
DPSIEGR2	—	—	Deep Standby Interrupt Edge Register 2
DPSIEGR3	—	—	Deep Standby Interrupt Edge Register 3

Register	Bit	RX231	RX65N
DPSBKRy	—	—	Deep Standby Backup Register (y = 0 to 31)

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

2.9 Battery Backup Function

Table 2.17 shows a Comparative Listing of Battery Backup Function Registers.

Table 2.17 Comparative Listing of Battery Backup Function Registers

Item	RX231	RX65N
VBATTCR	VBATT Control Register	—
VBATTSR	VBATT Status Register	—
VBTLVDICR	VBATT Pin Voltage Drop Detection Interrupt Control Register	—

2.10 Register Write Protection Function

Table 2.18 shows a Comparative Listing of Register Write Protection Function Specifications, and Table 2.19 shows a Comparative Listing of Register Write Protection Function Registers.

Table 2.18 Comparative Listing of Register Write Protection Function Specifications

Item	RX231	RX65N
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, CKOCR, UPLLCR, UPLLCR2, BCKCR, HOCOCR2, MEMWAIT, LOCOTRR, ILOCOTRR, HOCOTRR0, HOCOTRR3	Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR
PRC1 bit	• Register related to the operating modes: SYSCR0, SYSCR1 • Registers related to low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR3 • Registers related to clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR
PRC2 bit	Registers related to the low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR	—
PRC3 bit	• Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR • Registers related to the battery backup function: VBATTCR, VBATTSR, VBTLVDICR	Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.19 Comparative Listing of Register Write Protection Function Registers

Register	Bit	RX231	RX65N
PRCR	PRC2	Enables writing to the registers related to the low power timer.	—
	PRC3	Enables writing to the registers related to the LVD and the battery backup function.	Enables writing to the registers related to the LVD.

2.11 Interrupt Controller

Table 2.20 shows a Comparative Listing of Interrupt Controller Specifications, and Table 2.21 shows a Comparative Listing of Interrupt Controller Registers.

Table 2.20 Comparative Listing of Interrupt Controller Specifications

Item		RX231 (ICUb)	RX65N (ICUB)
Interrupt	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection (detection method is fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as an interrupt source. — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.

Item		RX231 (ICUb)	RX65N (ICUB)
Interrupt	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges. One of these detection methods can be set for each source. • Digital filter function: Supported	• Interrupts from signals input to IRQi pins (i = 0 to 15) • Number of sources:16 • Interrupt detection method: Detection of low level, falling edge, rising edge, rising and falling edges. One of these detection methods can be set for each source. • Digital filter can be used to remove noise.
	Software interrupt	• Interrupt generated by writing to a register. • One interrupt source	• Interrupt request can be generated by writing to a register. • Two interrupt sources
	Event link interrupt	The ELSR8I, ELSR18I or ELSR19I interrupt is generated by an ELC event	—
	Interrupt priority level	Specified by registers.	Priority level can be set with interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	Faster interrupt processing of the CPU can be set only for a single interrupt source.	CPU interrupt response time can be reduced. This function can be used for only one interrupt source.
	DTC and DMAC control	The DTC and DMAC can be activated by interrupt sources.	Interrupt sources can be used to start the DTC and DMAC.
	EXDMAC control	—	• Interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. • Interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported	• Interrupt by the input signal to the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter can be used to remove noise.
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	This interrupt occurs when the main clock oscillator stop is detected.
	WDT underflow/ refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	This interrupt occurs when the watchdog timer (WDT) underflows or a refresh error occurs.

Item		RX231 (ICUb)	RX65N (ICUB)
Non-maskable interrupts	IWDT underflow/ refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	This interrupt occurs when the independent watchdog timer (IWDT) underflows or a refresh error occurs.
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	—	This interrupt occurs when a parity check error is detected in the RAM.
	VBATT voltage monitoring interrupt	Voltage monitoring interrupt of the VBATT	—
Return from low power consumption modes	Sleep mode	Return is initiated by non-maskable interrupts or any other interrupt source.	Exit sleep mode by any interrupt source.
	Deep sleep mode	Return is initiated by non-maskable interrupts or any other interrupt source.	—
	All-module clock stop mode	—	Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, RTC alarm, RTC period, IWDT, software configurable interrupt 146 to 157).
	Software standby mode	Return is initiated by non-maskable interrupts, IRQ0 to IRQ7 interrupts, or RTC alarm/periodic interrupts.	Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period, IWDT).
	Deep software standby mode	—	Exit all-module clock stop mode by the NMI pin interrupt, specific external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period).

Table 2.21 Comparative Listing of Interrupt Controller Registers

Register	Bit	RX231 (ICUb)	RX65N (ICUB)
SWINT2R	—	—	Software Interrupt 2 Generation Register
DTCERn	—	DTC Transfer Request Enable Register n (n = 027 to 255)	DTC Transfer Request Enable Register n (n = 026 to 255)
IRQCRi	—	IRQ Control Register i (i = 0 to 7)	IRQ Control Register i (i = 0 to 15)
IRQFLTE1	—	—	IRQ Pin Digital Filter Enable Register 1
IRQFLTC1	—	—	IRQ Pin Digital Filter Setting Register 1
NMISR	RAMST	—	RAM Error Interrupt Status Flag
	VBATST	VBATT Voltage Monitoring Interrupt Status Flag	—
NMIER	RAMEN	—	RAM Error Interrupt Enable
	VBATEN	VBATT Voltage Monitoring Interrupt Enable	—
NMICLR	VBATCLR	VBAT Clear	—
GRPBE0	—	—	Group BE0 Interrupt Request Register
GRPBL0	—	—	Group BL0 Interrupt Request Register
GRPBL1	—	—	Group BL1 Interrupt Request Register
GRPBL2	—	—	Group BL2 Interrupt Request Register
GRPAL0	—	—	Group AL0 Interrupt Request Register
GRPAL1	—	—	Group AL1 Interrupt Request Register
GENBE0	—	—	Group BE0 Interrupt Request Enable Register
GENBL0	—	—	Group BL0 Interrupt Request Enable Register
GENBL1	—	—	Group BL1 Interrupt Request Enable Register
GENBL2	—	—	Group BL2 Interrupt Request Enable Register
GENAL0	—	—	Group AL0 Interrupt Request Enable Register
GENAL1	—	—	Group AL1 Interrupt Request Enable Register
GCRBE0	—	—	Group BE0 Interrupt Clear Register
PIBRk	—	—	Software Configurable Interrupt B Request Register k (k = 0h to Ah)
PIARk	—	—	Software Configurable Interrupt A Request Register k (k = 0h to 5h, Bh)
SLIBXRn	—	—	Software Configurable Interrupt B Source Select Register Xn (n = 128 to 143)

Register	Bit	RX231 (ICUb)	RX65N (ICUB)
SLIBRn	—	—	Software Configurable Interrupt B Source Select Register n (n = 144 to 207)
SLIARn	—	—	Software Configurable Interrupt A Source Select Register n (n = 208 to 255)
SELEXDR	—	—	EXDMAC Trigger Select Register
SLIPRCR	—	—	Software Configurable Interrupt Source Select Register Write Protect Register

2.12 Buses

Table 2.22 shows a Comparative Listing of Bus Specifications, Table 2.23 shows a Comparative Listing of External Bus Specifications, and Table 2.24 shows a Comparative Listing of Bus Registers.

Table 2.22 Comparative Listing of Bus Specifications

Bus Type		RX231	RX65N
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, expansion RAM*1, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, expansion RAM*1, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to code flash memory
	Memory bus 3	—	Connected to expansion RAM*1
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DMAC and DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DMAC, DTC, EDMAC, SDSI, GLCDC*1, and DRW2D*1 • Connected to on-chip memory (RAM, expansion RAM*1, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EDMAC operates in synchronization with the BCLK)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)

Bus Type		RX231	RX65N
Internal peripheral buses	Internal peripheral bus 3	• Connected to peripheral modules (USB0, CAN, and CTSU) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (USBb, PDC, and standby RAM) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU2) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (EDMAC, ETHERC, MTU3, SCIi, RSPI, and AES) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 5	Reserved area	• Connected to peripheral modules (GLCDC, DRW2D)*1 • Operates in synchronization with the peripheral-module clock (PCLKA)*1
	Internal peripheral bus 6	• Connected to the flash control module and E2 data flash • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash (in P/E) and data flash memory*1 • Operates in synchronization with the FlashIF clock (FCLK)
External bus CS area	CS area	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK)	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK)
	SDRAM area	—	• Connected to the SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

Table 2.23 Comparative Listing of External Bus Specifications

Item	RX231	RX65N
External address space	• An external address space is divided into four CS areas (CS0 to CS3) for management. • Chip select signals can be output for each area. • Bus width can be set for each area. — Separate bus: An 8- or 16-bit bus space is selectable. — Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • An endian mode can be specified for each area.	• An external address space is divided into eight CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management. • Chip select signals can be output for each area. • Bus width can be set for each area. — Separate bus: An 8- or 16-, or 32-bit*1 bus space is selectable. — Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • An endian mode can be specified for each area.

Item	RX231	RX65N
CS area controller	• Recovery cycles can be inserted. — Read recovery: Up to 15 cycles — Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles) • Wait control can be used to set up the following. — Timing of assertion and negation for chip-select signals (CS0# to CS3#) — The timing of assertion of the read signal (RD#) and write signals (WR0#/WR# and WR1#) — The timing with which data output starts and ends • Write access mode: Single write strobe mode/byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area	• Recovery cycles can be inserted. — Read recovery: Up to 15 cycles — Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles) • Wait control can be used to set up the following. — Timing of assertion and negation for chip-select signals (CS0# to CS7#) — The timing of assertion of the read signal (RD#) and write signals (WR0#/WR# and WR1# to WR3#*1) — The timing with which data output starts and ends • Write access mode: Single write strobe mode/byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area
SDRAM area controller	—	• Multiplexing output of row address/column address (8, 9, 10, or 11 bits) • Self-refresh and auto-Refresh selectable • CAS latency can be specified from one to three cycles
Write buffer function	When write data from the bus master has been written to the write buffer, write access by the bus master is completed.	When write data from the bus master has been written to the write buffer, write access by the bus master is completed.
Frequency	The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK).	• The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK)*2. • The SDRAM area controller (SDRAMC) operates in synchronization with the SDRAM clock (SDCLK).

Notes: 1. Can be used for products with at least 1.5 MB of code flash memory.
2. The BCLK and the SDCLK should be operated with the same frequency when the SDRAM is in use.

Table 2.24 Comparative Listing of Bus Registers

Register	Bit	RX231	RX65N
CSnCR	—	CSn Control Register (n = 0 to 3)	CSn Control Register (n = 0 to 7)
	BSIZE[1:0]	External Bus Width Select b5b4 0 0: A 16-bit bus space is selected 0 1: Setting prohibited 1 0: An 8-bit bus space is selected 1 1: Setting prohibited	External Bus Width Select b5b4 0 0: A 16-bit bus space is selected 0 1: Setting prohibited/ A 32-bit bus space is selected*1 1 0: An 8-bit bus space is selected 1 1: Setting prohibited
CSnREC	—	CSn Recovery Cycle Register (n = 0 to 3)	CSn Recovery Cycle Register (n = 0 to 7)
CSnMOD	—	CSn Mode Register (n = 0 to 3)	CSn Mode Register (n = 0 to 7)
CSnWCR1	—	CSn Wait Control Register 1 (n = 0 to 3)	CSn Wait Control Register 1 (n = 0 to 7)
CSnWCR2	—	CSn Wait Control Register 2 (n = 0 to 3)	CSn Wait Control Register 2 (n = 0 to 7)
SDCCR	—	—	SDC Control Register
SDCMOD	—	—	SDC Mode Register
SDAMOD	—	—	SDRAM Access Mode Register
SDSELF	—	—	SDRAM Self-Refresh Control Register
SDRFCR	—	—	SDRAM Refresh Control Register
SDRFEN	—	—	SDRAM Auto-Refresh Control Register
SDICR	—	—	SDRAM Initialization Sequence Control Register
SDIR	—	—	SDRAM Initialization Register
SDADR	—	—	SDRAM Address Register
SDTR	—	—	SDRAM Timing Register
SDMOD	—	—	SDRAM Mode Register
SDSR	—	—	SDRAM Status Register
BERSR1	MST[2:0]	Bus Master Code b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	Bus Master Code b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Extended bus master 1 1 1: EXDMAC
EBMAPCR	—	—	Extended bus master priority control register*1

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

2.13 DMA Controller

Table 2.25 shows a Comparative Listing of DMA Controller Specifications, and Table 2.26 shows a Comparative Listing of DMA Controller Registers.

Table 2.25 Comparative Listing of DMA Controller Specifications

Item		RX231 (DMACA)	RX65N (DMACAa)
Number of channels		4 (DMACm (m = 0 to 3))	8 (DMACm (m = 0 to 7))
Transfer space		512 MB (00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh, excluding reserved areas)	512 MB (00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh, excluding reserved areas)
Maximum transfer data count		1M data (Maximum number of transfers in block transfer mode: 1,024 data × 1,024 blocks)	64 MB (Maximum number of transfers in block transfer mode: 1,024 data × 65,536 blocks)
DMAC request sources		Activation source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins	Request source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins
Channel priority		Channel 0 > Channel 1 > Channel 2 > Channel 3 (Channel 0: highest)	Channel 0 > Channel 1 > Channel 2 > Channel 3 ... > Channel 7 (Channel 0: highest)
Transfer data	1 data unit	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32 bits
	Block size	Number of data: 1 to 1,024	Number of data: 1 to 1,024
Transfer modes	Normal transfer mode	• One data transfer by one DMA transfer request • Free running mode (setting in which total number of data transfers is not specified) settable	• One data transfer by one DMA transfer request • Free running mode (setting in which total number of data transfers is not specified) settable
	Repeat transfer mode	• One data transfer by one DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination • Maximum settable repeat size: 1,024	• One data transfer by one DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination • Maximum settable repeat size: 1,024
	Block transfer mode	• One block data transfer by one DMA transfer request • Maximum settable block size: 1,024 data	• One block data transfer by one DMA transfer request • Maximum settable block size: 1,024 data

Item		RX231 (DMACA)	RX65N (DMACAa)
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source and destination	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source and destination
Interrupt request	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.	Generated on completion of transferring data volume specified by the transfer counter.
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.
Event link function		Event link request is generated after one data transfer (for block, after one block transfer).	An event link request is generated after each data transfer (for block transfer, after each block is transferred).
Power consumption reduction function		Module stop state can be set.	Module-stop state can be set.

Table 2.26 Comparative Listing of DMA Controller Registers

Register	Bit	RX231 (DMACA)	RX65N (DMACAa)
DMCRB	—	DMA Block Transfer Count Register (b9 to b0)	DMA Block Transfer Count Register (b15 to b0)
DMIST	—	—	DMAC74 Interrupt Status Monitor Register

2.14 Data Transfer Controller

Table 2.27 shows a Comparative Listing of Data Transfer Controller Specifications, and Table 2.28 shows a Comparative Listing of Data Transfer Controller Registers.

Table 2.27 Comparative Listing of Data Transfer Controller Specifications

Item	RX231 (DTCa)	RX65N (DTCb)
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block. — The maximum block size is 256 × 32 bits = 1024 bytes.	• Normal transfer mode A single transfer request leads to a single data transfer. • Repeat transfer mode — A single transfer request leads to a single data transfer. — The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1024 bytes. • Block transfer mode — A single transfer request leads to the transfer of a single block. — The maximum block size is 256 × 32 bits = 1024 bytes.
Transfer channels	• Channel transfer corresponding to the interrupt source is possible (transferred by the DTC activation request from the ICU). • Multiple data can be transferred on a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.	• Channel transfer corresponding to the interrupt source is possible (transferred by the DTC activation request from the ICU). • Multiple data can be transferred on a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.
Transfer space	• In short-address mode: 16 MB (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 GB (Area from 0000 0000h to FFFF FFFFh except reserved areas)	• In short-address mode: 16 MB (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 GB (Area from 0000 0000h to FFFF FFFFh except reserved areas)
Data transfer units	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data
CPU interrupt requests	• An interrupt request can be generated to the CPU on a DTC activation interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.	• An interrupt request can be generated to the CPU on a request source for a data transfer. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.

Item	RX231 (DTCa)	RX65N (DTCb)
Event link activation	An event link request is generated after one data transfer (for block, after one block transfer).	An event link request is generated after one data transfer (for block, after one block transfer).
Read skip	Transfer information read skip can be executed.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	When “fixed” is selected for transfer source address or transfer destination address, write-back skip is executed.	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	—	Allows disabling the write-back of transfer information.
Chain transfer	• Multiple types of data transfers can sequentially be executed in response to a single request. • Either “performed only when the transfer counter becomes 0” or “every time” can be selected.	• Multiple types of data transfers can sequentially be executed in response to a single request. • Either “performed only when the transfer counter becomes 0” or “every time” can be selected.
Sequence transfer	—	• A series of complicated transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one trigger source can be set at a time. • Up to 256 sequences for a single trigger source • The data that is initially transferred in response to a transfer request determines a sequence • The whole sequence can be executed on a single request, or be suspended in the middle of the sequence and resumed on the next transfer request (division of sequence).
Displacement addition	—	The displacement value can be added to the transfer source address (for each transfer information)
Low power consumption function	Module stop state can be set.	It is possible to specify the module stop state.

Table 2.28 Comparative Listing of Data Transfer Controller Registers

Register	Bit	RX231 (DTCa)	RX65N (DTCb)
MRA	WBDIS	—	Write-back Disable
MRB	SQEND	—	Sequence Transfer End
	INDX	—	Index Table Reference
MRC	—	—	DTC Mode Register C
DTCIBR	—	—	DTC Index Table Base Register
DTCOR	—	—	DTC Operation Register
DTCSQE	—	—	DTC Sequence Transfer Enable Register
DTCDISP	—	—	DTC Address Displacement Register

2.15 Event Link Controller

Table 2.29 shows a Comparative Listing of Event Link Controller Specifications, Table 2.30 shows a Comparative Listing of Event Link Controller Registers, and Table 2.31 shows Correspondence between the ELSRn Register and the Peripheral Modules.

Table 2.29 Comparative Listing of Event Link Controller Specifications

Item	RX231 (ELC)	RX65N (ELC)
Event link function	• 63 types of event signals can be directly connected to modules. • The operation of timer modules can be selected when an event is input to the timer module. • Event link operation is possible for port B and port E. — Single port: An event link can be set for a single bit specified in a port. — Port group: An event link can be set for a group of single bits specified within eight I/O ports.	• 82 event signals can be linked to peripheral modules directly. • The operation of peripheral timer modules at event signal input is selectable. • Event link operation on port B or port E is supported. — Single port: Event link operation can be enabled for a single specified port. — Port group: Event link operation can be enabled for multiple specified ports within a group of up to eight ports.
Low power consumption function	Module stop state can be set.	Ability to transition to module stop state.

Table 2.30 Comparative Listing of Event Link Controller Registers

Register	Bit	RX231 (ELC)	RX65N (ELC)
ELSRn	—	Event Link Setting Register n (n = 1 to 4, 7, 8, 10, 12, 14 to 16, 18 to 29)	Event Link Setting Register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, 45)
	ELS[7:0]	Event Link Select b7 b0 00000000: Event output to the corresponding peripheral module is disabled. 00001000 to 01101010: Set the number for the event signal to be linked. Settings other than above are prohibited.	Event Link Select b7 b0 00000000: Event output to the corresponding peripheral module is disabled. 00000001 to 10111101: Set the number for the event signal to be linked. Settings other than above are prohibited.
ELOPA	MTU0MD[1:0]	—	MTU0 Operation Select
	MTU1MD[1:0]	MTU1 Operation Select	—
	MTU2MD[1:0]	MTU2 Operation Select	—
ELOPC	LPTMD[1:0]	LPT Operation Select	—
ELOPD	TMR1MD[1:0]	—	TMR1 Operation Select
	TMR3MD[1:0]	—	TMR3 Operation Select
ELOPF	—	—	Event Link Option Setting Register F
ELOPH	—	—	Event Link Option Setting Register H

Table 2.31 Correspondence between the ELSRn Register and the Peripheral Modules

Register	RX231	RX65N
ELSR0	—	MTU0
ELSR1	MTU1	—
ELSR2	MTU2	—
ELSR3	MTU3	MTU3
ELSR4	MTU4	MTU4
ELSR7	CMT1	CMT1
ELSR8	ICU (LPT dedicated interrupt)	—
ELSR10	TMR0	TMR0
ELSR11	—	TMR1
ELSR12	TMR2	TMR2
ELSR13	—	TMR3
ELSR14	CTSU	—
ELSR15	S12AD	S12AD
ELSR16	DA0	DA0
ELSR18	ICU (Interrupt 1)	ICU (Interrupt 1)
ELSR19	ICU (Interrupt 2)	ICU (Interrupt 2)
ELSR20	Output port group 1	Output port group 1
ELSR21	Output port group 2	Output port group 2
ELSR22	Input port group 1	Input port group 1
ELSR23	Input port group 2	Input port group 2
ELSR24	Single port 0	Single port 0
ELSR25	Single port 1	Single port 1
ELSR26	Single port 2	Single port 2
ELSR27	Single port 3	Single port 3
ELSR28	Clock source switching to LOCO	Clock source switching to LOCO
ELSR29	POE	—
ELSR33	—	CMTW0
ELSR35	—	TPU0
ELSR36	—	TPU1
ELSR37	—	TPU2
ELSR38	—	TPU3
ELSR45	—	S12AD1

2.16 I/O Ports

Table 2.32 and Table 2.33 show a Comparative Listing of I/O Ports Specifications for each package, and Table 2.34 shows a Comparative Listing of I/O Port Registers.

Table 2.32 Comparative Listing of I/O Ports (100-Pin) Specifications

Port	RX231 (100-Pin)	RX65N (100-Pin)
PORT0	P03, P05, P07	P05, P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTH	PH0 to PE3	—
PORTJ	PJ3	PJ3

Table 2.33 Comparative Listing of I/O Ports (64-Pin) Specifications

Port	RX231 (64-Pin)	RX651 (64-Pin)*1
PORT0	P03, P05	P05
PORT1	P14 to P17	P12, P13, P16, P17
PORT2	P26, P27	P26, P27
PORT3	P30, P31, P35 to P37	P30, P31, P34 to P37
PORT4	P40, P44, P46	P40 to P43
PORT5	P54, P55	P53
PORTA	PA0, PA1, PA3, PA4, PA6	PA1, PA2, PA4, PA6, PA7
PORTB	PB0, PB1, PB3, PB5 to PB7	PB5 to PB7
PORTC	PC2 to PC7	PC0, PC1, PC4 to PC7
PORTD	—	PD2 to PD7
PORTE	PE0 to PE5	PE0 to PE2, PE6, PE7
PORTH	PH0 to PH3	—
PORTJ	—	—

Note: 1. The RX65N is not available in 64-pin package versions.

Table 2.34 Comparative Listing of I/O Port Registers

Register	Bit	RX231	RX65N
ODR0	B2, B3	Pm1 Output Type Select For pins other than the port PE1 pin b2 0: CMOS output 1: N-channel open-drain b3 This bit is read as 0. The write value should be 0. PE1 b3 b2 0 0: CMOS output 0 1: N-channel open-drain 1 0: P-channel open-drain 1 1: Hi-Z	Pm1 Output Type Select For pins other than the port PE1 pin b2 0: CMOS output 1: N-channel open-drain b3 This bit is read as 0. The write value should be 0. For port PE1 pin b3 b2 0 0: CMOS output 0 1: NMOS open-drain output 1 0: PMOS open-drain output 1 1: Setting prohibited
PSRA	—	Port switching register A	—
PSRB	—	Port switching register B	—
DSCR2	—	—	Drive Capacity Control Register 2

2.17 Multi-Function Pin Controller

Table 2.35 shows a Comparative Listing of Realtime Clock Registers.

Table 2.35 Comparative Listing of Multi-Function Pin Controller Registers

Register	Bit	RX231 (MPC)	RX65N (MPC)
PmnPFS	—	Refer to the user's manual for descriptions of the pin function control registers.	
PFCSS0	—	—	CS Output Pin Select Register 0
PFCSS1	—	—	CS Output Pin Select Register 1
PFBCR0	ADRHMS	—	A16 to A23 Output Enable
	ADRHMS2	—	A18 to A20 Output Enable
	BCLKO	—	BCLK forced output bit
	DH32E	—	D16 to D31 Output Enable*1
	WR32BC32E	—	WR3#/BC3# and WR2#/BC2# Output Enable*1
PFBCR1	ALES	—	ALE select bit
	MDSDE	—	SDRAM Pin Enable
	DQM1E	—	DQM1 Enable
	SDCLKE	—	SDCLK Enable
PFBCR2	—	—	External Bus Control Register 2*1
PFBCR3	—	—	External Bus Control Register 3*1
PFENET	—	—	Ethernet Control Register

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

2.18 16-Bit Timer Pulse Unit

Table 2.36 shows a Comparative Listing of 16-Bit Timer Pulse Unit Specifications.

Table 2.36 Comparative Listing of 16-Bit Timer Pulse Unit Specifications

Item	RX231 (TPUa)	RX65N (TPUa)
Pulse input/output	Maximum 16	Maximum 16
Count clocks	Seven or eight types are provided for each channel.	Seven or eight types are provided for each channel.
Available operations	• Waveform output at compare match • Input capture function (noise filters can be set) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match and input capture • Synchronous input/output for registers by counter synchronous operation • Maximum of 15-phase PWM output by combination with synchronous operation • Cascaded operation	• Waveform output at compare match • Input capture function (noise filters can be set) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match and input capture • Synchronous input/output for registers by counter synchronous operation • Maximum of 15-phase PWM output by combination with synchronous operation • Cascaded operation
Buffer operation	• Channels 0, 3 • Automatic transfer of register data	• Channels 0 and 3 • Automatic transfer of register data
Phase coefficient mode	Channels 1, 2, 4, 5	Channels 1, 2, 4, and 5
Interrupt sources	26 sources	26 sources
Generation of trigger	—	Programmable pulse generator (PPG) output trigger can be generated.
	Conversion start trigger for the A/D converter can be generated.	Conversion start trigger for the A/D converter can be generated.
Event link function (output)	—	Six types of event signal can be output to the ELC. • Compare match A (TPU0 to TPU3) • Compare match B (TPU0 to TPU3) • Compare match C (TPU0, TPU3) • Compare match D (TPU0, TPU3) • Overflow (TPU0 to TPU3) • Underflow (TPU1, TPU2)
Event link function (input)	—	Any of the three operations in response to event input is possible. • Starting counts (TPU0 to TPU3) • Restarting counts (TPU0 to TPU3) • Input capture operation (TPU0 to TPU3)
Low power consumption function	Module stop state can be set.	Ability to transition to module stop state.

2.19 8-Bit Timer

Table 2.37 shows a Comparative Listing of 8-Bit Timer Specifications, and Table 2.38 shows a Comparative Listing of 8-Bit Timer Registers.

Table 2.37 Comparative Listing of 8-Bit Timer Specifications

Item	RX231 (TMR)	RX65N (TMR)
Count clocks	• Frequency divided clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock	• Frequency-divided clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selected by compare match A or B, or an external reset signal.	Selected by compare match A or B, or an external reset signal.
Timer output	Output pulses with a desired duty cycle or PWM output	Output pulses with a desired duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	Compare match A, compare match B, and overflow (TMR0, TMR2)	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (input)	One of the following three operations proceeds in response to an event reception: (1) Counting start operation (TMR0, TMR2) (2) Event counting operation (TMR0, TMR2) (3) Counting restart operation (TMR0, TMR2)	One of the following three operations proceeds in response to an event reception: (1) Counting start operation (TMR0 to TMR3) (2) Event counting operation (TMR0 to TMR3) (3) Counting restart operation (TMR0 to TMR3)
DTC activation	DTC can be activated by compare match A interrupts or compare match B interrupts.	DTC can be activated by compare match A interrupts or compare match B interrupts.
A/D conversion start trigger of the A/D converter	—	Compare match A of TMR0 or TMR2

Item	RX231 (TMR)	RX65N (TMR)
Capable of generating baud rate clock for SCI	Generates baud rate clock for SCI	Generation of baud rate clock for SCI
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.38 Comparative Listing of 8-Bit Timer Registers

Register	Bit	RX231 (TMR)	RX65N (TMR)
TCSR	ADTE	—	A/D Trigger Enable

2.20 Realtime Clock

Table 2.39 shows a Comparative Listing of Realtime Clock Specifications, and Table 2.40 shows a Comparative Listing of Realtime Clock Registers.

Table 2.39 Comparative Listing of Realtime Clock Specifications

Item	RX231 (RTCe)	RX65N (RTCd)
Count modes	Calendar count mode/binary count mode	Calendar count mode/binary count mode
Count source	Sub-clock (XCIN)	Sub-clock (XCIN) or main clock (EXTAL)
Clock and calendar functions	• Calendar count mode — Year, month, date, day-of-week, hour, minute, second are counted, BCD display — 12 hours/24 hours mode switching function — 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute) — Automatic adjustment function for leap years • Binary count mode Count seconds in 32 bits, binary display • Common to both modes — Start/stop function — The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz). — Clock error correction function — Clock (1 Hz/64 Hz) output	• Calendar count mode — Year, month, date, day-of-week, hour, minute, second are counted, BCD display — 12 hours/24 hours mode switching function — 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute) — Automatic adjustment function for leap years • Binary count mode Count seconds in 32 bits, binary display • Common to both modes — Start/stop function — The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz). — Clock error correction function — Clock (1 Hz/64 Hz) output
Interrupt	• Alarm interrupt (ALM) As an alarm interrupt condition, selectable which of the below is compared with: — Calendar count mode: Year, month, date, day-of-week, hour, minute, or second can be selected — Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, or 1/256 second can be selected as an interrupt period.	• Alarm interrupt (ALM) As an alarm interrupt condition, selectable which of the below is compared with: — Calendar count mode: Year, month, date, day-of-week, hour, minute, or second can be selected — Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, or 1/256 second can be selected as an interrupt period.

Item	RX231 (RTCe)	RX65N (RTCd)
Interrupt	• Carry interrupt (CUP) An interrupt is generated at either of the following timings: — When a carry from the 64-Hz counter to the second counter is generated. — When the 64-Hz counter is changed and the R64CNT register is read at the same time. • Recovery from software standby mode can be performed by an alarm interrupt or periodic interrupt	• Carry interrupt (CUP) An interrupt is generated at either of the following timings: — When a carry from the 64-Hz counter to the second counter is generated. — When the 64-Hz counter is changed and the R64CNT register is read at the same time. • Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt
Time-capture function	Times can be captured when the edge of the time capture event input pin is detected. For every event input, month, date, hour, minute, and second are captured or 32-bit binary counter value is captured.	Times can be captured when the edge of the time capture event input pin is detected. For every event input, month, date, hour, minute, and second are captured or 32-bit binary counter value is captured.
Event link function	Periodic event output	Periodic event output

Table 2.40 Comparative Listing of Realtime Clock Registers

Register	Bit	RX231 (RTCe)	RX65N (RTCd)
RCR4	—	—	RTC Control Register 4
RFRH/RFRL	—	—	Frequency Register H/L

2.21 Watchdog Timer

Table 2.41 shows a Comparative Listing of Watchdog Timer Specifications, and Table 2.42 shows a Comparative Listing of Watchdog Timer Registers.

Table 2.41 Comparative Listing of Watchdog Timer Specifications

Item	RX231 (WDTA)	RX65N (WDTA)
Count source	Peripheral module clock (PCLK)	Peripheral module clock (PCLK)
Clock division ratio	Divide by 4, 64, 128, 512, 2,048, or 8,192	Divide by 4, 64, 128, 512, 2,048, or 8,192
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Auto-start mode: Counting automatically starts after a reset or after an underflow or refresh error occurs • Register start mode: Counting is started by refresh operation (writing to the WDTRR register)	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the WDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated	• Reset (the down-counter and other registers return to their initial values) • Low power consumption state • Underflow or refresh error (register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Watchdog timer Reset sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Interrupt sources	Non-maskable interrupt sources • Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	Non-maskable interrupt/interrupt sources • Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the WDTSR register.	The down-counter value can be read by the WDTSR register.

Table 2.42 Comparative Listing of Watchdog Timer Registers

Register	Bit	RX231 (WDTA)	RX65N (WDTA)
WDTRCR	RSTIRQS	Reset Interrupt Request Selection 0: Non-maskable interrupt request output is enabled 1: Reset output is enabled	Reset Interrupt Request Selection 0: Non-maskable interrupt request or interrupt request output is enabled 1: Reset output is enabled

2.22 Independent Watchdog Timer

Table 2.43 shows a Comparative Listing of Independent Watchdog Timer Specifications, and Table 2.44 shows a Comparative Listing of Independent Watchdog Timer Registers.

Table 2.43 Comparative Listing of Independent Watchdog Timer Specifications

Item	RX231 (IWDTa)	RX65N (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Divide by1, 16, 32, 64, 128, or 256	Divide by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting automatically starts after a reset (auto-start mode) • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated Counting restarts (In auto-start mode, counting automatically restarts after a reset or after a non-maskable interrupt request is output. In register start mode, counting restarts after refreshing.)	• Reset (the down-counter and other registers return to their initial values) • Low power consumption state (by means of register setting) • Underflow or refresh error (register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Watchdog timer Reset sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Interrupt sources	Non-maskable interrupt sources • Down-counter underflows • When refreshing is done outside the refresh-permitted period (refresh error)	Non-maskable interrupt/interrupt sources • Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the IWDTSR register.	The down-counter value can be read by the IWDTSR register.
Event link function (output)	• Down-counter underflow event output • Refresh error event output	• Down-counter underflow event output • Refresh error event output
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX231 (IWDTa)	RX65N (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0]bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0]bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0]bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0]bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.44 Comparative Listing of Independent Watchdog Timer Registers

Register	Bit	RX231 (IWDTa)	RX65N (IWDTa)
IWDTCR	TOPS[1:0]	Timeout Period Select b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh)	Timeout Period Select b1 b0 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh)
IWDTRCR	RSTIRQS	Reset Interrupt Request Select 0: Non-maskable interrupt request output is enabled. 1: Reset output is enabled.	Reset Interrupt Request Select 0: Non-maskable interrupt request or interrupt request output is enabled. 1: Reset output is enabled.
IWDTCSTPR	SLCSTP	Sleep Mode Count Stop Control 0: Count stop is disabled. 1: Count is stopped at a transition to sleep mode, software standby mode, or deep sleep mode.	Sleep Mode Count Stop Control 0: Count stop is disabled. 1: Count is stopped at a transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode.

2.23 USB 2.0 Host/Function Module

Table 2.45 shows a Comparative Listing of USB 2.0 Host/Function Module Specifications, and Table 2.46 shows a Comparative Listing of USB 2.0 Host/Function Module Registers.

Table 2.45 Comparative Listing of USB 2.0 Host/Function Module Specifications

Item	RX231 (USBd)	RX65N (USBb)
Features	• USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated. Host controller, function controller, and On-The-Go (OTG) are supported (one channel) • The host controller and the function controller can be switched by software. • Self-power mode or bus power mode can be selected. • BC 1.2 (Battery Charging Specification Revision 1.2) is supported.	• USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated. Host controller, function controller, and On-The-Go (OTG) are supported (one channel) • The host controller and the function controller can be switched by software. • Self-power mode or bus power mode can be selected.
	When the host controller is selected: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported • Automatic scheduling for SOF and packet transmissions • Programmable intervals for isochronous and interrupt transfers	When the host controller is selected: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported • Automatic scheduling for SOF and packet transmissions • Programmable intervals for isochronous and interrupt transfers • Multiple peripheral devices can be connected for communication via a one-stage hub.
	When the function controller is selected: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS request • SOF interpolation function	When the function controller is selected: • Full-speed transfer (12 Mbps)*1 is supported • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS request • SOF interpolation function
Communication data transfer types	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer

Item	RX231 (USBd)	RX65N (USBb)
Pipe configuration	• Buffer memory for USB communication is provided. • Up to 10 pipes can be selected (including the default control pipe). • PIPE1 to PIPE9 can be assigned any endpoint number. Transfer conditions that can be set for each pipe: — PIPE0: Control transfer, 64-byte single buffer — PIPE1 and PIPE2: 64-byte double buffer can be specified for bulk transfer 256-byte double buffer for isochronous transfer — PIPE3 to PIPE5: Bulk transfer, 64-byte double buffer — PIPE6 to PIPE9: Interrupt transfer, 64-byte single buffer	• Buffer memory for USB communication is provided. • Up to 10 pipes can be selected (including the default control pipe). • PIPE1 to PIPE9 can be assigned any endpoint number. Transfer conditions that can be set for each pipe: — PIPE0: Control transfer, 64-byte single buffer — PIPE1 and PIPE2: 64-byte double buffer can be specified for bulk transfer 256-byte double buffer for isochronous transfer — PIPE3 to PIPE5: Bulk transfer, 64-byte double buffer — PIPE6 to PIPE9: Interrupt transfer, 64-byte single buffer
Other functions	• Reception ending function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0, 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK) • On-chip pull-up and pull-down resistors of DP/DM	• Reception ending function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0, 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK) • On-chip pull-up and pull-down resistors of D+/DM-
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Note: 1. Low-speed transfer (1.5 Mbps) is not supported when Function controller operation is selected.

Table 2.46 Comparative Listing of USB 2.0 Host/Function Module Registers

Register	Bit	RX231 (USBd)	RX65N (USBb)
SYSCFG	DMRPU	D-Line Resistor Control	—
	CNEN	CNEN Single End Receiver Enable	—
SYSSTS0	SOFEA	—	SOF Active Monitor Flag When the Host Controller is Selected
DVSTCTR0	RHST[2:0]	USB Bus Reset Status • When the host controller is selected b2 b0 0 0 0: Communication speed not determined (powered state or no connection) 1 x x: USB bus reset in progress 0 0 1: Low-speed connection 0 1 0: Full-speed connection • When the function controller is selected b2 b0 0 0 0: Communication speed not determined 0 0 1: USB bus reset in progress or low-speed connection 0 1 0: USB bus reset in progress or full-speed connection	USB Bus Reset Status Flag • When the host controller is selected b2 b0 0 0 0: Communication speed not determined (powered state or no connection) 1 x x: USB bus reset in progress 0 0 1: Low-speed connection 0 1 0: Full-speed connection • When the function controller is selected b2 b0 0 0 0: Communication speed not determined 0 0 1: USB bus reset in progress 0 1 0: USB bus reset in progress or full-speed connection
INTENB1	PDDETINTE0	PDDETINT0 Detection Interrupt Enable	—
INTSTS1	PDDETINT0	PDDET0 Detection Interrupt Status	—
DVCHGR	—	—	Device State Change Register
USBADDR	—	—	USB Address Register
PHYSLEW	—	—	PHY Cross Point Adjustment Register
DPUSR0R	—	—	Deep Standby USB Transceiver Control/Pin Monitoring Register
DPUSR1R	—	—	Deep Standby USB Suspend/Resume Interrupt Register
USBMC	—	USB Module Control Register	—
USBBCCTRL0	—	BC Control Register 0	—

2.24 Serial Communications Interface

The RX231 Group has 7 independent serial communications interface channels (SCIg: 6 channels, SCIh: 1 channel).

The RX65N Group has 13 independent serial communications interface channels (SCIg: 10 channels, SCIi: 2 channels, SCIh: 1 channel).

Table 2.47 shows a Comparative Listing of SCIg Specifications, Table 2.48 shows a Comparative Listing of SCIi Specifications, Table 2.49 shows a Comparative Listing of Serial Communications Interface Channel Specifications, and Table 2.50 shows a Comparative Listing of Serial Communications Interface Registers.

Table 2.47 Comparative Listing of SCIg Specifications

Item		RX231 (SCIg)	RX65N (SCIg)
Number of channels		6 channels	10 channels
Serial communication modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
Interrupt sources		Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Module stop state can be set for each channel.	Module stop state can be set for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Start bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.

Item		RX231 (SCIg)	RX65N (SCIg)
Asynchronous mode	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5 and SCI6).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5 and SCI6).
	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/ reception.	CTSn# and RTSn# pins can be used in controlling transmission/ reception.
Smart card interface mode	Error processing	An error signal can be automatically transmitted when detecting a parity error during reception	An error signal can be automatically transmitted when detecting a parity error during reception
		Data can be automatically retransmitted when receiving an error signal during transmission	Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Fast mode is supported.	Fast mode is supported.
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.

Item	RX231 (SCIg)	RX65N (SCIg)
Event link function	Error (receive error, error signal detection) event output	Error (receive error, error signal detection) event output
	Receive data full event output	Receive data full event output
	Transmit data empty event output	Transmit data empty event output
	Transmit end event output	Transmit end event output

Table 2.48 Comparative Listing of SCIi Specifications

Item		RX231 (—)	RX65N (SCIi)
Number of channels		—	2 channels
Serial communication modes		—	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		—	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		—	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		—	Selectable between LSB-first or MSB-first transfer.
Interrupt sources		—	Transmit end, transmit data empty, receive data full, receive error, receive data ready, and match Completion of generation of start condition, restart condition, or stop condition (simple I²C mode)
Low power consumption function		—	Module stop state can be set for each channel.
Asynchronous mode	Data length	—	7, 8, or 9 bits
	Transmission stop bits		1 or 2 bits
	Parity	—	Even parity, odd parity, or no parity
	Receive error detection	—	Parity, overrun, and framing errors
	Hardware flow control	—	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/ receive FIFO	—	16-stage FIFOs for transmit and receive buffers
	Data match detection	—	Compares receive data and comparison data, and generates interrupt when they are matched
	Start bit detection	—	Low level or falling edge is selectable.

Item		RX231 (—)	RX65N (SCIi)
Asynchronous mode	Break detection	—	When a framing error occurs, a break can be detected by reading the level of the RXDn pin directly or reading the SPTR.RXDMON flag.
	Clock source	—	An internal or external clock can be selected.
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	—	Serial communication among multiple processors
	Noise cancellation	—	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	—	8 bits
	Receive error detection	—	Overrun error
	Hardware flow control	—	CTSn# and RTSn# pins can be used in controlling transmission/ reception.
	Transmit/ receive FIFO	—	16-stage FIFOs for transmit and receive buffers
Smart card interface mode	Error processing	—	An error signal can be automatically transmitted when detecting a parity error during reception
		—	Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	—	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	—	I^2C bus format
	Operating mode	—	Master (single-master operation only)
	Transfer speed	—	Fast mode is supported.
	Noise canceler	—	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI mode	Data length	—	8 bits
	Error detection	—	Overrun error
	SS input pin function	—	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	—	Four kinds of settings for clock phase and clock polarity are selectable.

Item	RX231 (—)	RX65N (SCIi)
Bit rate modulation function	—	Correction of outputs from the on-chip baud rate generator can reduce errors.

Table 2.49 Comparative Listing of Serial Communications Interface Channel Specifications

Item	RX231 (SCIg, SCIh)	RX65N (SCIg, SCIi, SCIh)
Synchronous mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI0 to SCI12
Clock synchronous mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI0 to SCI12
Smart card interface mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI0 to SCI12
Simple I^2C mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI0 to SCI12
Simple SPI mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI0 to SCI12
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5
Transmit/receive FIFO	—	SCI10, SCI11
Data match detection	—	SCI10, SCI11

Table 2.50 Comparative Listing of Serial Communications Interface Registers

Register	Bit	RX231 (SCIg, SCIh)	RX65N (SCIg, SCIi, SCIh)
FRDR	—	—	Receive FIFO Data Register
FTDR	—	—	Transmit FIFO Data Register
SSRFIFO	—	—	Serial Status Register
FCR	—	—	FIFO Control Register
FDR	—	—	FIFO Data Count Register
LSR	—	—	Line Status Register
CDR	—	—	Comparison Data Register
DCCR	—	—	Data Comparison Control Register
SPTR	—	—	Serial Port Register

2.25 I²C-bus Interface

Table 2.51 shows a Comparative Listing of I²C Bus Interface Specifications, and Table 2.52 shows a Comparative Listing of I²C Bus Interface Registers.

Table 2.51 Comparative Listing of I²C Bus Interface Specifications

Item	RX231 (RIICa)	RX65N (RIICa)
Number of channels	1 channel	2 channels / 3 channels*1
Communication format	• I²C bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer speed	Fast-mode is supported (up to 400 kbps)	Fast-mode Plus is supported (up to 1 Mbps)
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.
Issuing and detection conditions	Start, restart, and stop conditions are generated automatically. Start conditions (including restart conditions) and stop conditions are detectable.	Start, restart, and stop conditions are generated automatically. Start conditions (including restart conditions) and stop conditions are detectable.
Slave addresses	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgement	• For transmission, the acknowledge bit is automatically loaded. Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is automatically loaded. Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level: • Waiting between the eighth and ninth clock cycles • Waiting between the ninth clock cycle and the first clock cycle of the next transfer	In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level: • Waiting between the eighth and ninth clock cycles • Waiting between the ninth clock cycle and the first clock cycle of the next transfer
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.

Item	RX231 (RIICa)	RX65N (RIICa)
Arbitration	• For multi-master operation — Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.	• For multi-master operation — Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.
Timeout detection function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise canceler	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.
Interrupt sources	Four sources • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end	Four sources • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end
Low power consumption function	Module stop state can be set.	Module stop state can be set.
RIIC operating modes	Four modes Master transmit mode, master receive mode, slave transmit mode, and slave receive mode	Four modes Master transmit mode, master receive mode, slave transmit mode, and slave receive mode

Item	RX231 (RIICa)	RX65N (RIICa)
Event link function	Four sources (RIIC0): • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end	Four sources (RIIC0): • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end

Note: 1. Can be used for products with at least 1.5 MB of code flash memory. However, two channels on 64-pin versions.

Table 2.52 Comparative Listing of I²C Bus Interface Registers

Register	Bit	RX231 (RIICa)	RX65N (RIICa)
ICFER	FMPE	—	Fast-Mode Plus Enable

2.26 CAN Module

Table 2.53 shows a Comparative Listing of CAN Module Specifications, and Table 2.54 shows a Comparative Listing of CAN Module Registers.

Table 2.53 Comparative Listing of CAN Module Specifications

Item	RX231 (RSCAN)	RX65N (CAN)
Number of channels	1 channel	2 channels
Protocol	ISO 11898-1 compliant	ISO 11898-1 compliant (standard and extended frames)
Bit rate	Maximum 1 Mbps	Programmable bit rate up to 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source
Message box	16 message boxes	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.
Reception	• Receives data frames and remote frames. • Selects ID format (standard ID, extended ID, or both IDs) to be received. • Sets interrupt enable/disable for each FIFO. • Mirror function (to receive messages transmitted from the own CAN node) • Timestamp function (to record message reception time as a 16-bit timer value)	• Data frame and remote frame can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable from overwrite mode (message overwritten) and overrun mode (message discarded) • The reception complete interrupt can be individually enabled or disabled for each mailbox.
Acceptance filter	Refer to the Reception filter function	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.

Item	RX231 (RSCAN)	RX65N (CAN)
Reception filter function	• Selects receive messages according to 16 receive rules. • Sets the number of receive rules (0 to 16) for each channel. • Acceptance filter processing: Sets ID and mask for each receive rule. • DLC filter processing: Sets DLC check value for each receive rule.	—
Receive message transfer function	• Routing function to transfer receive messages to arbitrary destinations (can be transferred to up to 2 buffers). Transfer destination: Receive buffer, receive FIFO buffer, and transmit/receive FIFO buffer • Label addition function Stores label information together when storing a message in a receive buffer and FIFO buffer.	—
Transmission	• Transmits data frames and remote frames. • Selects ID format (standard ID, extended ID, or both IDs) to be transmitted. • One-shot transmission function • Selects ID priority transmission or transmit buffer number priority transmission. • Transmit abort function (completion of the abort can be confirmed with the flag) • Sets interrupt enable/disable for each transmit buffer and transmit/receive FIFO buffer.	• Data frame and remote frame can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable from ID priority mode and mailbox number priority mode • Transmission request can be aborted (the completion of abort can be confirmed with a flag) • The transmission complete interrupt can be individually enabled or disabled for each mailbox.
Interval transmission function	Sets message transmission interval time (transmit mode of transmit/receive FIFO buffers)	—
Transmit history function	Stores the history information of transmitted messages.	—
Mode transition for bus-off recovery	Selects a method of returning from bus off state. • ISO 11898-1 compliant • Automatic transition to channel halt mode at bus-off entry • Automatic transition to channel halt mode at bus-off end • Transition to channel halt mode by a program • Transition to the error-active state by a program (forcible return from the bus off state)	Mode transition for the recovery from the bus-off state can be selected: • ISO 11898-1 Standards compliant • Automatic entry to CAN halt mode at bus-off entry • Automatic entry to CAN halt mode at bus-off end • Entry to CAN halt mode by a program • Transition into error-active state by a program

Item	RX231 (RSCAN)	RX65N (CAN)
Error status monitoring	• Monitors CAN protocol errors (stuff error, form error, ACK error, CRC error, bit error, ACK delimiter error, and bus dominant lock). • Detects error status transitions (error warning, error passive, bus off entry, and bus off recovery) • Reads the error counter. • Monitors DLC errors.	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off entry, and bus-off recovery). • The error counters can be read.
Time stamp function	• Time stamp function using a 16-bit counter • Timestamp clock source can be divided	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.
Interrupt function	• 5 sources • Global (2 sources) — Global receive FIFO interrupt — Global error interrupt • Channel (3 sources/channel) Channel transmit interrupt — Transmit complete interrupt — Transmit abort interrupt — Transmit/receive FIFO transmit complete interrupt — Transmit history interrupt Transmit/receive FIFO receive interrupt Channel error interrupt	Five types of interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupts)
CAN sleep mode	—	Current consumption can be reduced by stopping the CAN clock.
Software support unit	—	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support
CAN clock source	Peripheral module clock (PCLK), CANMCLK	Peripheral module clock (PCLKB) or CANMCLK
Test mode	Test function for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback) • RAM test (read/write test)	Three test modes available for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)
Power consumption reducing function	Module stop state can be set.	Module stop state can be set.

Table 2.54 Comparative Listing of CAN Module Registers

Register	Bit	RX231 (RSCAN)	RX65N (CAN)
CTLR	—	—	Control Register
BCR	—	—	Bit Configuration Register
MKRk	—	—	Mask Register k (k = 0 to 7)
FIDCR0	—	—	FIFO Received ID Compare Registers 0
FIDCR1	—	—	FIFO Received ID Compare Registers 1
MKIVLR	—	—	Mask Invalid Register
MBj	—	—	Mailbox Register j (j = 0 to 31)
MIER	—	—	Mailbox Interrupt Enable Register
MCTLj	—	—	Message Control Register j (j = 0 to 31)
RFCR	—	—	Receive FIFO Control Register
RFPCR	—	—	Receive FIFO Pointer Control Register
TFCR	—	—	Transmit FIFO Control Register
TFPCR	—	—	Transmit FIFO Pointer Control Register
STR	—	—	Status Register
MSMR	—	—	Mailbox Search Mode Register
MSSR	—	—	Mailbox Search Status Register
CSSR	—	—	Channel Search Support Register
AFSR	—	—	Acceptance Filter Support Register
EIER	—	—	Error Interrupt Enable Register
EIFR	—	—	Error Interrupt Factor Judge Register
RECR	—	—	Receive Error Count Register
TECR	—	—	Transmit Error Count Register
ECSR	—	—	Error Code Store Register
TSR	—	—	Time Stamp Register
TCR	—	—	Test Control Register
CFGL	—	Bit Configuration Register L	—
CFGH	—	Bit Configuration Register H	—
CTRL	—	Control Register L	—
CTRH	—	Control Register H	—
STSL	—	Status Register L	—
STSH	—	Status Register H	—
ERFLL	—	Error Flag Register L	—
ERFLH	—	Error Flag Register H	—
GCFGL	—	Global Configuration Register L	—
GCFGH	—	Global Configuration Register H	—
GCTRL	—	Global Control Register L	—
GCTRH	—	Global Control Register H	—
GSTS	—	Global Status Register	—
GERFLL	—	Global Error Flag Register	—
GTINTSTS	—	Global Transmit Interrupt Status Register	—
GTSC	—	Timestamp Register	—

Register	Bit	RX231 (RSCAN)	RX65N (CAN)
GAFLCFG	—	Receive Rule Number Configuration Register	—
GAFLIDLj	—	Receive Rule Entry Register jAL (j = 0 to 15)	—
GAFLIDHj	—	Receive Rule Entry Register jAH (j = 0 to 15)	—
GAFLMLj	—	Receive Rule Entry Register jBL (j = 0 to 15)	—
GAFLMHj	—	Receive Rule Entry Register jBH (j = 0 to 15)	—
GAFLPLj	—	Receive Rule Entry Register jCL (j = 0 to 15)	—
GAFLPHj	—	Receive Rule Entry Register jCH (j = 0 to 15)	—
RMNB	—	Receive Buffer Number Configuration Register	—
RMND0	—	Receive Buffer Receive Complete Flag Register	—
RMIDLn	—	Receive Buffer Register nAL (n = 0 to 15)	—
RMIDHn	—	Receive Buffer Register nAH (n = 0 to 15)	—
RMTSn	—	Receive Buffer Register nBL (n = 0 to 15)	—
RMPTRn	—	Receive Buffer Register nBH (n = 0 to 15)	—
RMDF0n	—	Receive Buffer Register nCL (n = 0 to 15)	—
RMDF1n	—	Receive Buffer Register nCH (n = 0 to 15)	—
RMDF2n	—	Receive Buffer Register nDL (n = 0 to 15)	—
RMDF3n	—	Receive Buffer Register nDH (n = 0 to 15)	—
RFCCm	—	Receive FIFO Control Register m (m = 0, 1)	—
RFSTSm	—	Receive FIFO Status Register m (m = 0, 1)	—
RFPCTRm	—	Receive FIFO Pointer Control Register m (m = 0, 1)	—
RFIDLm	—	Receive FIFO Access Register mAL (m = 0, 1)	—
RFIDHm	—	Receive FIFO Access Register mAH (m = 0, 1)	—
RFTSm	—	Receive FIFO Access Register mBL (m = 0, 1)	—
RFPTRm	—	Receive FIFO Access Register mBH (m = 0, 1)	—
RFDF0m	—	Receive FIFO Access Register mCL (m = 0, 1)	—
RFDF1m	—	Receive FIFO Access Register mCH (m = 0, 1)	—

Register	Bit	RX231 (RSCAN)	RX65N (CAN)
RFDF2m	—	Receive FIFO Access Register mDL (m = 0, 1)	—
RFDF3m	—	Receive FIFO Access Register mDH (m = 0, 1)	—
CFCCL0	—	Transmit/Receive FIFO Control Register 0L	—
CFCCH0	—	Transmit/Receive FIFO Control Register 0H	—
CFSTS0	—	Transmit/Receive FIFO Status Register 0	—
CFPCTR0	—	Transmit/Receive FIFO Pointer Control Register 0	—
CFIDL0	—	Transmit/Receive FIFO Access Register 0AL	—
CFIDH0	—	Transmit/Receive FIFO Access Register 0AH	—
CFTS0	—	Transmit/Receive FIFO Access Register 0BL	—
CFPTR0	—	Transmit/Receive FIFO Access Register 0BH	—
CFDF00	—	Transmit/Receive FIFO Access Register 0CL	—
CFDF10	—	Transmit/Receive FIFO Access Register 0CH	—
CFDF20	—	Transmit/Receive FIFO Access Register 0DL	—
CFDF30	—	Transmit/Receive FIFO Access Register 0DH	—
RFMSTS	—	Receive FIFO Message Lost Status Register	—
CFMSTS	—	Transmit/Receive FIFO Message Lost Status Register	—
RFISTS	—	Receive FIFO Interrupt Status Register	—
CFISTS	—	Transmit/Receive FIFO Receive Interrupt Status Register	—
TMCp	—	Transmit Buffer Control Register p (p = 0 to 3)	—
TMSTSp	—	Transmit Buffer Status Register p (p = 0 to 3)	—
TMTRSTS	—	Transmit Buffer Transmit Request Status Register	—
TMTCSTS	—	Transmit Buffer Transmit Complete Status Register	—
TMTASTS	—	Transmit Buffer Transmit Abort Status Register	—
TMIEC	—	Transmit Buffer Interrupt Enable Register	—
TMIDLp	—	Transmit Buffer Register pAL (p = 0 to 3)	—
TMIDHp	—	Transmit Buffer Register pAH (p = 0 to 3)	—

Register	Bit	RX231 (RSCAN)	RX65N (CAN)
TMPTRp	—	Transmit Buffer Register pBH (p = 0 to 3)	—
TMDF0p	—	Transmit Buffer Register pCL (p = 0 to 3)	—
TMDF1p	—	Transmit Buffer Register pCH (p = 0 to 3)	—
TMDF2p	—	Transmit Buffer Register pDL (p = 0 to 3)	—
TMDF3p	—	Transmit Buffer Register pDH (p = 0 to 3)	—
THLCC0	—	Transmit History Buffer Control Register	—
THLSTS0	—	Transmit History Buffer Status Register	—
THLACC0	—	Transmit History Buffer Access Register	—
THLPCTR0	—	Transmit History Buffer Pointer Control Register	—
GRWCR	—	Global RAM Window Control Register	—
GTSTCFG	—	Global Test Configuration Register	—
GTSTCTRL	—	Global Test Control Register	—
GLOCKK	—	Global Test Protection Unlock Register	—
RPGACCr	—	RAM Test Register r (r = 0 to 127)	—

2.27 Serial Peripheral Interface

Table 2.55 shows a Comparative Listing of Serial Peripheral Interface Specifications, and Table 2.56 shows a Comparative Listing of Serial Peripheral Interface Registers.

Table 2.55 Comparative Listing of Serial Peripheral Interface Specifications

Item	RX231 (RSPIa)	RX65N (RSPIc)
Number of channels	1 channel	3 channels
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection

Item	RX231 (RSPIa)	RX65N (RSPIc)
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range:1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLn0 to SSLn3) for each channel • In single-master mode, SSLn0 to SSLn3 pins are output. • In multi-master mode: SSLn0 pin for input, and SSLn1 to SSLn3 pins for either output or unused. • In slave mode: SSLn0 pin for input, and SSLn1 to SSLn3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function
Interrupt sources	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, or parity error) • RSPI idle interrupt (RSPI idle)	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, underrun, or parity error) • RSPI idle interrupt (RSPI idle)

Item	RX231 (RSPIa)	RX65N (RSPIc)
Event link function (output)	The following events can be output to the event link controller. (RSPI0) • Receive buffer full signal • Transmit buffer empty signal • Mode fault, overrun, or parity error signal • RSPI idle signal • Transmission-completed signal	The following events can be output to the event link controller. (RSPI0) • Receive buffer full signal • Transmit buffer empty signal • Mode fault, overrun, underrun, or parity error signal • RSPI idle signal • Transmission-completed signal
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.56 Comparative Listing of Serial Peripheral Interface Registers

Register	Bit	RX231 (RSPIa)	RX65N (RSPIc)
SPSR	MODF	Mode Fault Error Flag 0: No mode fault error occurs 1: A mode fault error occurs	Mode Fault Error Flag 0: Neither a mode fault error nor an underrun error occurs 1: A mode fault error or an underrun error occurs
	UDRF	—	Underrun Error Flag
SPDR	—	RSPI Data Register Accessible size • Longwords access (the SPLW bit is 1) • Words access (the SPLW bit is 0)	RSPI Data Register Accessible size • Longwords access (the SPLW bit is 1 and the SPBYT bit is 0) • Words access (the SPLW bit is 0 and the SPBYT bit is 0) • Bytes access (the SPBYT bit is 1)
SPDCR	SPBYT	—	RSPI Byte Access Specification
SPDCR2	—	—	RSPI Data Control Register 2

2.28 CRC Calculator

Table 2.57 shows a Comparative Listing of CRC Calculator Specifications, and Table 2.58 shows a Comparative Listing of CRC Calculator Registers.

Table 2.57 Comparative Listing of CRC Calculator Specifications

Item	RX231 (CRC)	RX65N (CRCA)	
Data size	8 bits	8 bits	32 bits
Data for CRC calculation	CRC code generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)
CRC processor unit	Operation executed on 8 bits in parallel	8-bit parallel processing	32-bit parallel processing
CRC generating polynomial	One of three generating polynomials selectable: • 8-bit CRC $X^8 + X^2 + X + 1$ • 16-bit CRC — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of five generating polynomials selectable: • 8-bit CRC $X^8 + X^2 + X + 1$ • 16-bit CRC — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of five generating polynomials selectable: • 32-bit CRC — $X^{32} + X^{26} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ — $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	The bit order of CRC calculation results can be switched for LSB first or MSB first communication	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	
Low power consumption function	Module stop state can be set.	Module stop state can be set.	

Table 2.58 Comparative Listing of CRC Calculator Registers

Register	Bit	RX231 (CRC)	RX65N (CRCA)
CRCCR	GPS[1:0]: RX231 GPS[2:0]: RX65N	CRC Generating Polynomial Switching b1 b0 0 0: No calculation is executed. 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$)	CRC Generating Polynomial Switching b2 b0 0 0 0: No calculation is executed. 0 0 1: 8-bit CRC ($X^8 + X2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0: No calculation is executed. 1 1 1: No calculation is executed.
	LMS	CRC Calculation Switching (b2)	CRC Calculation Switching (b6)
CRCDIR	—	CRC Data Input Register Accessible size • Bytes access	CRC Data Input Register Accessible size • Longwords access (When 32-bit CRC is selected) • Bytes access (When 16-bit or 8-bit CRC is selected)
CRCDOR	—	CRC Data Output Register Accessible size • Words access When an 8-bit CRC is in use, the valid CRC code is obtained in the low-order byte (b7 to b0)	CRC Data Output Register Accessible size • Longwords access (When 32-bit CRC is selected) • Words access (When 16-bit CRC is selected) • Bytes access (When 8-bit CRC is selected)

2.29 SD Host Interface

Table 2.59 shows a Comparative Listing of SD Host Interface Specifications, and Table 2.60 shows a Comparative Listing of SD Host Interface Registers.

Table 2.59 Comparative Listing of SD Host Interface Specifications

Item	RX231 (SDHIa)	RX65N (SDHI)
SD bus interface	• Compatible with SD memory card and SDIO card • Transfer bus mode selectable from 4-bit wide bus mode or 1-bit default bus mode • Compatible with SD, SDHC, and SDXC formats	• Compatible with SD memory card and SDIO card • Transfer bus mode selectable from 4-bit wide bus mode or 1-bit default bus mode • Compatible with SD, SDHC, and SDXC formats
Transfer modes	Supports default speed mode	Selectable from high-speed mode or default speed mode
SDHI clock	The SDHI clock is generated by dividing peripheral module clock B (PCLKB) by n, where n = 1, 2, 4, 8, 16, 32, 64, 128, 256, or 512	The SDHI clock is generated by dividing peripheral module clock B (PCLKB) by n, where n = 1, 2, 4, 8, 16, 32, 64, 128, 256, or 512
Error check functions	• CRC7 (command/response) • CRC16 (transfer data)	• CRC7 (command/response) • CRC16 (transfer data)
Interrupt sources	• Card access interrupt (CACI) • SDIO access interrupt (SDACI) • Card detection interrupt (CDETI) • SD buffer access interrupt (SBFAI)	• Card access interrupt (CACI) • SDIO access interrupt (SDACI) • Card detection interrupt (CDETI) • SD buffer access interrupt (SBFAI)
DMA transfer sources	• DMAC and DTC triggerable by the SBFAI interrupt • SD buffer is read and write accessible using the DMAC and DTC	• DMAC and DTC triggerable by the SBFAI interrupt • SD buffer is read and write accessible using the DMAC and DTC
Other functions	• Card detection • Write protection	• Card detection • Write protection

Table 2.60 Comparative Listing of SD Host Interface Registers

Register	Bit	RX231 (SDHIa)	RX65N (SDHI)
SDVER	—	—	Version Register

2.30 12-Bit A/D Converter

Table 2.61 shows a Comparative Listing of 12-Bit A/D Converter Specifications, and Table 2.62 shows a Comparative Listing of 12-Bit A/D Converter Registers.

Table 2.61 Comparative Listing of 12-Bit A/D Converter Specifications

Item	RX231 (S12ADE)	RX65N (S12ADFa)
Number of units	1 unit	2 units
Input channels	24 channels	• Unit 0: 8 channels • Unit 1: 21 channels + one extended channel
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	0.83 μs per channel (when A/D conversion clock ADCLK = 54 MHz)	• 0.48 μs per channel (12-bit conversion mode) • 0.45 μs per channel (10-bit conversion mode) • 0.42 μs per channel (8-bit conversion mode) (A/D conversion clock: when ADCLK operates at 60 MHz)
A/D conversion clock (ADCLK)	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data register	• 24 registers for analog input, 1 for A/D-converted data duplication in double trigger mode • One register for temperature sensor output • One register for internal reference voltage • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion	• 29 registers for analog input (eight for Unit0 and 21 for Unit1), 1 for A/D-converted data duplication in double trigger mode per unit, and 2 for A/D-converted data duplication during extended operation in double trigger mode per unit. • One register for temperature sensor (Unit1) • One register for internal reference (Unit1) • One register for self-diagnosis per unit • The results of A/D conversion are stored in 12-bit A/D data registers. • 8-, 10-, and 12-bit accuracy output for the results of A/D conversion

Item	RX231 (S12ADE)	RX65N (S12ADFa)
Data register	• The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.	• The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating modes	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 24 channels arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 24 channels arbitrarily selected.	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 8 channels (Unit0) / 21 channels (Unit1) arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output (Unit1). — A/D conversion is performed only once on the internal reference voltage (Unit1). — A/D conversion is performed only once on the extended analog input (Unit1). • Continuous scan mode: — A/D conversion is performed repeatedly on the analog input of up to 8 channels (Unit0) / 21 channels (Unit1) arbitrarily selected, temperature sensor output (Unit1), and internal reference voltage (Unit1) of the arbitrarily selected channel. — A/D conversion is performed repeatedly on the extended analog input (Unit1).

Item	RX231 (S12ADE)	RX65N (S12ADFa)
Operating modes	• Group scan mode: — Analog inputs of up to 24 channels arbitrarily selected, are divided into group A and group B, and A/D conversion of the analog input selected on a group basis is performed only once. — The conditions for scanning start of group A and group B (synchronous trigger) can be independently selected, thus allowing A/D conversion of group A and group B to be started independently. • Group scan mode (when group A is given priority): — If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B is stopped and A/D conversion is performed on group A. — Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be set.	• Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. Only the combination of groups A and B can be selected when the number of the groups is two. — Analog inputs, temperature sensor output (Unit1), and internal reference voltage (Unit1) that are arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. — The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently. • Group scan mode (when group priority control selected): — If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) > group B > group C (lowest). — Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU), the event link controller (ELC), or the 16-bit timer pulse unit (TPU). • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), 16-bit timer pulse unit (TPU), or event link controller (ELC). • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# (Unit0) or ADTRG1# (Unit1) pin (independently for two units).

Item	RX231 (S12ADE)	RX65N (S12ADFa)
Functions	• Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • 16 ring buffers when the compare function is used	• Channel-dedicated sample-and-hold function (three channels for Unit0 only) • Variable sampling state count (settable for each channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • 12-/10-/8-bit conversion switching • Automatic clear function of A/D data registers • Extended analog input • Comparison function (windows A and B)
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan of group A, whereas A/D scan end interrupt request (GBADI) specially for group B can be generated on completion of group B scan.	• In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of single scan. • In double trigger mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of double scan. • In group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (S12GBADI or S12GBADI1) can be generated, and on completion of a group C scan a dedicated group C scan end interrupt request (S12GCADI or S12GCADI1) can be generated. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of double scan of group A, and the corresponding scan end interrupt request (S12GBADI/S12GCADI or S12GBADI1/S12GCADI1) can be generated on completion of group B and group C scan.

Item	RX231 (S12ADE)	RX65N (S12ADFa)
Interrupt sources	• The S12ADI0 and GBADI interrupts can activate the DMA controller (DMAC) and the data transfer controller (DTC).	• A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPBI, or S12CMPBI1) can be generated upon a match with the comparison condition for the digital compare function. • The S12ADI/S12ADI1, S12GBADI/S12GBADI1, and S12GCADI/S12GCADI1 interrupts can activate the DMA controller (DMAC) and data transfer controller (DTC).
Event link function	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • An ELC event is generated on completion of group B scan in group scan mode. • An ELC event is generated on completion of all scans. • Scan can be started by a trigger output by the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode.	• An ELC event is generated upon completion of all scans • Able to start scanning by a trigger from the ELC
Low power consumption function	Module stop state can be set	Module stop state can be set.

Table 2.62 Comparative Listing of 12-Bit A/D Converter Registers

Register	Bit	RX231 (S12ADE)	RX65N (S12ADFa)
ADDBLDRA	—	—	A/D Data Duplication Register A
ADDBLDRB	—	—	A/D Data Duplication Register B
ADRD	—	A/D Self-Diagnosis Data Register [Formats] • Flush-right format The A/D-converted value is stored in bits 11 to 0. The self-diagnosis status is stored in bits 15 and 14. Bits 13 and 12 are read as 0.	A/D Self-Diagnosis Data Register [Formats] • Flush-right format with setting of 12-bit resolution The A/D-converted value is stored in bits 11 to 0. The self-diagnosis status is stored in bits 15 and 14. Bits 13 and 12 are read as 0. • Flush-right format with setting of 10-bit resolution The A/D-converted value is stored in bits 9 to 0. The self-diagnosis status is stored in bits 15 and 14. Bits 13 to 10 are read as 0.

Register	Bit	RX231 (S12ADE)	RX65N (S12ADFa)
ADRD	—	• Flush-left format The A/D-converted value is stored in bits 15 to 4. The self-diagnosis status is stored in bits 1 and 0. Bits 3 and 2 are read as 0.	• Flush-right format with setting of 8-bit resolution The A/D-converted value is stored in bits 7 to 0. The self-diagnosis status is stored in bits 15 and 14. Bits 13 to 8 are read as 0. • Flush-left format with setting of 12-bit resolution The A/D-converted value is stored in bits 15 to 4. The self-diagnosis status is stored in bits 1 and 0. Bits 3 and 2 are read as 0. • Flush-left format with setting of 10-bit resolution The A/D-converted value is stored in bits 15 to 6. The self-diagnosis status is stored in bits 1 and 0. Bits 5 to 2 are read as 0. • Flush-left format with setting of 8-bit resolution The A/D-converted value is stored in bits 15 to 8. The self-diagnosis status is stored in bits 1 and 0. Bits 7 to 2 are read as 0.
ADCSR	ADHSC	A/D Conversion Select	—
ADANSA0 (S12AD1)	—	—	A/D Channel Select Register A0
ADANSA1 (S12AD)	—	A/D Channel Select Register A1	—
ADANSA1 (S12AD1)	—	—	A/D Channel Select Register A1
ADANSB0 (S12AD1)	—	—	A/D Channel Select Register B0
ADANSB1 (S12AD)	—	A/D Channel Select Register B1	—
ADANSB1 (S12AD1)	—	—	A/D Channel Select Register B1
ADANSC0 (S12AD)	—	—	A/D Channel Select Register C0
ADANSC0 (S12AD1)	—	—	A/D Channel Select Register C0
ADANSC1 (S12AD1)	—	—	A/D Channel Select Register C1
ADADS0 (S12AD1)	—	—	A/D-Converted Value Addition/Average Function Select Register 0
ADADS1 (S12AD)	—	A/D-Converted Value Addition/Average Function Select Register 1	—

Register	Bit	RX231 (S12ADE)	RX65N (S12ADFa)
ADADS1 (S12AD1)	—	—	A/D-Converted Value Addition/Average Function Select Register 1
ADCER	ADPRC[1:0]	—	A/D Conversion Resolution Setting
ADEXICR	TSSA	Temperature Sensor Output A/D Conversion Select This bit selects A/D conversion of the temperature sensor output in signal scan mode. 0: A/D conversion of temperature sensor output is not performed. 1: A/D conversion of temperature sensor output is performed.	Temperature Sensor Output A/D Conversion Select This bit selects A/D conversion of the temperature sensor output for group A in signal scan mode, sequence scan mode, or group scan mode. 0: A/D conversion of temperature sensor output is not performed. 1: A/D conversion of temperature sensor output is performed.
	TSSB	—	Temperature Sensor Output A/D Conversion Select
	OCSB	—	Internal Reference Voltage A/D Conversion Select
	EXSEL[1:0]	—	Extended Analog Input Select
	EXOEN	—	Extended Analog Output Control
ADGCEXCR	—	—	A/D Group C Extended Input Control Register
ADGCTRGR	—	—	A/D Group C Trigger Select Register
ADSSTRn	—	A/D Sampling State Register n (n = 0 to 7, L, T, O)	A/D Sampling State Register n (n = 0 to 15, L, T, O)
ADSHCR	—	—	A/D Sample-and-Hold Circuit Control Register
ADSHMSR	—	—	A/D Sample-and-Hold Operating Mode Select Register
ADELCCR	—	A/D Event Link Control Register	—
ADGSPCR	PGS	Group-A Priority Control Setting	Group Priority Control Setting
	GBRSCN	Group B Restart Setting	Low-Priority Group Restart Setting
	LGRRS	—	Restart Channel Select
	GBRP	Group B Single Scan Continuous Start	Single Scan Continuous Start
ADCMPCR	CMPAB[1:0]	Window A/B Composite Condition Setting b1 b0 0 0: S12ADWMELC is output when window A comparison conditions are met OR window B comparison conditions are met. S12ADWUMELC is output in other cases.	Window A/B Complex Conditions Setting b1 b0 0 0: Window A comparison condition matched OR window B comparison condition matched

Register	Bit	RX231 (S12ADE)	RX65N (S12ADFa)
ADCMPCR	CMPAB[1:0]	b1 b0 0 1: S12ADWMELC is output when window A comparison conditions are met EXOR window B comparison conditions are met. S12ADWUMELC is output in other cases. 1 0: S12ADWMELC is output when window A comparison conditions are met AND window B comparison conditions are met. S12ADWUMELC is output in other cases. 1 1: Setting prohibited.	b1 b0 0 1: Window A comparison condition matched EXOR window B comparison condition matched 1 0: Window A comparison condition matched AND window B comparison condition matched 1 1: Setting is prohibited
	CMPBE	Compare Window B Operation Enable 0: Compare window B operation is disabled. S12ADWMELC and S12ADWUMELC outputs are disabled. 1: Compare window B operation is enabled.	Comparison Window B Enable 0: Comparison window B disabled 1: Comparison window B enabled
	CMPAE	Compare Window A Operation Enable 0: Compare window A operation is disabled.S12ADWMELC and S12ADWUMELC outputs are disabled. 1: Compare window A operation is enabled.	Comparison Window A Enable 0: Comparison window A disabled 1: Comparison window A enabled
	CMPBIE	—	Comparison Window B Interrupt Enable
	CMPAIE	—	Comparison Window A Interrupt Enable
ADCMPANSR0 (S12AD1)	—	—	A/D Comparison Function Window A Channel Select Register 0
ADCMPANSR1 (S12AD)	—	A/D Comparison Function Window A Channel Select Register 1	—
ADCMPANSR1 (S12AD1)	—	—	A/D Comparison Function Window A Channel Select Register 1
ADCMPANSER	CMPSTS	—	Temperature Sensor Output Comparison Select
	CMPTSA	Temperature Sensor Output Compare Select	—
	CMPSOC	—	Internal Reference Voltage Compare Select
	CMPOCA	Internal Reference Voltage Compare Select	—

Register	Bit	RX231 (S12ADE)	RX65N (S12ADFa)
ADCMPLR0 (S12AD1)	—	—	A/D Comparison Function Window A Comparison Condition Setting Register 0
ADCMPLR1 (S12AD)	—	A/D Compare Function Window A Comparison Condition Setting Register 1	—
ADCMPLR1 (S12AD1)	—	—	A/D Comparison Function Window A Comparison Condition Setting Register 1
ADCMPLER	CMPLTS	—	Comparison Window A Temperature Sensor Output Comparison Condition Select
	CMPLTSA	Compare Window A Temperature Sensor Output Comparison Condition Select	—
	CMPLOC	—	Comparison Window A Internal Reference Voltage Comparison Condition Select
	CMPLOCA	Internal Reference Voltage Comparison Condition Select	—
ADCMPDR0	—	A/D Compare Function Window A Lower-Side Level Setting Register The ADCMPDR0 register uses different formats depending on conditions. For details on the conditions, see User's Manuals, listed in section 5, Reference Documents.	
ADCMPDR1	—	A/D Compare Function Window A Upper-Side Level Setting Register The ADCMPDR1 register uses different formats depending on conditions. For details on the conditions, see User's Manuals, listed in section 5, Reference Documents.	
ADCMPSR0 (S12AD1)	—	—	A/D Comparison Function Window A Channel Status Register 0
ADCMPSR1 (S12AD)	—	A/D Compare Function Window A Channel Status Register 1	—
ADCMPSR1 (S12AD1)	—	—	A/D Compare Function Window A Channel Status Register 1
ADCMPSER	CMPFTS	—	Comparison Window A Temperature Sensor Output Comparison Flag
	CMPSTTSA	Compare Window A Temperature Sensor Output Compare Flag	—
	CMPFOC	—	Comparison Window A Internal Reference Voltage Comparison Flag
	CMPSTOCA	Compare Window A Internal Reference Voltage Compare Flag	—
ADHVREFCNT	—	A/D High-Potential/Low-Potential Reference Voltage Control Register	—

Register	Bit	RX231 (S12ADE)	RX65N (S12ADFa)
ADCMPBNSR (S12AD)	CMPCHB [5:0]	Compare Window B Channel Select b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : 0 0 0 1 1 0: AN006 0 0 0 1 1 1: AN007 0 1 0 0 0 0: AN016 0 1 0 0 0 1: AN017 : 0 1 1 0 0 1: AN029 0 1 1 1 1 0: AN030 0 1 1 1 1 1: AN031 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage Settings other than above are prohibited.	Compare Window B Channel Select b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : 0 0 0 1 1 0: AN006 0 0 0 1 1 1: AN007 Settings other than above are prohibited.
ADCMPBNSR (S12AD1)	—	—	A/D Comparison Function Window B Channel Select Register
ADWINLLB	—	A/D Compare Function Window B Lower-Side Level Setting Register The ADWINLLB register uses different formats depending on the conditions. For details on the conditions, see User's Manuals, listed in section 5, Reference Documents.	
ADWINULB	—	A/D Comparison Function Window B Upper Level Setting Register The ADWINULB register uses different formats depending on the conditions. For details on the conditions, see User's Manuals, listed in section 5, Reference Documents.	
ADSAM	—	—	A/D Conversion Time Setting Register
ADSAMPR	—	—	A/D Conversion Time Setting Protection Release Register
ADBUFn	—	A/D Data Storage Buffer Register n (n = 0 to 15)	—
ADBUFEN	—	A/D Data Storage Buffer Enable Register	—
ADBUFPTR	—	A/D Data Storage Buffer Pointer Register	—

2.31 12-Bit D/A Converter

Table 2.63 shows a Comparative Overview of 12-Bit D/A Converter for specifications, and Table 2.64 shows a Comparative Listing of 12-bit D/A Converter Registers.

Table 2.63 Comparative Overview of 12-Bit D/A Converter

Item	RX231 (R12DAA)	RX65N (R12DA)
Resolution	12 bits	12 bits
Output channel	2 channels	2 channels
Measure against mutual interference between analog modules	Measure against interference between D/A and A/D conversion: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal output by the the 12-bit A/D converter. Degradation of 12-bit D/A conversion accuracy caused by interference is reduced by controlling the D/A converter inrush current generation timing with the enable signal.	Measure against interference between D/A and A/D conversion: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal output by the the 12-bit A/D converter (unit 1). Degradation of 12-bit A/D conversion accuracy caused by interference is reduced by controlling the D/A converter inrush current generation timing with the enable signal.
Low power consumption function	Ability to transition to module stop state.	Ability to transition to module stop state.
Event link function (input)	Ability to activate D/A conversion on channel 0 by event signal input	Ability to activate D/A conversion on channel 0 by event signal input
Output buffer amplifier control function	—	Buffered output (gain = 1) or unbuffered output can be selected.

Table 2.64 Comparative Listing of 12-bit D/A Converter Registers

Register	Bit	RX231 (R12DAA)	RX65N (R12DA)
DACR	DAE	—	D/A Enable
DAADUSR	—	—	D/A A/D Synchronous Unit Select Register
DAVREFCR	—	D/A VREF Control Register	—
DAAMPCR	—	—	D/A Output Amplifier Control Register
DAASWCR	—	—	D/A Output Amplifier Stabilization Wait Control Register

2.32 Temperature Sensor

Table 2.65 shows a Comparative Listing of Temperature Sensor Specifications, and Table 2.66 shows a Comparative Listing of Temperature Sensor Registers.

Table 2.65 Comparative Listing of Temperature Sensor Specifications

Item	RX231 (TEMPSA)	RX65N (TEMPS)
Temperature sensor voltage output	The temperature sensor voltage is output to the 12-bit A/D converter.	Temperature sensor outputs a voltage to the 12-bit A/D converter unit 1.
Low power consumption function	—	The module-stop state is selectable.
Temperature sensor calibration data	—	Reference data measured for each chip at factory shipment is stored.

Table 2.66 Comparative Listing of Temperature Sensor Registers

Register	Bit	RX231 (TEMPSA)	RX65N (TEMPS)
TSCR	—	—	Temperature Sensor Control Register
TSCDRH, TSCDRL (RX231) TSCDR (RX65N)	—	Temperature Sensor Calibration Data Register (b7 to b0) Bits 3 to 0 in TSCDRH and bits 7 to 0 in TSCDRL hold the temperature sensor calibration data measured for each chip at the time of shipment.	Temperature Sensor Calibration Data Register (b31 to b0) Bits 11 to 0 hold the temperature sensor calibration data measured for each chip at the time of shipment.

2.33 RAM

Table 2.67 shows a Comparative Listing of RAM Specifications, and Table 2.68 shows a Comparative Listing of RAM Registers.

Table 2.67 Comparative Listing of RAM Specifications

Item	RX231	RX65N
RAM capacity	• 32 KB RAM0: 32 KB • 64 KB RAM0: 64 KB	• 256 KB / 384 KB*1 RAM0: 256 KB Expansion RAM: 384 KB*1
RAM address	• When the RAM capacity is 32 KB RAM0: 0000 0000h to 0000 7FFFh • When the RAM capacity is 64 KB RAM0: 0000 0000h to 0000 FFFFh	RAM0: 0000 0000h to 0003 FFFFh Expansion RAM: 0080 0000h to 0085 FFFFh*1
Access	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • Enabling or disabling of the RAM is selectable.
Data retention function	—	Not available in deep software standby mode
Low power consumption function	The module stop state is selectable for RAM0.	Transition to the module stop state is separately possible for the RAM and expansion RAM*1.
Error checking function	—	• Detection of 1-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

Table 2.68 Comparative Listing of RAM Registers

Register	Bit	RX231	RX65N
RAMMODE	—	—	RAM Operating Mode Control Register
RAMSTS	—	—	RAM Error Status Register
RAMECAD	—	—	RAM Error Address Capture Register
RAMPRCR	—	—	RAM Protection Register
EXRAMMODE	—	—	Expansion RAM Operating Mode Control Register*1
EXRAMSTS	—	—	Expansion RAM Error Status Register*1
EXRAMECAD	—	—	Expansion RAM Error Address Capture Register*1
EXRAMPRCR	—	—	Expansion RAM Protection Register*1

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

2.34 Flash Memory (Code Flash)

Table 2.69 shows a Comparative Listing of Flash Memory (Code Flash) Specifications, and Table 2.70 shows a Comparative Listing of Flash Memory Registers.

Table 2.69 Comparative Listing of Flash Memory (Code Flash) Specifications

Item	RX231	RX65N
Memory space	• User area: Up to 512 KB • Extra area: Stores the start-up area information, access window information, and unique ID	User area: Maximum 2 MB*1
ROM cache	—	• Capacity: 256 Bytes • Mapping method: 8-way set associative • Replace method: LRU method • Line size: 16 bytes
Read cycle	Read mode is for high-speed reading. Reading from a ROM address for reading can be accomplished in one ICLK clock.	• When the cache is hit: One cycle • When the cache is missed: One cycle if ICLK ≤ 50 MHz Two cycles if 50 MHz < ICLK ≤ 100 MHz Three cycles if ICLK > 100 MHz
Value after erase	ROM: FFh	ROM: FFh
Programming/erasing method	• The ROM can be programmed and erased by changing the mode of the dedicated sequencer for programming and erasure, and by issuing commands for programming and erasure • Programming through transfer by a dedicated flash-memory programmer via a serial interface (serial programming) • Programming of flash memory by a user program (self-programming)	• Programming and erasing the code flash memory is handled by the FACI commands specified in the FACI command issuing area (007E 0000h) • Programming/erasure through transfer by a dedicated flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)
Security function	Prevents unauthorized modification or reading of data.	Protects against illicit tampering with or reading out of data in flash memory
Protection function	Prevents unintentional programming of the flash memory.	Protects against erroneous programming of the flash memory
Dual bank function*1	—	The dual-bank structure makes a safe update possible in cases where programming is suspended. • Linear mode: the code flash memory is used as one area • Dual mode: the code flash memory is divided into two areas
Trusted Memory (TM) function	—	• Protects against illicit reading of blocks 8 and 9 in the code flash memory • Dual mode: blocks 8, 9 ,46, and 47*1
Units of programming and erasure	• ROM programming: 8 bytes • ROM erasing: Block units	• Units of programming for the user area: 128 bytes • Units of erasure for the user area: Block units

Item	RX231	RX65N
Other functions	Interrupts can be accepted during self-programming	Interrupts can be accepted during self-programming
	In the initial settings of this MCU, an expansion area of the option-setting memory can be set	In the initial settings of this MCU, an expansion area of the option-setting memory can be set
	The startup area of the code flash memory is selectable from blocks 0 to 7, and from blocks 8 to 15.	The startup area of the code flash memory is selectable from blocks 0 and 1.
On-board programming	• Boot mode (SCI) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. — The communication speed is adjusted automatically. • Boot mode (USB interface) — Channel 0 of the USB 2.0 function (USB0) module is used. — A personal computer can be connected using only a USB cable. — The flash memory can be rewritable in self-powered or bus-powered mode. • Boot mode (FINE interface) — The FINE is used. • Self-programming in single-chip mode — The user area is rewritable using the flash rewrite routine in the user program.	• Programming/erasure in boot mode (for the SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. • Programming/erasure in boot mode (for the USB interface) — USBb is used — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasure in boot mode (for the FINE interface) — FINE is used. • Programming/erasure by a routine for code flash memory programming within the user program — This allows code flash memory programming without resetting the system
Off-board programming	The user area is rewritable using a flash programmer (serial programmer or parallel programmer) compatible with this MCU.	A flash programmer can be used to program or erase the user area
Unique ID	A 16-byte ID code provided for each MCU	A 16-byte ID code provided for each MCU
ID codes protection	• Connection with the serial programmer can be enabled or disabled using ID codes in boot mode. • Connection with the on-chip debugging emulator can be enabled or disabled using ID codes. • Connection with the parallel programmer can be enabled or disabled using ROM codes.	• Connection with the serial programmer can be enabled or disabled using ID codes in boot mode. • Connection with the on-chip debugging emulator can be enabled or disabled using ID codes. • Connection with the parallel programmer can be enabled or disabled using ROM codes.
Start-up program protection	This function is used to safely rewrite block 0 to block 7. (1 block: 2 KB)	This function is used to safely rewrite block 0. (1 block: 8 KB)

Item	RX231	RX65N
Area protection	This function enables rewriting only the selected blocks in the user area and disables the other blocks during self-programming.	This function is valid only in the user area of the code flash memory, and provides an access window for specifying the rewritable area. When area protection is enabled, programming and erasure by serial programming or self-programming is prohibited to all other areas.
Background Operation (BGO)	Programs on the ROM can be executed while rewriting the E2 data flash.	• The code flash memory can be read while the code flash memory is being programmed or erased*1. • The data flash memory can be read while the code flash memory is being programmed or erased*1. • The code flash memory can be read while the data flash memory is being programmed or erased*1.

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

Table 2.70 Comparative Listing of Flash Memory Registers

Register	Bit	RX231	RX65N
DFLCTL	—	E2 Data Flash Control Register	—
FENTRYR	FENTRY0	ROM P/E Mode Entry 0	—
	FENTRYC	—	Code Flash Memory P/E Mode
	FENTRYD	E2 Data Flash P/E Mode Entry	—
	FEKEY[7:0]	Key Code	—
	KEY[7:0]	—	Key Code
FPR	—	Protection Unlock Register	—
FPSR	—	Protection Unlock Status Register	—
FPMCR	—	Flash P/E Mode Control Register	—
FISR	—	Flash Initial Setting Register	—
FRESETR	—	Flash Reset Register	—
FASR	—	Flash Area Select Register	—
FCR	—	Flash Control Register	—
FEXCR	—	Flash Extra Area Control Register	—
FSARH	—	Flash Processing Start Address Register H	—
FSARL	—	Flash Processing Start Address Register L	—
FEARH	—	Flash Processing End Address Register H	—
FEARL	—	Flash Processing End Address Register L	—
FWBn	—	Flash Write Buffer n Register (n = 0 to 3)	—
FSTATR0	—	Flash Status Register 0	—
FSTATR1	—	Flash Status Register 1	—
FSTATR	—	—	Flash Status Register
FEAMH	—	Flash Error Address Monitor Register H	—
FEAML	—	Flash Error Address Monitor Register L	—

Register	Bit	RX231	RX65N
FSCMR	—	Flash Start-Up Setting Monitor Register	—
FAWSMR	—	Flash Access Window Start Address Monitor Register	—
FAWEMR	—	Flash Access Window End Address Monitor Register	—
FWEPROR	—	—	Flash P/E Protect Register
FASTAT	—	—	Flash Access Status Register
FAEINT	—	—	Flash Access Error Interrupt Enable Register
FRDYIE	—	—	Flash Ready Interrupt Enable Register
FSADDR	—	—	FACI Command Start Address Register
FSUINITR	—	—	Flash Sequencer Set-Up Initialization Register
FCMDR	—	—	FACI Command Register
FAWMON	—	—	Flash Access Window Monitor Register
FCPSR	—	—	Flash Sequencer Processing Switching Register
FPCKAR	—	—	Flash Sequencer Processing Clock Notification Register
FSUACR	—	—	Start-Up Area Control Register
ROMCE	—	—	ROM Cache Enable Register
ROMCIV	—	—	ROM Cache Invalidate Register
EEPFCLK	—	—	Data Flash Memory Access Frequency Setting Register*1

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

2.35 Package

As indicated in Table 2.71, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.71 Package

Package Type	Renesas Code	
	RX231	RX65N
100-pin TFLGA (0.55 mm)	○	×
100-pin TFLGA (0.65 mm)	×	○
64-pin WFLGA	○	×
64-pin HWQFN	○	×
48-pin HWQFN	○	×
48-pin LFQFP	○	×

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

A comparison of pin functions, power supplies, clocks, and system control pins is shown below. Items that apply to one group only are colored blue, while items that are implemented on both groups but with points of difference are colored red. Items are shown in **black** when there are no points of difference in their specifications.

3.1 100-Pin Package

Table 3.1 shows a Comparative Listing of Pin Functions on 100-Pin Package.

Table 3.1 Comparative Listing of Pin Functions on 100-Pin Package

100-Pin LFQFP	100-Pin TFLGA	RX231	RX65N
1	A2	VREFH	AVCC1
2	B1	P03/DA0	EMLE
3	C2	VREFL	AVSS1
4	C3	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#
5	C1	VCL	VCL
6	D4	VBATT	VBATT
7	D3	MD/FINED	MD/FINED
8	D1	XCIN	XCIN
9	D2	XCOUT	XCOUT
10	E3	RES#	RES#
11	E1	P37/XTAL	P37/XTAL
12	E2	VSS	VSS
13	F1	P36/EXTAL	P36/EXTAL
14	F2	VCC	VCC
15	F3	P35/NMI	P35/UPSEL/NMI
16	E4	P34/MTIOC0A/TMCI3/POE2#/SCK6/TS0/IRQ4	P34/TRST#/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4
17	G1	P33/MTIOC0D/TIOCD0/TMRI3/POE3#/RXD6/SMISO6/SSCL6/TS1/IRQ3	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/IRQ3-DS
18	F4	P32/MTIOC0C/TIOCC0/TMO3/RTCOUT/RTCIC2/TXD6/SMOSI6/SSDA6/USB0_VBUSEN/IRQ2	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/IRQ2-DS
19	G2	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/SSISCK0/IRQ1	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
20	G3	P30/MTIOC4B/TMRI3/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/AUDIO_MCLK/IRQ0/CMPOB3	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
21	G4	P27/CS3#/MTIOC2B/TMCI3/SCK1/SSIWS0/TS2/CVREFB3	P27/TCK/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A
22	H1	P26/CS2#/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/SSIRXD0/TS3/CMPB3	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A

100-Pin LFQFP	100-Pin TFLGA	RX231	RX65N
23	H2	P25/CS1#/MTIOC4C/MTCLKB/TIOCA4/TS4/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/ADTRG0#
24	J1	P24/CS0#/MTIOC4A/MTCLKA/TIOCB4/TMRI1/USB0_VBUSEN/TS5	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN
25	K1	P23/MTIOC3D/MTCLKD/TIOCD3/CTS0#/RTS0#/SS0#/SSISCK0/TS6	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3
26	K2	P22/MTIOC3B/MTCLKC/TIOCC3/TMO0/SCK0/USB0_OVRCURB/AUDIO_MCLK/TS7	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB
27	J2	P21/MTIOC1B/TIOCA3/TMCI0/RXD0/SMISO0/SSCL0/USB0_EXICEN/SSIWS0/TS8	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/IRQ9/(SCL1)*1
28	K3	P20/MTIOC1A/TIOCB3/TMRI0/TXD0/SMOSI0/SSDA0/USB0_ID/SSIRXD0/TS9	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/IRQ8/(SDA1)*1
29	J3	P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/TMO1/POE8#/SCK1/MISOA/SDA/SSITXD0/IRQ7/CMPOB2	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/IRQ7/ADTRG1#
30	H3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#
31	H4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/RXD1/SMISO1/SSCL1/CRXD0/TS12/IRQ5/CMPB2	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/IRQ5
32	K4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA/TS13/IRQ4/CVREFB2	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4
33	J4	P13/MTIOC0B/TIOCA5/TMO3/SDA/IRQ3	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#
34	F5	P12/TMCI1/SCL/IRQ2	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2
35	J6	VCC_USB	VCC_USB
36	K5	USB0_DM	USB0_DM
37	K6	USB0_DP	USB0_DP
38	J5	VSS_USB	VSS_USB
39	H5	P55/WAIT#/MTIOC4D/TMO3/CRXD0/TS15	P55/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/ET0_EXOUT/IRQ10/(D0[A0/D0])*1
40	H6	P54/ALE/MTIOC4B/TMCI1/CTXD0/TS16	P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ET0_LINKSTA/(D1[A1/D1])*1
41	G5	P53/BCLK/TS17	P53/BCLK
42	G6	P52/RD#/TS18	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A

100-Pin LFQFP	100-Pin TFLGA	RX231	RX65N
43	K7	P51/WR1#/BC1#/WAIT#/TS19	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
44	J7	P50/WR0#/WR#/TS20	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A
45	H7	PC7/UB/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TXD8/SMOSI8/SSDA8/MISOA/CACREF	PC7/UB/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/MISOA-A/ET0_COL/TXD10/SMOSI10/SSDA10/IRQ14
46	H8	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/SSCL8/MOSIA/TS22	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/MOSIA-A/ET0_ETXD3/RXD10/SMISO10/SSCL10/IRQ13/(D2[A2/D2])*1
47	K8	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA/TS23	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA-A/ET0_ETXD2/SCK10/(D3[A3/D3])*1
48	J8	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/SDHI_D1/TSCAP	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0-A/ET0_TX_CLK/CTS10#/RTS10#/SS10#
49	K9	PC3/A19/MTIOC4D/TCLKB/TXD5/SMOSI5/SSDA5/IRTXD5/SDHI_D0/TS27	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER
50	K10	PC2/A18/MTIOC4B/TCLKA/RXD5/SMISO5/SSCL5/SSLA3/IRRXD5/SDHI_D3/TS30	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV
51	J10	PC1/A17/MTIOC3A/TCLKD/SCK5/SSLA2/TS33	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/ET0_ERXD2/IRQ12
52	J9	PC0/A16/MTIOC3C/TCLKC/CTS5#/RTS5#/SS5#/SSLA1/TS35	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
53	H10	PB7/A15/MTIOC3B/TIOCB5/TXD9/SMOSI9/SSDA9/SDHI_D2	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/ET0_CRS/RMII0_CRS_DV/TXD11/SMOSI11/SSDA11/SDSI_D1-B
54	H9	PB6/A14/MTIOC3D/TIOCA5/RXD9/SMISO9/SSCL9/SDHI_D1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/ET0_ETXD1/RMII0_TXD1/RXD11/SMISO11/SSCL11/SDSI_D0-B
55	G7	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/POE1#/SCK9/USB0_VBUS/SDHI_CD	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/ET0_ETXD0/RMII0_TXD0/SCK11/SDSI_CLK-B/(LCD_CLK-B)*1
56	G8	PB4/A12/TIOCA4/CTS9#/RTS9#/SS9#	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/ET0_TX_EN/RMII0_TXD_EN/CTS11#/RTS11#/SS11#/SDSI_CMD-B/(LCD_TCON0-B)*1
57	F6	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/POE3#/SCK6/SDHI_WP	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK6/ET0_RX_ER/RMII0_RX_ER/SDSI_D3-B/(LCD_TCON1-B)*1
58	F7	PB2/A10/TIOCC3/TCLKC/CTS6#/RTS6#/SS6#	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/RTS6#/SS6#/ET0_RX_CLK/REF50CK0/SDSI_D2-B/(LCD_TCON2-B)*1

100-Pin LFQFP	100-Pin TFLGA	RX231	RX65N
59	G9	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/TXD6/SMOSI6/SSDA6/SDHI_CLK/IRQ4/CMPOB1	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD6/SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/IRQ4-DS/(LCD_TCON3-B)*1
60	G10	VCC	VCC
61	F8	PB0/A8/MTIC5W/TIOCA3/RXD6/SMISO6/SSCL6/RSPCKA/SDHI_CMD	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/SMISO6/SSCL6/ET0_ERXD1/RMII0_RXD1/IRQ12/(LCD_DATA0-B)*1
62	F10	VSS	VSS
63	F9	PA7/A7/TIOCB2/MISOA	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/(LCD_DATA1-B)*1
64	E7	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/POE2#/CTS5#/RTS5#/SS5#/MOSIA/SSIWS0	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/ET0_EXOUT/(LCD_DATA2-B)*1
65	E9	PA5/A5/TIOCB1/RSPCKA	PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B/ET0_LINKSTA/(LCD_DATA3-B)*1
66	E8	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5/IRQ5/CVREFB1	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/IRQ5-DS/(LCD_DATA4-B)*1
67	E10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5/IRQ6/CMPB1	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/IRQ6-DS/(LCD_DATA5-B)*1
68	E6	PA2/A2/RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B/(LCD_DATA6-B)*1
69	D9	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/SCK5/SSLA2/SSISCK0	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/SCK5/SSLA2-B/ET0_WOL/IRQ11/(LCD_DATA7-B)*1
70	D10	PA0/A0/BC0#/MTIOC4A/TIOCA0/SSLA1/CACREF	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16/SSLA1-B/ET0_TX_EN/RMII0_TXD_EN/(LCD_DATA8-B)*1
71	D8	PE7/D15[A15/D15]/IRQ7/AN023	PE7/D15[A15/D15]/MTIOC6A/TOC1/MISOB-B/MMC_RES#-B/SDHI_WP-B/IRQ7/AN105/(D7[A7/D7]/LCD_DATA9-B)*1
72	D7	PE6/D14[A14/D14]/IRQ6/AN022	PE6/D14[A14/D14]/MTIOC6C/TIC1/MOSIB-B/MMC_CD-B/SDHI_CD-B/IRQ6/AN104/(D6[A6/D6]/SDHI_CD/LCD_DATA10-B)*1
73	C9	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/IRQ5/AN021/CMPOB0	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ET0_RX_CLK/REF50CK0/RSPCKB-B/IRQ5/AN103/(D5[A5/D5]/LCD_DATA11-B)*1
74	C10	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/AN020/CMPA2/CLKOUT	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/AN102/(D4[A4/D4]/LCD_DATA12-B)*1
75	B10	PE3/D11[A11/D11]/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/AUDIO_MCLK/AN019/CLKOUT	PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/TOC3/CTS12#/RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/AN101/(D3[A3/D3]/LCD_DATA13-B)*1

100-Pin LFQFP	100-Pin TFLGA	RX231	RX65N
76	A10	PE2/D10[A10/D10]/MTIOC4A/RXD12/SMISO12/SSCL12/RXDX12/IRQ7/AN018/CVREFB0	PE2/D10[A10/D10]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/IRQ7-DS/AN100/(D2[A2/D2]/LCD_DATA14-B)*1
77	A9	PE1/D9[A9/D9]/MTIOC4C/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/AN017/CMPB0	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ANEX1/(D1[A1/D1]/LCD_DATA15-B)*1
78	A8	PE0/D8[A8/D8]/SCK12/AN016	PE0/D8[A8/D8]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/ANEX0/(D0[A0/D0]/LCD_DATA16-B)*1
79	B9	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7/AN031	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107/(SSLC3-A/LCD_DATA17-B)*1
80	B8	PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6/AN030	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2/MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/IRQ6/AN106/(SSLC2-A/LCD_DATA18-B)*1
81	C8	PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5/AN029	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1/MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/IRQ5/AN113/(SSLC1-A/LCD_DATA19-B)*1
82	A7	PD4/D4[A4/D4]/POE3#/IRQ4/AN028	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0/MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/AN112/(SSLC0-A/LCD_DATA20-B)*1
83	B7	PD3/D3[A3/D3]/POE8#/IRQ3/AN027	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC/MMC_D3-B/SDHI_D3-B/QIO3-B/IRQ3/AN111/(RSPCKC-A/LCD_DATA21-B)*1
84	C7	PD2/D2[A2/D2]/MTIOC4D/IRQ2/AN026	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC/MMC_D2-B/SDHI_D2-B/QIO2-B/IRQ2/AN110/(MISOC-A/LCD_DATA22-B)*1
85	B6	PD1/D1[A1/D1]/MTIOC4B/IRQ1/AN025	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC/IRQ1/AN109/(MOSIC-A/LCD_DATA23-B)*1
86	A6	PD0/D0[A0/D0]/IRQ0/AN024	PD0/D0[A0/D0]/POE4#/IRQ0/AN108/(LCD_EXTCLK-B)*1
87	C6	P47/AN007	P47/IRQ15-DS/AN007
88	D6	P46/AN006	P46/IRQ14-DS/AN006
89	D5	P45/AN005	P45/IRQ13-DS/AN005
90	B5	P44/AN004	P44/IRQ12-DS/AN004
91	A5	P43/AN003	P43/IRQ11-DS/AN003
92	C5	P42/AN002	P42/IRQ10-DS/AN002
93	E5	P41/AN001	P41/IRQ9-DS/AN001
94	A4	VREFL0	VREFL0
95	B4	P40/AN000	P40/IRQ8-DS/AN000
96	C4	VREFH0	VREFH0
97	B3	AVCC0	AVCC0
98	A3	P07/ADTRG0#	P07/IRQ15/ADTRG0#

100-Pin LFQFP	100-Pin TFLGA	RX231	RX65N
99	B2	AVSS0	AVSS0
100	A1	P05/DA1	P05/IRQ13/DA1

Note: 1. Can be used for products with at least 1.5 MB of code flash memory.

3.2 64-Pin Package (RX231: WFLGA, RX651: TFBGA)

Table 3.2 shows a Comparative Listing of Pin Functions on 64-Pin Package (RX231: WFLGA, RX651: TFBGA). Note that the RX65N Group is not available in 64-pin package versions.

Table 3.2 Comparative Listing of Pin Functions on 64-Pin Package

64-Pin	RX231 (64-Pin WFLGA)	RX651 (64-Pin TFBGA)
A1	P05/DA1	AVCC1
A2	AVCC0	AVSS0
A3	VREFH0	VREFH0
A4	VREFL0	VREFL0
A5	VREFH	PD2/MTIOC4D/TIC2/QIO2-B/SDHI_D2-B/IRQ2/AN110
A6	VREFL	PD7/MTIC5U/POE0#/QMI-B/QIO1-B/SDHI_D1-B/IRQ7/AN107
A7	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/IRQ7/AN018/CVREFB0	PE0/MTIOC3D/SCK12/ANEX0
A8	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/AUDIO_MCLK/AN019/CLKOUT	PE2/MTIOC4A/TIC3/RXD12/SSCL12/RXDX12/IRQ7-DS
B1	VCL	EMLE
B2	AVSS0	AVSS1
B3	P40/AN000	AVCC0
B4	P42/AN002	P42/IRQ10-DS/AN002
B5	P44/AN004	PD3/MTIOC8D/TOC2/POE8#/QIO3-B/SDHI_D3-B/IRQ3/AN111
B6	P46/AN006	PD6/MTIC5V/MTIOC8A/POE4#/QMO-B/QIO0-B/SDHI_D0-B/IRQ6/AN106
B7	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/AN017/CMPB0	PE1/MTIOC4C/MTIOC3B/TXD12/SSDA12/TXDX12/SIOX12/ANEX1
B8	PE4/MTIOC4D/MTIOC1A/AN020/CMPA2/CLKOUT	PE6/MTIOC6C/TIC1/SDHI_CD/IRQ6
C1	XCIN	VCL
C2	MD/FINED	VBATT
C3	P03/DA0	MD/FINED
C4	P41/AN001	P41/IRQ9-DS/AN001
C5	P43/AN003	PD4/MTIOC8B/POE11#/QSSL-B/SDHI_CMD-B/IRQ4/AN112
C6	PE0/SCK12/AN016	PD5/MTIC5W/MTIOC8C/POE10#/QSPCLK-B/SDHI_CLK-B/IRQ5/AN113
C7	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/CMPOB0	PA1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/SCK5/IRQ11
C8	PA0/MTIOC4A/TIOCA0/SSLA1/CACREF	PE7/MTIOC6A/TOC1/SDHI_WP/IRQ7
D1	XCOUT	XCIN
D2	RES#	XCOUT
D3	P27/MTIOC2B/TMCI3/SCK1/SSIWS0/TS2/CVREFB3	RES#
D4	P14/MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA/CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA/TS13/IRQ4/CVREFB2	P40/IRQ8-DS/AN000
D5	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/TIOCA2/CTS5#/RTS5#/SS5#/MOSIA/SSIWS0	P43/IRQ11-DS/AN003

64-Pin	RX231 (64-Pin WFLGA)	RX651 (64-Pin TFBGA)
D6	PA4/MTIC5U/MTCLKA/TMRI0/TIOCA1/TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5/IRQ5/CVREFB1	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/POE10#/CTS5#/RTS5#/SS5#
D7	PA1/MTIOC0B/MTCLKC/TIOCB0/SCK5/SSLA2/SSISCK0	PA2/MTIOC7A/RXD5/SMISO5/SSCL5
D8	PA3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5/IRQ6/CMPB1	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/TXD5/SMOSI5/SSDA5/IRQ5-DS
E1	VSS	XTAL/P37
E2	VBATT	VSS
E3	P30/MTIOC4B/TMRI3/POE8#/RTCIC0/RXD1/SMISO1/SSCL1/AUDIO_MCLK/IRQ0/CMPOB3	TRST#/P34/MTIOC0A/TMCI3/POE10#/IRQ4
E4	P16/MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#	P13/MTIOC0B/TIOCA5/TMO3/TXD2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#
E5	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/SDHI_D1/TSCAP	BSCANP
E6	VCC	PA7/TIOCB2
E7	VSS	VCC
E8	PB0/MTIC5W/TIOCA3/RXD6/SMISO6/SSCL6/RSPCKA/SDHI_CMD	VSS
F1	VCC	EXTAL/P36
F2	UPSEL/P35/NMI	VCC
F3	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/SSISCK0/IRQ1	UPSEL/P35/NMI
F4	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA/USB0_ID/TS23	P12/TMCI1/RXD2/SSCL2/SCL0[FM+]/IRQ2
F5	P15/MTIOC0B/MTCLKB/TMCI2/TIOCB2/TCLKB/RXD1/SMISO1/SSCL1/CRXD0/TS12/IRQ5/CMPB2	P53
F6	PB1/MTIOC0C/MTIOC4C/TMCI0/TIOCB3/TXD6/SMOSI6/SSDA6/SDHI_CLK/IRQ4/CMPOB1	PB7/MTIOC3B/TIOCB5/TXD9/SSDA9/SSDA11/TXD11
F7	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4/SCK9/USB0_VBUS/SDHI_CD	PB6/MTIOC3D/TIOCA5/RXD9/SSCL9/SSCL11/RXD11
F8	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/TIOCD3/TCLKD/SCK6/SDHI_WP	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/POE4#/SCK9/SCK11
G1	EXTAL/P36	TCK/P27/MTIOC2B/TMCI3/SCK1/RSPCKB-A
G2	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/USB0_VBUSEN/SSIRXD0/TS3/CMPB3	TMS/P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
G3	VCC_USB	TDI/P30/MTIOC4B/TMRI3/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
G4	VSS_USB	VCC_USB
G5	UB/PC7/MTIOC3A/MTCLKB/TMO2/TXD8/SMOSI8/SSDA8/MISOA/CACREF	VSS_USB
G6	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/SSCL8/MOSIA/USB0_EXICEN/TS22	UB/PC7/MTIOC3A/MTCLKB/TMO2/TOC0/CACREF/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/IRQ14

64-Pin	RX231 (64-Pin WFLGA)	RX651 (64-Pin TFBGA)
G7	PC3/MTIOC4D/TCLKB/TXD5/SMOSI5/SSDA5/IRTXD5/SDHI_D0/TS27	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/SCK10/RSPCKA-A
G8	PB6/PC0/MTIOC3D/TIOCA5/RXD9/SMISO9/SSCL9/SDHI_D1	PC0/MTIOC3C/TCLKC/SSLA1-A/IRQ14
H1	XTAL/P37	TDO/P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/MOSIB-A
H2	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/TCLKD/SCK1/MISOA/SDA/SSITXD0/IRQ7/CMPOB2	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/POE8#/SCK1/TXD3/SSDA3/SDA2-DS/IRQ7/ADTRG1#
H3	USB0_DM	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/SSCL3/SCL2-DS/USB0_VBUS/IRQ6/ADTRG0#
H4	USB0_DP	USB0_DM
H5	P55/MTIOC4D/TMO3/CRXD0/TS15	USB0_DP
H6	P54/MTIOC4B/TMCI1/CTXD0/TS16	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/IRQ13
H7	PC2/MTIOC4B/TCLKA/RXD5/SMISO5/SSCL5/SSLA3/IRRXD5/SDHI_D3/TS30	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A
H8	PB7/PC1/MTIOC3B/TIOCB5/TXD9/SMOSI9/SSDA9/SDHI_D2	PC1/MTIOC3A/TCLKD/SSLA2-A/IRQ12

3.3 64-Pin Package (RX231: LFQFP/HWQFN, RX651: LFQFP)

Table 3.3 shows a Comparative Listing of Pin Functions on 64-Pin Package (RX231: LFQFP/HWQFN, RX651: LFQFP). Note that the RX65N Group is not available in 64-pin package versions.

Table 3.3 Comparative Listing of Pin Functions on 64-Pin Package

64-Pin	RX231 (64-Pin LFQFP/HWQFN)	RX651 (64-Pin LFQFP)
1	P03/DA0	AVCC1
2	VCL	EMLE
3	MD/FINED	AVSS1
4	XCIN	VCL
5	XCOUT	VBATT
6	RES#	MD/FINED
7	XTAL/P37	XCIN
8	VSS	XCOUT
9	EXTAL/P36	RES#
10	VCC	XTAL/P37
11	UPSEL/P35/NMI	VSS
12	VBATT	EXTAL/P36
13	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/SSISCK0/IRQ1	VCC
14	P30/MTIOC4B/TMRI3/POE8#/RTCIC0/RXD1/SMISO1/SSCL1/AUDIO_MCLK/IRQ0/CMPOB3	UPSEL/P35/NMI
15	P27/MTIOC2B/TMCI3/SCK1/SSIWS0/TS2/CVREFB3	TRST#/P34/MTIOC0A/TMCI3/POE10#/IRQ4
16	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/USB0_VBUSEN/SSIRXD0/TS3/CMPB3	TDI/P30/MTIOC4B/TMRI3/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
17	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/TCLKD/SCK1/MISOA/SDA/SSITXD0/IRQ7/CMPOB2	TMS/P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
18	P16/MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#	TDO/P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/MOSIB-A
19	P15/MTIOC0B/MTCLKB/TMCI2/TIOCB2/TCLKB/RXD1/SMISO1/SSCL1/CRXD0/TS12/IRQ5/CMPB2	TCK/P27/MTIOC2B/TMCI3/SCK1/RSPCKB-A
20	P14/MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA/CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA/TS13/IRQ4/CVREFB2	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCBb0/TCLKD/TMO1/POE8#/SCK1/TXD3/SSDA3/SDA2-DS/IRQ7/ADTRG1#
21	VCC_USB	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/SSCL3/SCL2-DS/USB0_VBUS/IRQ6/ADTRG0#
22	USB0_DM	P13/MTIOC0B/TIOCA5/TMO3/TXD2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#
23	USB0_DP	P12/TMCI1/RXD2/SSCL2/SCL0[FM+]/IRQ2
24	VSS_USB	VCC_USB
25	P55/MTIOC4D/TMO3/CRXD0/TS15	USB0_DM
26	P54/MTIOC4B/TMCI1/CTXD0/TS16	USB0_DP
27	UB/PC7/MTIOC3A/MTCLKB/TMO2/TXD8/SMOSI8/SSDA8/MISOA/CACREF	VSS_USB

64-Pin	RX231 (64-Pin LFQFP/HWQFN)	RX651 (64-Pin LFQFP)
28	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/SSCL8/MOSIA/USB0_EXICEN/TS22	P53
29	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA/USB0_ID/TS23	UB/PC7/MTIOC3A/MTCLKB/TMO2/TOC0/CACREF/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/IRQ14
30	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/SDHI_D1/TSCAP	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/IRQ13
31	PC3/MTIOC4D/TCLKB/TXD5/SMOSI5/SSDA5/IRTXD5/SDHI_D0/TS27	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/SCK10/RSPCKA-A
32	PC2/MTIOC4B/TCLKA/RXD5/SMISO5/SSCL5/SSLA3/IRRXD5/SDHI_D3/TS30	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A
33	PB7/PC1/MTIOC3B/TIOCB5/TXD9/SMOSI9/SSDA9/SDHI_D2	PC1/MTIOC3A/TCLKD/SSLA2-A/IRQ12
34	PB6/PC0/MTIOC3D/TIOCA5/RXD9/SMISO9/SSCL9/SDHI_D1	PC0/MTIOC3C/TCLKC/SSLA1-A/IRQ14
35	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4/SCK9/USB0_VBUS/SDHI_CD	PB7/MTIOC3B/TIOCB5/TXD9/SSDA9/SSDA11/TXD11
36	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/TIOCD3/TCLKD/SCK6/SDHI_WP	PB6/MTIOC3D/TIOCA5/RXD9/SSCL9/SSCL11/RXD11
37	PB1/MTIOC0C/MTIOC4C/TMCI0/TIOCB3/TXD6/SMOSI6/SSDA6/SDHI_CLK/IRQ4/CMPOB1	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/POE4#/SCK9/SCK11
38	VCC	VCC
39	PB0/MTIC5W/TIOCA3/RXD6/SMISO6/SSCL6/RSPCKA/SDHI_CMD	VSS
40	VSS	PA7/TIOCB2
41	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/TIOCA2/CTS5#/RTS5#/SS5#/MOSIA/SSIWS0	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/POE10#/CTS5#/RTS5#/SS5#
42	PA4/MTIC5U/MTCLKA/TMRI0/TIOCA1/TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5/IRQ5/CVREFB1	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/TXD5/SMOSI5/SSDA5/IRQ5-DS
43	PA3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5/IRQ6/CMPB1	PA2/MTIOC7A/RXD5/SMISO5/SSCL5
44	PA1/MTIOC0B/MTCLKC/TIOCB0/SCK5/SSLA2/SSISCK0	PA1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/SCK5/IRQ11
45	PA0/MTIOC4A/TIOCA0/SSLA1/CACREF	PE7/MTIOC6A/TOC1/SDHI_WP/IRQ7
46	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/CMPOB0	PE6/MTIOC6C/TIC1/SDHI_CD/IRQ6
47	PE4/MTIOC4D/MTIOC1A/AN020/CMPA2/CLKOUT	PE2/MTIOC4A/TIC3/RXD12/SSCL12/RXDX12/IRQ7-DS
48	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/AUDIO_MCLK/AN019/CLKOUT	PE1/MTIOC4C/MTIOC3B/TXD12/SSDA12/TXDX12/SIOX12/ANEX1
49	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/IRQ7/AN018/CVREFB0	PE0/MTIOC3D/SCK12/ANEX0
50	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/AN017/CMPB0	PD7/MTIC5U/POE0#/QMI-B/QIO1-B/SDHI_D1-B/IRQ7/AN107
51	PE0/SCK12/AN016	PD6/MTIC5V/MTIOC8A/POE4#/QMO-B/QIO0-B/SDHI_D0-B/IRQ6/AN106
52	VREFL	PD5/MTIC5W/MTIOC8C/POE10#/QSPCLK-B/SDHI_CLK-B/IRQ5/AN113

64-Pin	RX231 (64-Pin LFQFP/HWQFN)	RX651 (64-Pin LFQFP)
53	P46/AN006	PD4/MTIOC8B/POE11#/QSSL-B/SDHI_CMD-B/IRQ4/AN112
54	VREFH	PD3/MTIOC8D/TOC2/POE8#/QIO3-B/SDHI_D3-B/IRQ3/AN111
55	P44/AN004	PD2/MTIOC4D/TIC2/QIO2-B/SDHI_D2-B/IRQ2/AN110
56	P43/AN003	P43/IRQ11-DS/AN003
57	P42/AN002	P42/IRQ10-DS/AN002
58	P41/AN001	P41/IRQ9-DS/AN001
59	VREFL0	VREFL0
60	P40/AN000	P40/IRQ8-DS/AN000
61	VREFH0	VREFH0
62	AVCC0	AVCC0
63	P05/DA1	AVSS0
64	AVSS0	P05/IRQ13/DA1

4. Notes on Migration

4.1 Operating Voltage Range

4.1.1 Power Supply Voltage

The power supply voltage ranges are different between RX231 and RX65N.

Table 4.1 shows a Comparative of Power Supply Voltage Ranges.

Table 4.1 Comparative of Power Supply Voltage Ranges

Item	RX231	RX65N
VCC	1.8 V to 5.5 V*1	2.7 V to 3.6 V
AVCC0	1.8 V to 5.5 V*2	Set to the same potential as VCC
AVCC1	None	Set to the same potential as VCC
VREFH0	1.8 V to AVCC0	2.7 V to AVCC0
VREFH	1.8 V to AVCC0	None
VCC_USB	Set to the same potential as VCC	Set to the same potential as VCC
VBATT	1.8 V to 5.5 V	2.0 V to 3.6 V

Notes: 1. When USB is not used.
2. AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.0V
AVCC0 = VCC when VCC < 2.0V

4.1.2 Analog power supply voltage

On the RX231 Group, AVCC0 and VCC can be supplied independently within the operating voltage range when VCC ≥ 2.0V. However, on the RX65N Group, AVCC0 and AVCC1 should be supplied with the same potential as VCC.

4.2 Notes on Pin Design

4.2.1 VCL Pin (External Capacitor)

Connect a smoothing capacitor rated at 0.22 μF to the VCL pin of the RX65N Group for stabilization of the internal power supply.

4.2.2 Main clock oscillator

When connecting an oscillator to EXTAL pin and XTAL pin of RX65N Group, frequency should be in a range of 8 MHz to 24 MHz.

4.2.3 USB External Connection Circuit

The example of USB external connection circuit is different between RX231 Group and RX65N Group.

For details on external connection circuits, see RX65N Group, RX651 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.2.4 Transition to Boot Mode (FINE Interface)

On the RX65N Group, the chip enters boot mode (FINE interface) when the MD pin is set to the low level at the time of release from the reset state and then the pin is switched to the high level within 20 to 100 msec.

For details on operating modes, see RX65N Group, RX651 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.3 Notes on Function Settings

4.3.1 Changing Option-Setting Memory by Self-Programming

Making changes to the option-setting memory by self-programming on the RX65N Group is accomplished by programming the configuration setting area in the option-setting memory using the configuration setting command.

For details on the configuration setting command, see RX65N Group, RX651 Group Flash Memory User's Manual: Hardware Interface, listed in section 5, Reference Documents.

4.3.2 Setting Number of Flash Memory Access Wait States

On the RX65N Group it is necessary to specify the number of access wait states to be used when accessing the flash memory, based on the system clock (ICLK) frequency of the microcontroller. This setting is made to the ROMWT register.

Table 4.2 shows The Number of Flash Memory Access Wait States according to ICLK frequency.

Table 4.2 The Number of Flash Memory Access Wait States

Item	ICLK ≤ 50 MHz	50 MHz < ICLK ≤ 100 MHz	100 MHz < ICLK ≤ 200 MHz
Wait states	0 to 2	1 or 2	2

Note: For details on register setting and the detail of specifications, see RX65N Group, RX651 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.3.3 Selectable Interrupts

A selectable interrupt function has been added to the RX65N Group. From among multiple peripheral module interrupt sources, the user may assign one each to interrupt vector numbers 128 to 255.

For details on selectable interrupt function, see RX65N Group, RX651 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.3.4 Command of Flash Memory Usage

On the RX231 Group, the Flash memory can be programmed and erased by changing the mode of the dedicated sequencer for programming and erasure, and by issuing software commands.

On the RX65N Group, the Flash memory can be programmed and erased by setting the FACI commands specified in the FACI command issuing area to control the FCU.

Table 4.3 shows The Specification Comparison Between Software Commands and FACI Commands.

Table 4.3 The Specification Comparison Between Software Commands and FACI Commands

Item	Software Command (RX231)	FACI Command (RX65N)
Command issuing area	—	FACI command issuing area (007E 0000h)
Available commands	• Program • Block erase • All-block erase • Blank check • Start-up area information program • Access window information program	• Program • Block erase • Multi-block erase • Blank check • P/E suspend • P/E resume • Status clear • Forced stop • Configuration setting

4.3.5 Flash Access Window Setting Register (FAW)

On the RX65N Group, once 0 is written to the access window protection bit (FSPR) in flash access window setting register (FAW), the bit can never be restored to 1.

For details, see RX65N Group, RX651 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.3.6 Software Standby Mode

On the RX65N Group, it is selectable that the main and sub-clock oscillators operate or stop in software standby mode. The main clock oscillator forced oscillation bit (MOFXIN) in main clock oscillator forced oscillation control register (MOFCR) should be 0 to stop the main clock oscillator.

4.3.7 Battery Backup Function

The RX65N Group does not support the VBATT pin voltage drop detection. When the voltage level at the VBATT pin voltage falls below the operation guaranteed voltage, operation of the RTC cannot be guaranteed. The RTC must be initialized to restart power supply after the VBATT pin falls below the operation guaranteed voltage.

5. Reference Documents

User's Manual: Hardware

RX230 Group, RX231 Group User's Manual: Hardware Rev.1.20 (R01UH0496EJ0120)
(The latest version can be downloaded from the Renesas Electronics website.)

RX65N Group, RX651 Group User's Manual: Hardware Rev.2.10 (R01UH0590EJ0210)
(The latest version can be downloaded from the Renesas Electronics website.)

RX65N Group, RX651 Group Flash Memory User's Manual: Hardware Interface Rev.2.00 (R01UH0602EJ0200)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates.

None

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 1, 2016	—	First edition issued
2.00	Nov. 6, 2017	All pages	Supports RX65N with at least 1.5 MB of code flash memory
2.10	May 24, 2019	1	Introduction, revised
		3	1, Comparison of Functions of RX65N Group and RX231 Group, revised
		7	2.3, Address Space, added
			2.3, Table 2.4, Comparative Memory Map of Single-Chip Mode, added
		8	2.3, Table 2.5, Comparative Memory Map of On-Chip ROM Enabled Extended Mode, added
		9	2.3, Table 2.6, Comparative Memory Map of On-Chip ROM Disabled Extended Mode, added
		11	2.5, Table 2.9, Comparative Listing of Option-Setting Memory Registers, revised
		16	2.7, Table 2.12, Comparative Listing of Clock Generation Circuit Specifications, revised
		22	2.8, Table 2.15, Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, added
		30	2.11, Table 2.20, Comparative Listing of Interrupt Controller Specifications, revised
		33	2.11, Table 2.21, Comparative Listing of Interrupt Controller Registers, revised
		35	2.12, Table 2.22, Comparative Listing of Bus Specifications, revised
		38	2.12, Table 2.24, Comparative Listing of Bus Registers, revised
		41	2.14, Table 2.27, Comparative Listing of Data Transfer Controller Specifications, revised
		43	2.15, Table 2.29, Comparative Listing of Event Link Controller Specifications, revised
		45	2.16, Table 2.33, Comparative Listing of I/O Ports (64-Pin) Specifications, added
		47	2.17, Table 2.35, Comparative Listing of Multi-Function Pin Controller Registers, revised
		53	2.21, Table 2.41, Comparative Listing of Watchdog Timer Specifications, revised
		54	2.22, Table 2.43, Comparative Listing of Independent Watchdog Timer Specifications, revised
		59	2.23, Table 2.46, Comparative Listing of USB 2.0 Host/Function Module Registers, revised
		60	2.24, Table 2.47, Comparative Listing of SCIg Specifications, revised
		62	2.24, Table 2.48, Comparative Listing of SCIi Specifications, revised
		81	2.30, Table 2.61, Comparative Listing of 12-Bit A/D Converter Specifications, revised
		85	2.30, Table 2.62, Comparative Listing of 12-Bit A/D Converter Registers revised

Rev.	Date	Description	
		Page	**Summary**
2.10	May 24, 2019	91	2.31, Table 2.63, Comparative Overview of 12-Bit D/A Converter, added
			2.31, Table 2.64, Comparative Listing of 12-bit D/A Converter Registers, revised
		92	2.32, Table 2.66, Comparative Listing of Temperature Sensor Registers, revised
		94	2.34, Table 2.69, Comparative Listing of Flash Memory (Code Flash) Specifications, revised
		98	2.35, Package, added
		105	3.2, Table 3.2, Comparative Listing of Pin Functions on 64-Pin Package, added
		108	3.3, Table 3.3, Comparative Listing of Pin Functions on 64-Pin Package, added
		113	4.3.4, Command of Flash Memory Usage, revised
		114	5, Reference Documents, revised

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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