Application Note

Dialog PMICs and Terrestrial Cosmic Rays

AN-PM-117

Abstract

This document explains how Dialog Semiconductor ensures that the technology it uses mitigates the risk of single event transients (SETs) caused by cosmic rays. It uses the DA9063L-A as a case study but the overall approach is applicable to all Dialog system PMICs and sub-PMICs. DA9063L-A soft errors due to terrestrial cosmic radiation are expected to contribute an insignificant failure rate. Other reliability failure mechanisms are likely to dominate by many orders of magnitude.

Contents

1 Terms and Definitions

EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FIT	Failures In Time
HTOL	High Temperature Operating Life
OTP	One-Time Programmable
SER	Soft Error Rate
SET	Single Event Transient

2 References

[1] Ferlet-Cavrois, V., et al., ‘Single Event Transients in Digital CMOS—A Review’, IEEE Transactions on Nuclear Science, 60, 3, 2013.

[2] Baumann, R.C., ‘Radiation-Induced Soft Errors in Advanced Semiconductor Technologies’, IEEE Transactions on Device and Materials Reliability, 5, 3, 2005.

[3] JESD89-2A, ‘Test Method for Alpha Source Accelerated Soft Error Rate’, JEDEC, 2007.

[4] JS-001-2017, ‘Joint JEDEC/ESDA Standard For Electrostatic Discharge Sensitivity Test - Human Body Model (HBM) - Component Level’, JEDEC, 2017.

[5] JESD22-C101F, ‘Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components’, JEDEC, 2013

[6] Qualification Report – DA9063, D2071-Q54-00-REV1, Dialog, 2014.

[7] ‘IP Reliability Report – TSMC 0.25um 2.5V/5V Mixed-Signal Process 256x8 OTP’, E-090501, eMemory, v1.0, 2009.

3 Introduction

Dialog Semiconductor offers a range of system PMICs and sub-PMICs for consumer and automotive applications. General requirements are defined by the AEC-Q100 specifications. An increasing concern in the semiconductor industry is the resilience of parts to ionizing radiation, including cosmic rays and associated high-energy secondary particles. This topic is discussed thoroughly in the academic literature [1].

One specific industry concern is that device failure rates attributable to single event transients (SETs) caused by ionizing radiation can increase on advanced-node CMOS technologies. As market expectations for reliability rise, and as failure rates due to other mechanisms decline, the failure rates due to SETs may become more significant.

This document explains how Dialog ensures that the technology it uses mitigates the risk of SETs caused by cosmic rays. It uses the DA9063L-A as a case study but the overall approach is applicable to all Dialog system PMICs and sub-PMICs.

4 Background

The DA9063L-A is implemented on a 250 nm CMOS process. There is no pressing requirement to utilize advanced deep sub-micron CMOS technologies due to the economics specific to analog mixed-signal manufacture. In common with general digital CMOS design, DA9063L-A comprises registers based on D-type flip-flops. There are 328 registers visible to the application host, as defined by the DA9063L-A register map. Many of these are mirrored as on-chip OTP memory cells.

5 OTP

The DA9063L-A OTP is implemented using floating gate standard cells (leveraging traditional EPROM technology) and has been certified by the TSMC foundry. SETs in OTP may also be seen as hard errors if a bit that is critical to the PMIC behavior is affected. SETs in OTP are mitigated primarily by the use of redundancy, implemented as two parallel floating gate PMOS transistors per bit. Therefore, if one of the transistors suffers from an SET, the other transistor has sufficient charge to maintain the correct value. Redundancy reduces the probability of failure from 1/x with one transistor to $1/x^2$ with two transistors.

6 Registers

SETs affecting CMOS digital registers have been evaluated by Baumann [2]. If we consider one register bit as a flip-flop, Baumann shows that the soft error rate (SER) for the register bit is predicted to be approximately $5 * 10^{-6}$ versus SRAM.

The DA9063L-A has only ~6700 flip-flops. The failure rate for all the flip-flops combined is therefore $6700 / 1 * 10^6 = 6 * 10^{-3}$ that of a 1 Mbit SRAM. Incidentally, note that JESD89-2A (2007) [3] states that only devices with ≥1 Mbit of SRAM require SER evaluation.

Combining the above two factors shows that the FIT rate due to DA9063L-A soft errors is expected to be $5 * 10^{-6} \times 6 * 10^{-3} = 10^{-8}$ of the rate of 1 Mbit of SRAM on the same fab process.

7 Other Data Corruption Mechanisms

Corruption of the DA9063L-A OTP is also assessed within product qualification. The OTP is tested prior to and after qualification stresses, not only via conventional data retention/disturb (thermally accelerated) stresses such as HTOL and High Temperature Storage, but also through other qualification tests such as ESD. Testing to JEDEC JS-001-2017 [4] and JESD22-C101 [5] ESD methods show no OTP corruption [6]. These results are supported by the foundry's process-level certification of the standard OTP cell [7].

Electromagnetic interference (EMI) is performed at a system-level. The Dialog silicon validation process is based on board-level tests. The Dialog performance boards used in this evaluation closely reflect a typical application board layout: no failures attributable to EMI were noted at this basic level. However, since results are strongly dependent on the physical construction of the whole system combined with the external components, EMI testing should be performed at the application level. There have been no reports of the DA9063L-A failing customer EMI tests.

8 Conclusion

DA9063L-A soft errors due to terrestrial cosmic radiation are expected to contribute an insignificant failure rate. Other reliability failure mechanisms are likely to dominate by many orders of magnitude. Data corruption of OTP cells by terrestrial cosmic radiation has been mitigated by using redundancy in the standard cell.

Revision History

Revision	Date	Description
1.1	25-Feb-2022	File was rebranded with new logo, copyright and disclaimer
1.0	27-Jun-2018	Initial version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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