RL78/G1D

Design data of the RL78/G1D Evaluation Module

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Introduction

This document describes the design data of the RL78/G1D Evaluation module (RTK0EN0002C01001BZ) that are mounted on the RL78/G1D Evaluation board (RTK0EN0001D01001BZ). The design data includes schematics, BOM list, Gerber data and board layout diagram.

Target Device

RL78/G1D

Contents

1. Overview

This document aim to deliver the design data of the RL78/G1D Evaluation module (RTK0EN0002C01001BZ) that are mounted on the RL78/G1D Evaluation board (RTK0EN0001D01001BZ). The design data includes schematics, BOM list, Gerber data and board layout diagram.

1.1 Related documents

The following document is related to this application note. Also refer to this document when using this application note.

- Guidelines for RF Board Design（R01AN2465）

2. Configuration of Application Note

This Application Note contains the following contents listed in table 1.

Table 1 Configuration of Application Note

File organization	Description
r01an2890jj0100_rl78g1d.pdf	Application Note(This application note)
RTK0EN0002C01001BZ_Design_Data	
01_Circuit_Diagrams	
RTK0EN0002C01001BZ_Circuit_Diagrams.pdf	Circuit of RL78/G1D Evaluation module
02_Parts_List	
RTK0EN0002C01001BZ_Parts_List.pdf	BOM list of RL78/G1D Evaluation module
03_Gerber_Data	
DFX_DATA	
m404705-2_chk_911v2_AllLay.dxf	CAD data of RL78/G1D Evaluation module
Gerber_Data	
m404705-2_gai.gbr	Gerber data(Dimensions)
m404705-2_l1.gbr	Gerber data(L1: parts , Analog signal layer)
m404705-2_l2g.gbr	Gerber data(L2: GND layer)
m404705-2_l3v.gbr	Gerber data(L3: VDD, GND layer)
m404705-2_l3v_gousei.gbr	Gerber data(L3: Synthetic layer)
m404705-2_l4.gbr	Gerber data(L4: Digital signal ,GND layer)
m404705-2_res1.gbr	Gerber data(L1: Resist)
m404705-2_res4.gbr	Gerber data(L4: Resist)
m404705-2_silk1.gbr	Gerber data(L1: silk)
m404705-2_silk4.gbr	Gerber data(L4: silk)
m404705-2-TAN.XGB	Gerber data(drill data)
Pattern_Figure	
m404705-2_ana.pdf	Pattern figure(Through hole)
m404705-2_kumi1.pdf	Pattern figure(Surface substrate)
m404705-2_kumi4.pdf	Pattern figure(Rear surface substrate)
m404705-2_l1.pdf	Pattern figure(L1: parts , Analog signal layer)
m404705-2_l2g.pdf	Pattern figure(L2: GND layer)
m404705-2_l3v.pdf	Pattern figure(L3: VDD, GND layer)
m404705-2_l3v_gousei.pdf	Pattern figure(L3: Synthetic layer)
m404705-2_l4.pdf	Pattern figure(L4: Digital signal ,GND layer)
m404705-2_mask1.pdf	Pattern figure(L1: Mask)
m404705-2_mask4.pdf	Pattern figure(L4: Mask)
m404705-2_res1.pdf	Pattern figure(L1: Resist)
m404705-2_res4.pdf	Pattern figure(L4: Resist)
m404705-2_silk1.pdf	Pattern figure(L1: silk)
m404705-2_silk4.pdf	Pattern figure(L4: silk)
04_Outline	
RTK0EN0002C01001BZ_Side_View.pdf	Dimensions (side view)
RTK0EN0002C01001BZ_Top_View.pdf	Dimensions (Top view)

(Note1)GBR file is the data that output the RS274X format by using CAD tool "MMcolmo".

(Note2) DXF file is the data that combines the layers in CAD tool "ZUNOU RAPID9" after a DXF file (polygon) by using the GBR editing CAM "U-CAM" from GBR data.

3. Substrate layer configuration of RL78/G1D Evaluation module

The substrate layer configuration is shown in Figure 1 and Figure 2. This module is composed by four substrate layer. Because the change of substrate layer configuration is an effect on RF characteristics, the substrate layer structure should be the same one if you want to get the same characteristics of RL78/G1D evaluation module.

Figure 1 substrate layer configuration

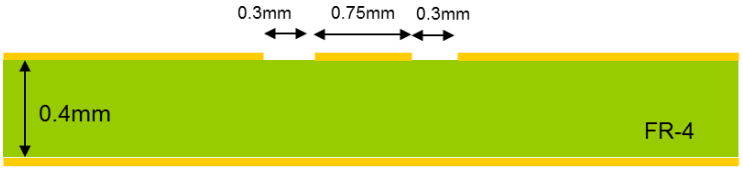

Figure 2 RF unit (50 Ohm impedance line) substrate layer configuration

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2015.3.31	-	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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