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H8SX Family

ΔΣ A/D Converter User's Guide

Introduction

This application note describes the basic principles of ΔΣ A/D converter and the main features of the ΔΣ A/D converter integrated in the H8SX family.

Contents

1. Basic Principles of the ΔΣ A/D Converters

1.1 Difference from Successive-Approximation-Type A/D Converters

1.1.1 Successive-Approximation-Type A/D Converters

Measurement in this method proceeds by comparing the values of the analog voltage to be measured with a variable reference voltage generated by a D/A converter (DAC). The operation can be summarized as follows.

1. The output of the DAC is set to the central value of its output range and compared with the voltage to be measured.
2. According to whether the analog voltage to be measured is less or greater than the central value, the output of the DAC is set to the central value of the lower or upper half of its output range and the voltage are again compared.
3. The above step is performed up to n + 1 times (resolution is assumed to be n bits) to complete the comparison.

This may be compared to measuring an object by using rulers with various lengths and determining which most closely matches the length of the object to be measured.

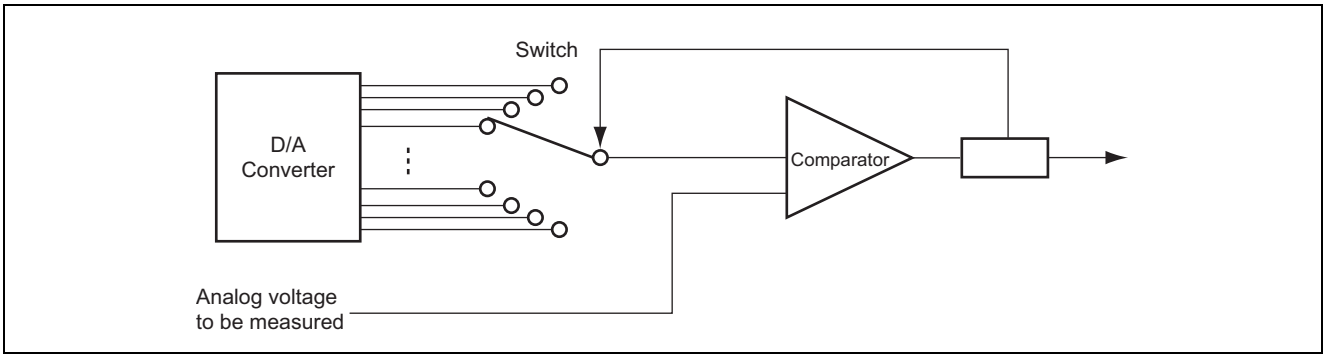


Figure 1.1 A/D Converter of the Successive-Approximation Type

1.1.2 ΔΣ-Type A/D Converter

In an A/D converter of the delta-sigma (ΔΣ) type, the voltage to be measured is sampled and integrated. It is then compared (differentiated) with a constant reference voltage and converted to digital values.

This is similar to measuring the length of an object by counting the number of 1inch units and then multiplying the result by 1 inch. Since this method of analog-to-digital conversion includes both differentiation and integration, it is called the delta-sigma (or sigma-delta) technique.

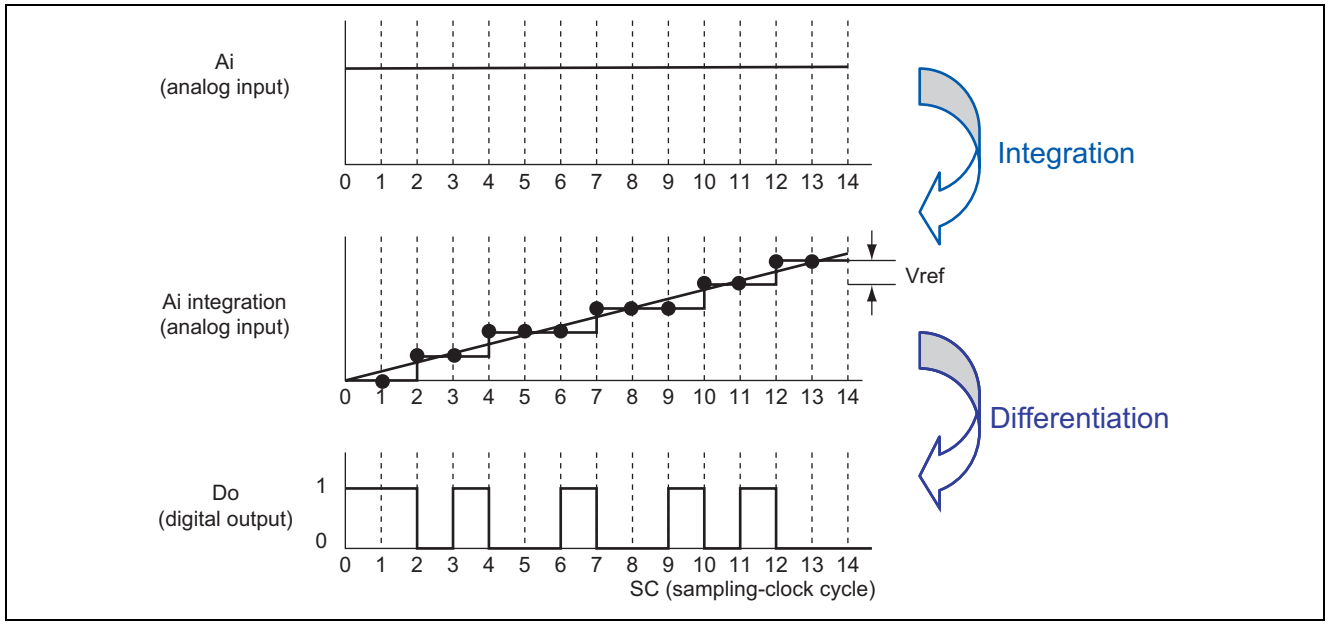


Figure 1.2 Principle of a ΔΣ-Type A/D Converter

1.2 Overview of the ΔΣ A/D Converter

An example of measuring a direct current (DC) voltage is described here for simplicity. When the analog input (Ai) is compared without integration, the measurement is proceeded as follows.

- When SC* = 1, the digital output is 1 since the voltage being compared with the analog input was 0 V and thus 0 < Ai when SC = 0. A voltage Vref is then added to the reference voltage.
- When SC = 2, Vref is compared with Ai. The digital output is 0 since Vref > Ai. The same voltage value is thus used in the next round of measurement.
- When SC = 3, Vref is again compared with Ai. The digital output is 0 since Vref > Ai. The same voltage value is again to be used in the next round of measurement.

However many times the above procedure is repeated, the result will be a digital output made up of a single 1 for the first measurement and successive 0s for subsequent measurements, leaving the value of Ai unchanged.

Note: * SC indicates sampling clocks for ΔΣ A/D Conversion as shown in fig 1.3.

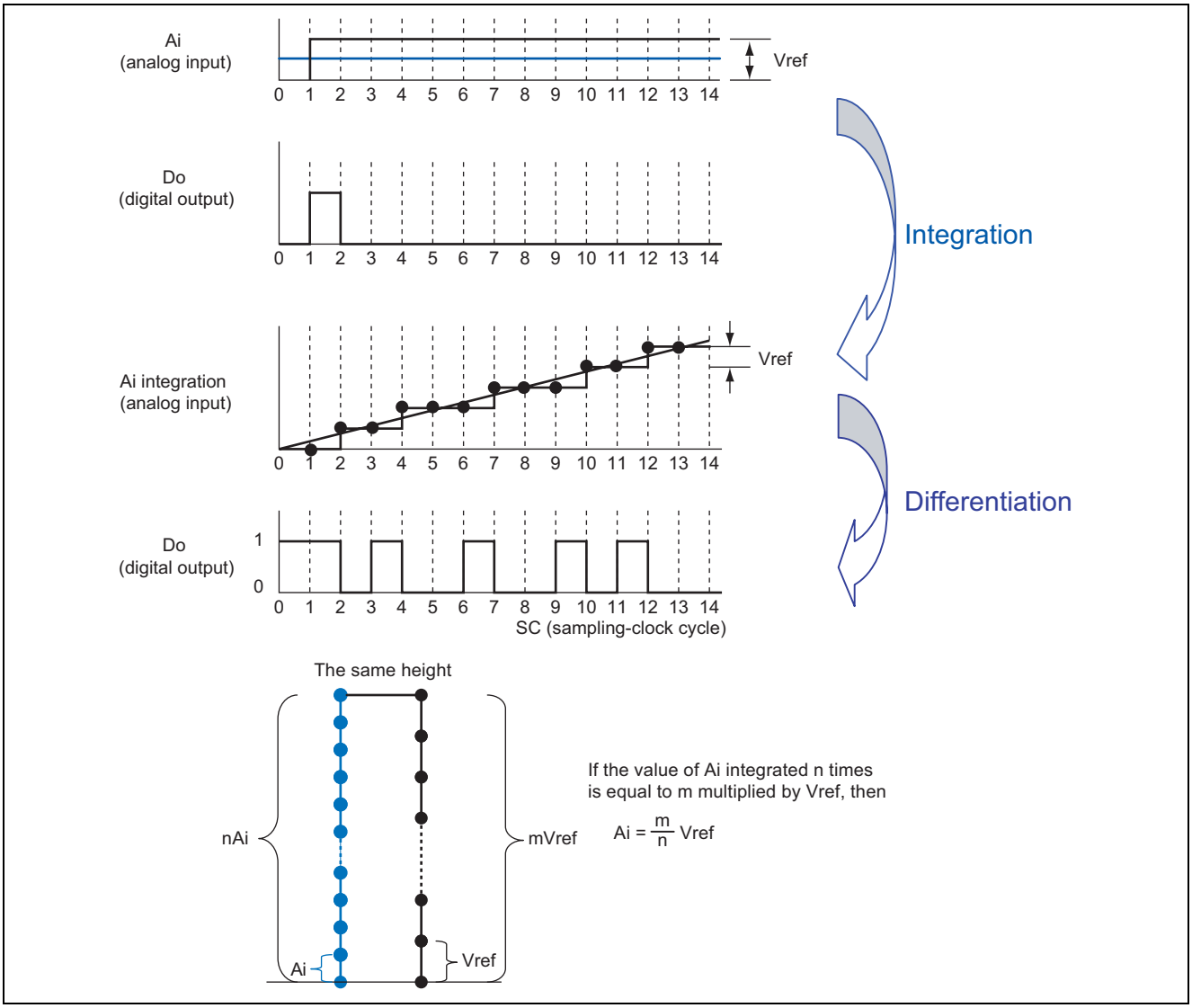


Figure 1.3 Comparison of the Integrated Value and Vref

Now, let us compare the integrated value with Vref as shown in figure 1.3.

- When SC = 1, Ai has only been integrated once and Vref remains 0 V. The digital output is 1 since Vf is less than or equal to Ai and therefore Vref is added to the above 0 V.
- When SC = 2, Ai has been integrated twice. Vf is compared with 2Ai. The digital output is now 0 since Vref > 2Ai. The same voltage (Vref) is used in the next round of measurement.
- When SC = 3, Ai has been integrated three times. Vf is compared with 3Ai. The digital output is 1 since Vref < 3Ai. Vref is again added to the voltage for use in the next measurement (the result being 2Vref).
- When SC = 4, Ai has been integrated four times. Thus 2Vref is compared with 4Ai. In figure 1.3, the digital output is 0 since 2Vref > 4Ai. The same voltage (2Vref) is then used in the next round of measurement.

The above procedure is repeated several times.
Ai is periodically integrated and the resulting slope represents Ai. The integral is compared with Vf to check the relation between the magnitudes of the two values. Addition is repeated and if the result is greater than Vf, Vref is again added to Vf on the next round, and the comparison is repeated. That is, Vf is compared with Ai represented as a slope. Each increase in Ai produced by integration is smaller than Vref.

Ai integration is repeated several times with the result compared to Vf until the result of integration has become greater than Vf. Then another Vref unit is then added to Vf, which is again compared with the integral of Ai. Sampling twice is better than sampling once, and sampling three times is better than sampling twice, and in this way we can see how the precision improves with repeated sampling. In other words, more samples correspond to greater accuracy.

1.3 Advantages of the ΔΣ A/D Converter

1.3.1 Successive-Approximation-Type A/D Converter

- The speed of conversion is high yet devices with lower resolutions are relatively cheap to implement.
- Obtaining N bits of resolution requires the inclusion of 2^n on-chip resistors. Process variation limits the precision of resistors formed on silicon wafer. This approach is thus not suitable for high resolution. That is, due to the limitation imposed on resolution by variation in process accuracy, a new method is necessary for high resolution.

1.3.2 ΔΣ-Type A/D Converter

- Converters of the ΔΣ type have lower conversion speeds than those of the successive-approximation type but higher conversion speeds than those of the double-integrating type.
- This method is suitable for high resolution.

Table 1.1 Comparison of Characteristics of Successive Approximation and ΔΣ Converters

Item	Successive-Approximation Type	ΔΣ Type
Method	Sample and hold	Sampling
Module size	Large	Fitting
Conversion time	Fast (5.33 μs) (H8SX/1622)	Slow (91.5 μs) (H8SX/1622)
High resolution	No	Yes
Frequency band	Without constraint	Depends on digital filter
Noise immunity	Low	High (noise shaping)

2. ΔΣ A/D Converter

2.1 Configuration

A ΔΣ A/D converter consists of one or more integrators, a delta modulator, and a digital filter. The delta modulator modulates the analog input signal to produce a digital signal. The digital filter subsequently eliminates noise to produce the measured data.

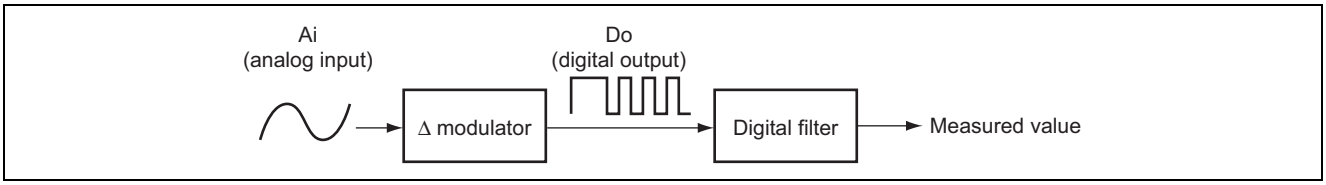


Figure 2.1 Configuration of a ΔΣ A/D Converter

2.2 Δ Modulator

The digital values are produced by comparing an analog input (Ai) with the output of the integrator (Vf). The flow of operations is as follows.

1. The adder determines the difference between the integrator's output (Vf) of the result of D/A-conversion in the previous clock cycle and the analog input signal (Ai).
2. The comparator compares the adder's output with 0 V. According to the result the comparator outputs a digital value of 1 if Ai > Vf or 0 if Ai < Vf.

The above procedure is repeated to convert the analog input into a stream of digital values.

Disadvantages of the Δ modulator necessitate a countermeasure as follows:

[Conversion]

The digital output is a signal obtained by differentiating the analog signal.

[Disadvantages]

1. Direct current voltages cannot be converted.
2. Slope overload* is not supported and precise conversion of high-frequency signal is difficult.

Note: * Slope overload means the situation where the signal rapidly changes by such a large amount (high voltage and rapid change) that the change is faster than the speed of integration.

[Countermeasure]

Integrate the analog input before it is input to the Δ modulator.

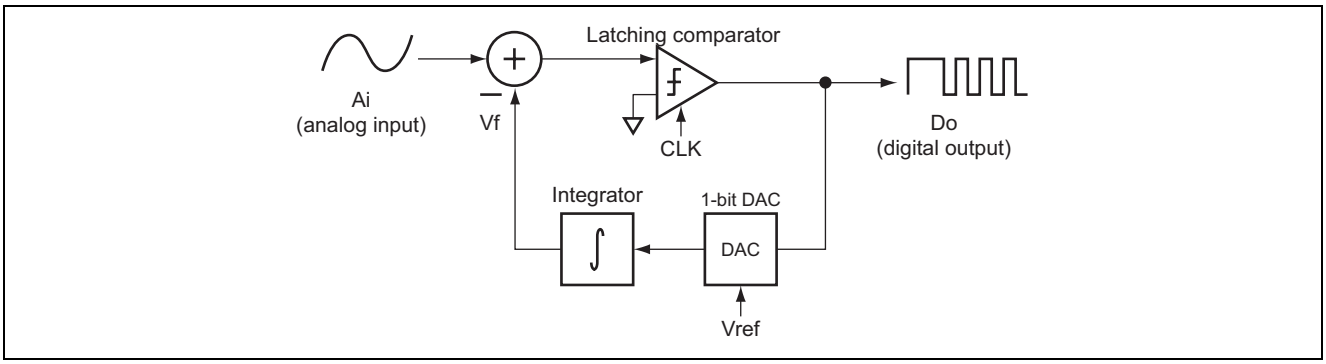


Figure 2.2 Δ Modulator

2.3 ΔΣ Modulator (Integrator + Δ Modulator)

For conversion of direct-current voltages, an integrator is added to the input circuit of the modulator. A Δ modulator at the input of which an integrator has been included is called a ΔΣ modulator.

ΔΣ modulator: Integrator + Δ modulator

Since the two integrators can be treated as a single integrator according to the approach shown below, the integrator is placed after the adder.

$$\int f1(x)dx + \int f2(x)dx$$
$$= \int (f1(x) + f2(x)) dx$$
$$= \int f(x)dx$$

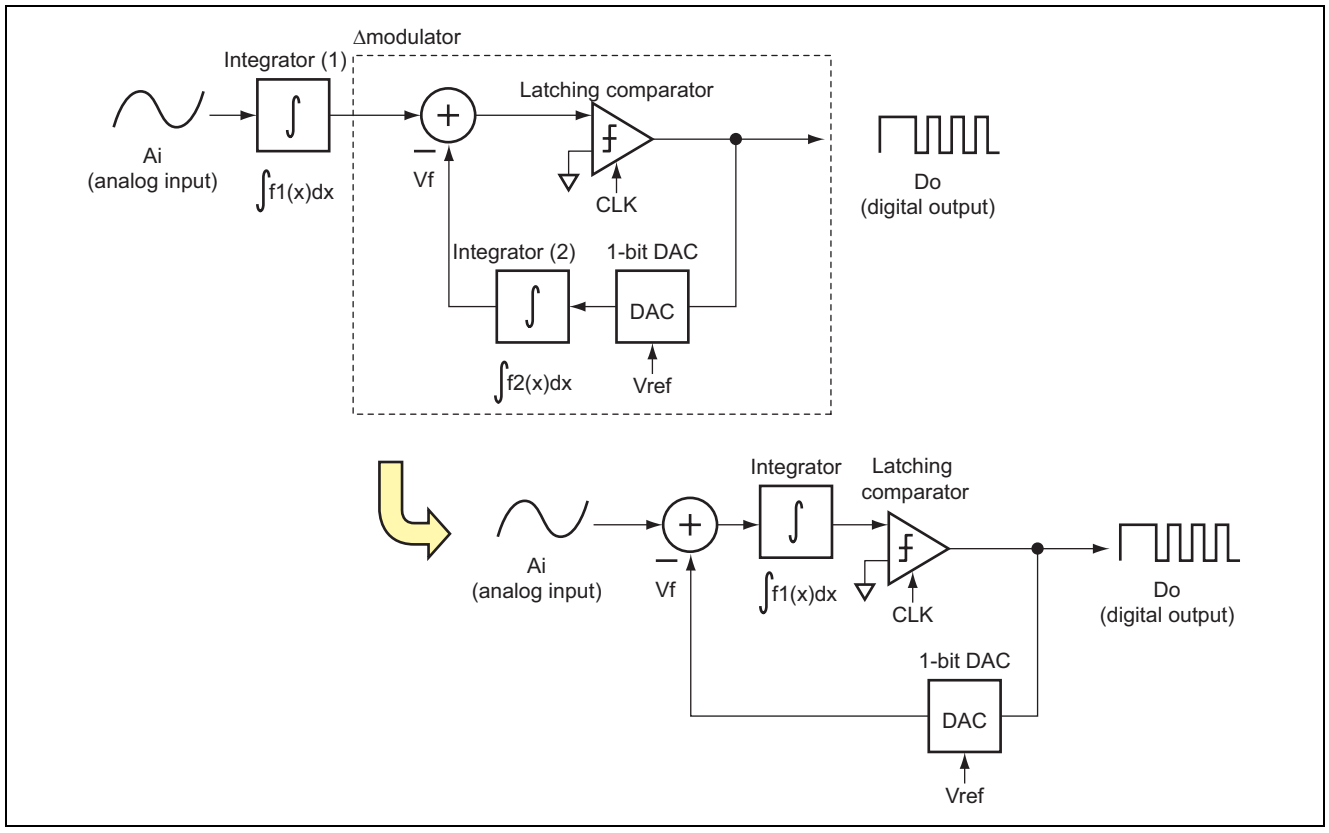


Figure 2.3 Input-Stage Integrator + Δ Modulator

2.4 First- and Second-Order ΔΣ Modulators

The first-order ΔΣ modulator has a single integrator while the second-order ΔΣ modulator has two. The second-order ΔΣ modulator is superior to the first-order ΔΣ modulator in terms of noise-shaping effect.

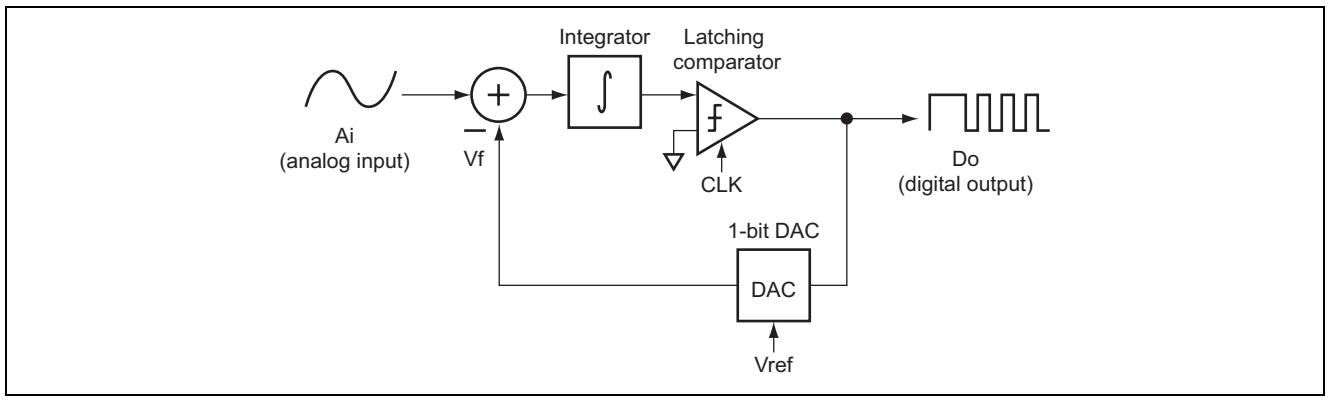


Figure 2.4 First-Order ΔΣ Modulator

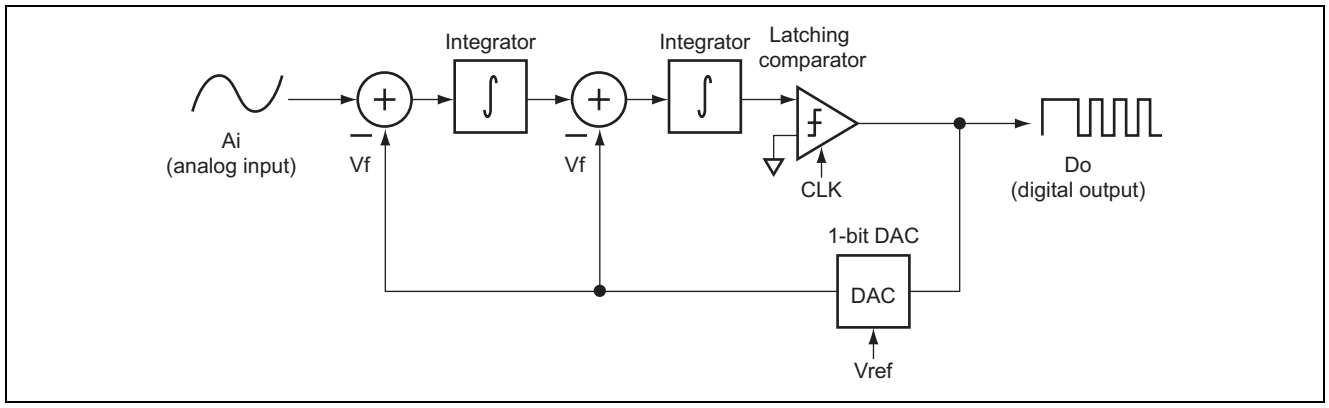


Figure 2.5 Second-Order ΔΣ Modulator

2.5 Second-Order ΔΣ A/D Converter

The operation of the second-order ΔΣ A/D converter is summarized as follows:

1. The analog input is integrated twice.
2. Differentiation is performed twice in two loops (although the principles of operation would have differentiation twice, the result of expanding the formula is their unification as a single comparator in the circuit).
3. Since differentiation and integration are each other's reverse functions, differentiation and integration ultimately restore the original. In addition, we have now obtained a digital signal.
4. Digital filtering removes the noise introduced by sampling.

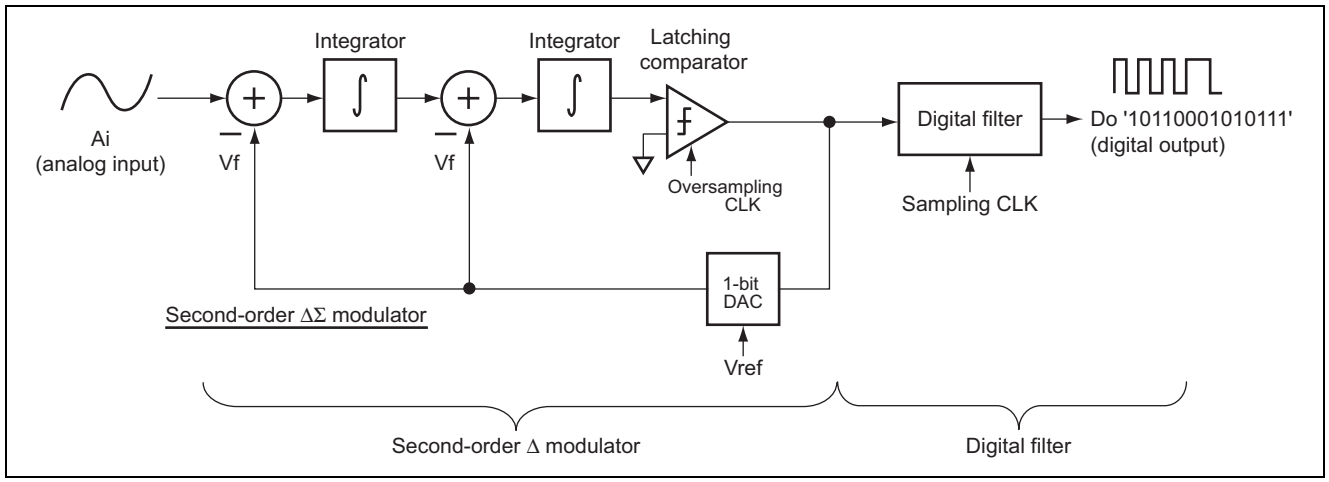


Figure 2.6 Second-Order ΔΣ A/D Converter

3. Filter

3.1 Digital Filter

The digital output of the ΔΣ modulator contains two types of noise from sampling: quantization error (figure 3.2) and aliasing noise (figure 3.3). The characteristics of a digital filter are handled by impulse responses. That is, by the calculating digital values in real time, we can perform interpolation and decimation to remove noise components. Decimation is the operation of converting a higher sampling frequency to a lower sampling frequency.

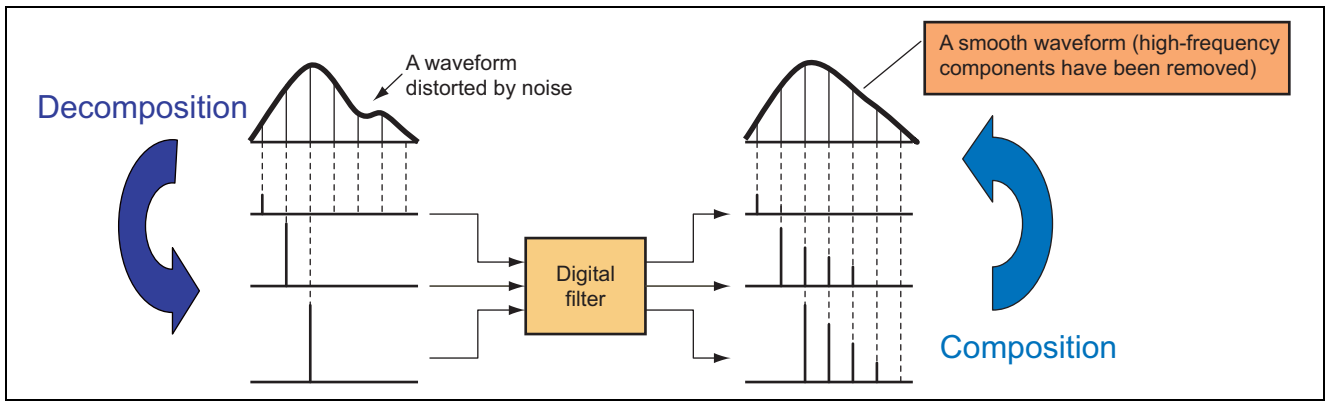


Figure 3.1 Digital Filter

3.2 Quantization Error

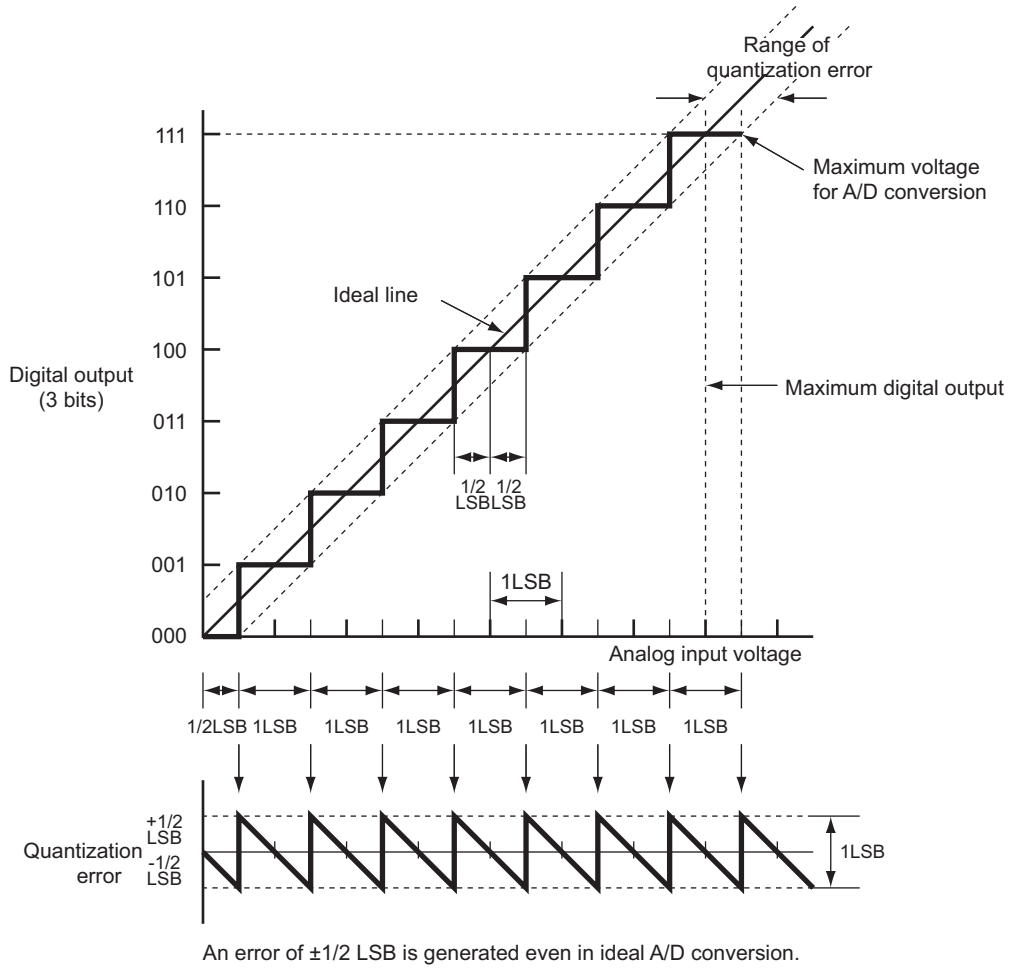


Figure 3.2 Quantization Error

3.3 Aliasing Noise

When analog signals f1 and f2 (f1 multiplied by 7) below are sampled at eight times the frequency of f1, the sampling points in analog signals of f1 and f2 become identical. The sampling points thus have a frequency component of f2, and f2 is called an aliasing noise of f1.

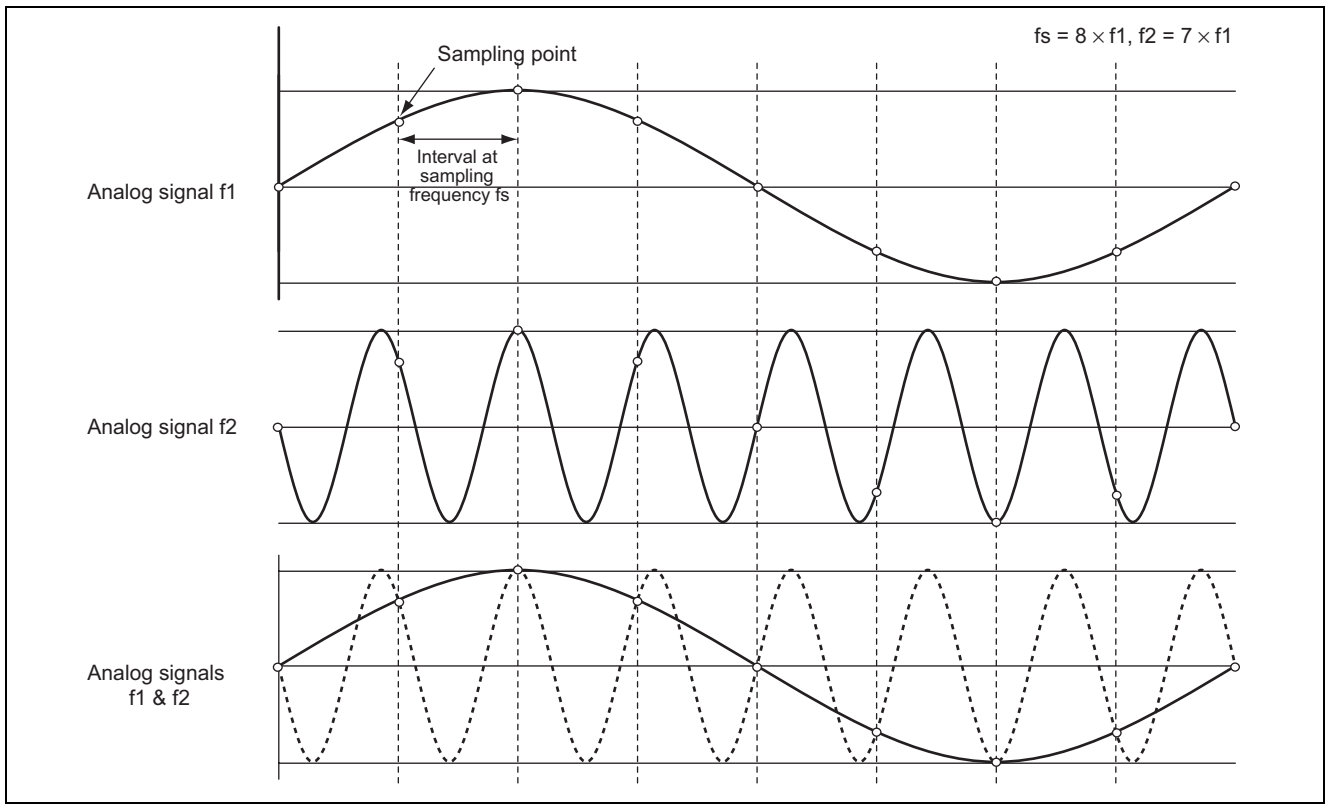


Figure 3.3 Aliasing Noise

3.4 Impulse Response

The impulse response is one way to analyze a continuous analog signal. The impulse response is a response generated when a unit impulse is input to a system.

1. The continuous analog signal is decomposed into impulses, since it is difficult to analyze the signal without modification.
2. Given a transfer function h(t), the waveform in response to a single impulse is obtained by **y(t) = h(t) * x(t)**.
3. By definition, the principle of superposition is valid in a linear system. Consequently, the superposition of the waveforms in response to the individual pulses is ultimately the waveform in response to the overall input signal.

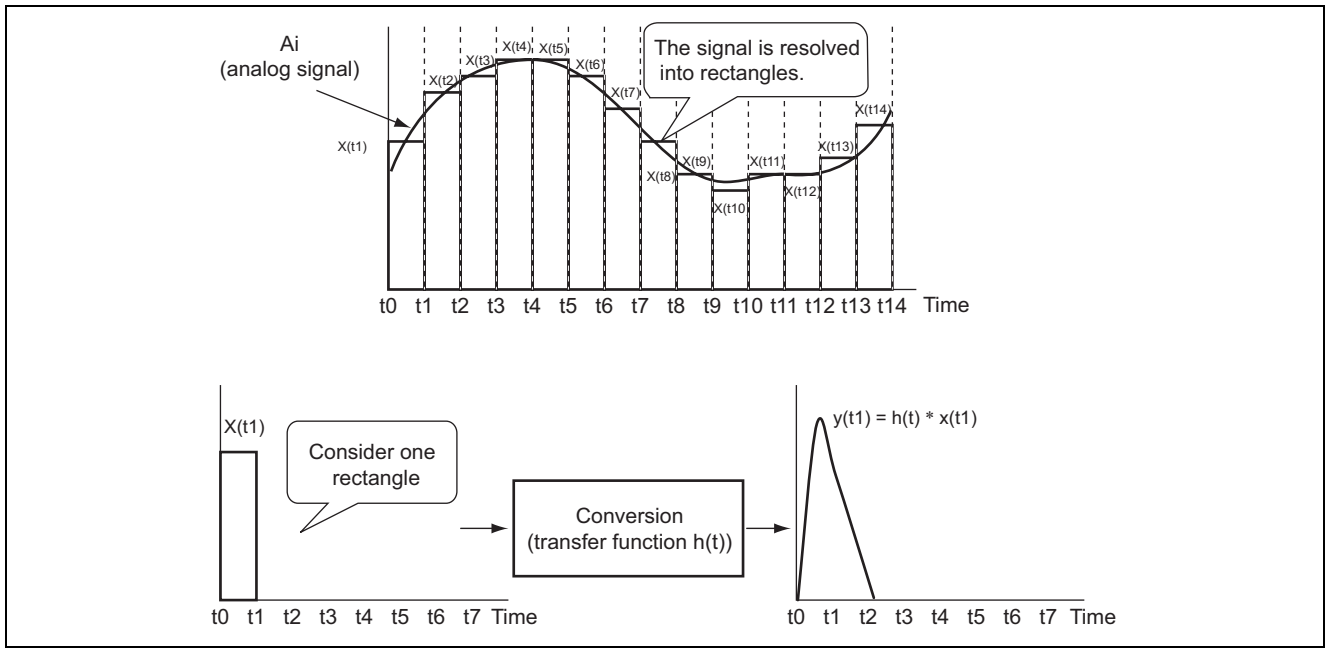


Figure 3.4 Impulse Responses

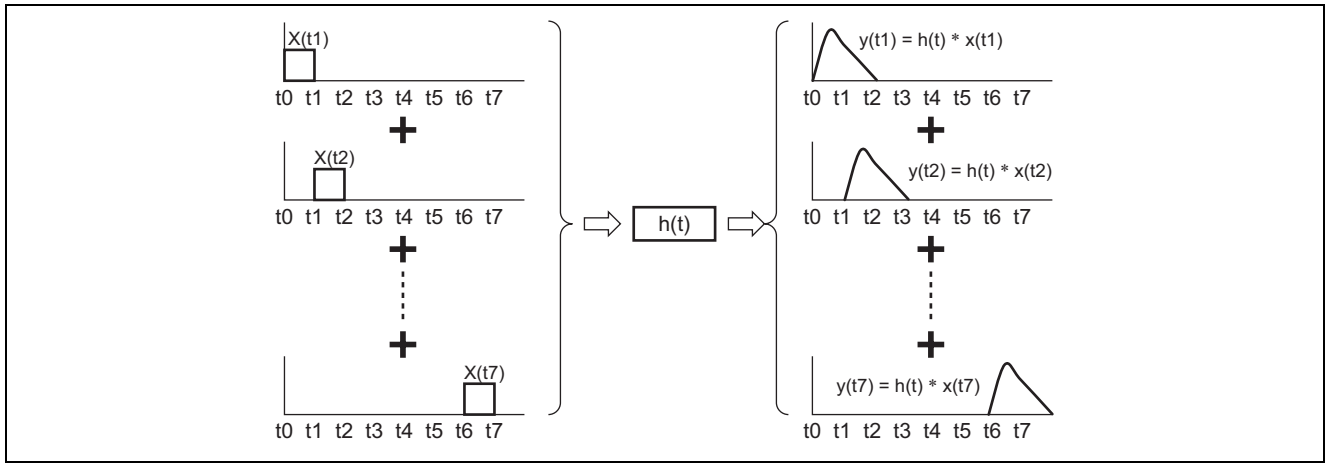


Figure 3.5 Definition of Superposition

3.5 Noise Reduction by Digital Filtering

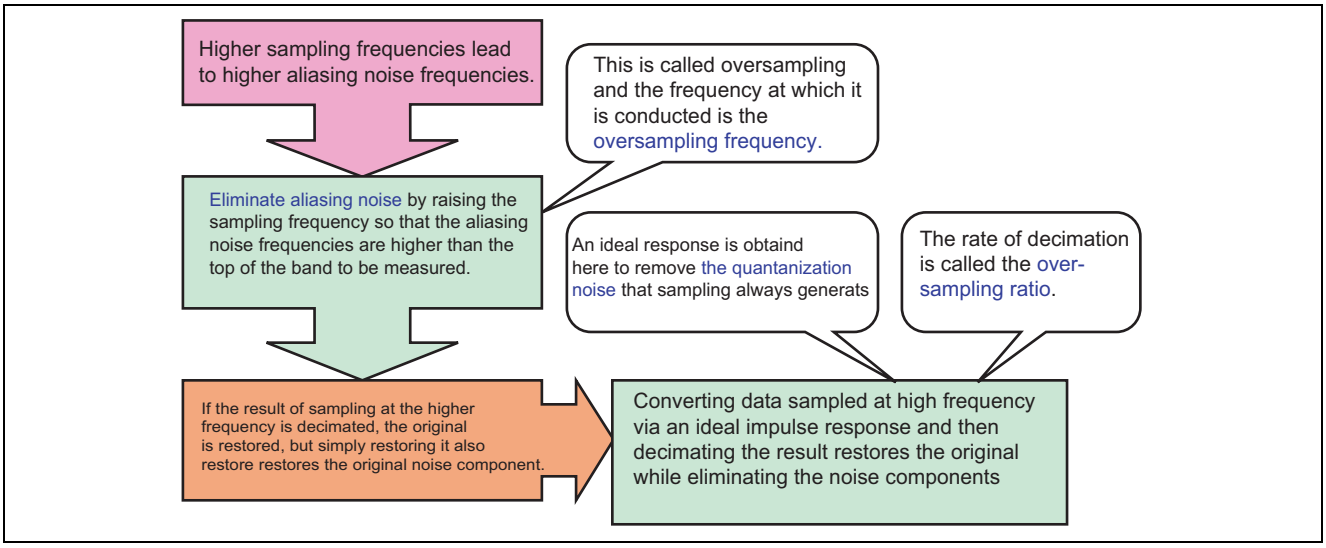


Figure 3.6 Procedure for Noise Reduction by Digital Filtering

3.6 Methods of Digital Filtering

The role of the digital filter is to convert sampled data into a stream of ideal impulse responses. To be specific the conversion is achieved by multiplying the input impulses by a transfer function. There are two methods, which differ according to how multiplication by the transfer function is achieved.

1. IIR (Infinite Impulse Response) Filter
   This is a method that combines an adder and a delay element to form a feedback loop. This kind of filter is referred to as an infinite impulse response filter because the output waveform in response to an impulse is dampened but continues indefinitely.

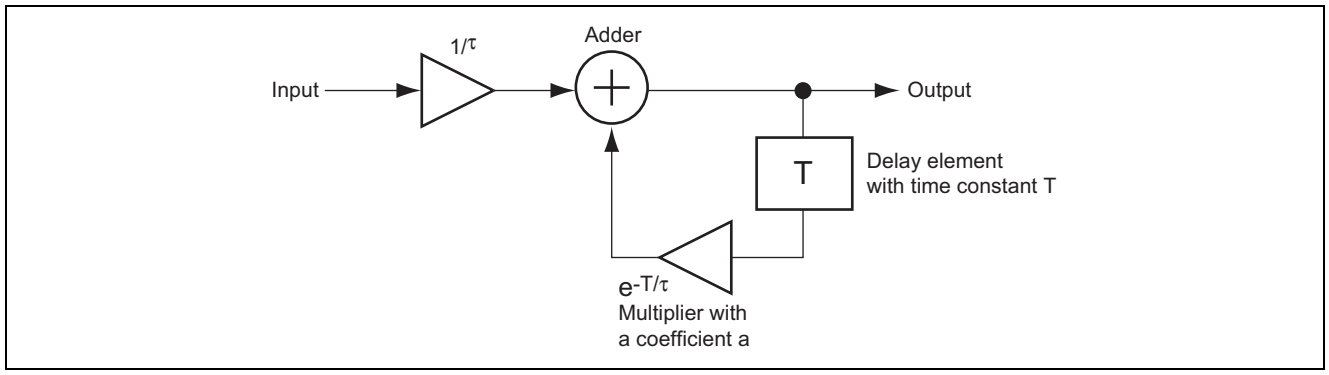


Figure 3.7 IIR (Infinite Impulse Response) Filter

2. FIR (Finite Impulse Response) Filter
   An FIR filter consists of shift registers, multipliers which multiply output of the registers by data, and an adder. The data here are coefficients calculated from impulse response of an ideal filter.

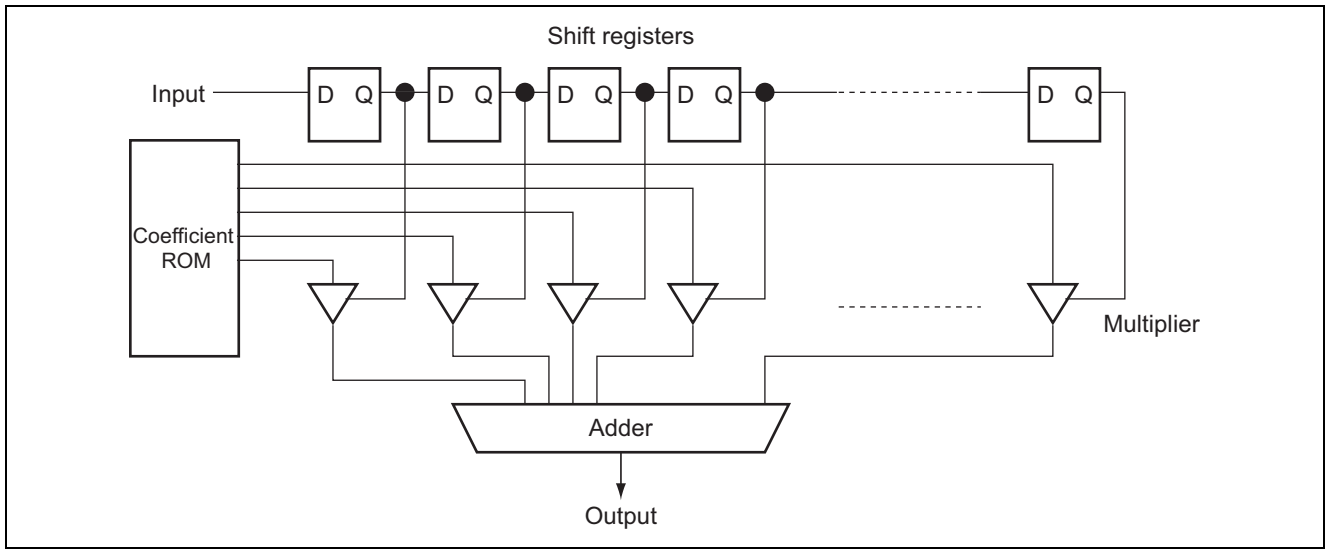


Figure 3.8 FIR (Finite Impulse Response) Filter

4. Errors and Methods of Correction

4.1 Errors in A/D Converters

4.1.1 Successive Approximation A/D Converter

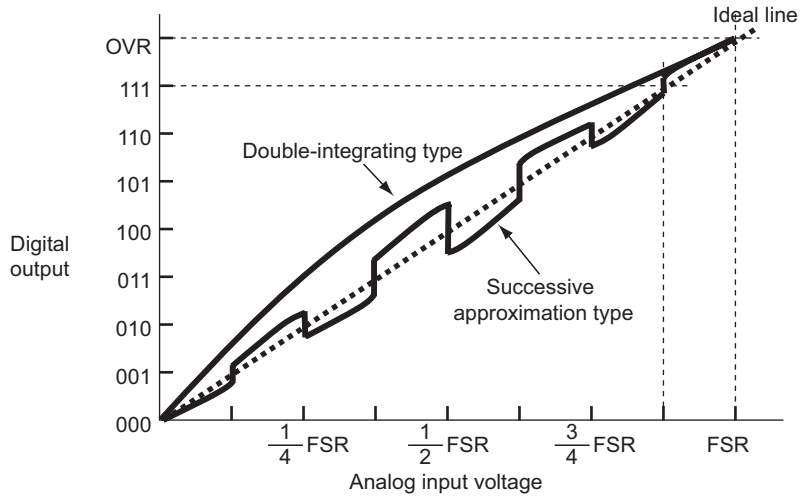
Major errors are readily generated in the output characteristics at point where output values change, such as 1/2 FSR and 1/4 FSR. Differential nonlinearity is a major portion of the error and reaches its maximum where all bits change at 1/2 FSR.

4.1.2 Double-Integrating A/D Converter

The output characteristic has no sharp changes, integral nonlinearity produces a large error, and the curve produced is smooth.

4.1.3 ΔΣ-Type A/D Converter

Since offset (OS) error and full-scale (FS) error are produced, the range of measurement becomes OS to FS. Once offset and full-scale correction have been applied, an output characteristic with superior linearity is obtained.



Note : FSR : Full-scale range (maximum input range)

Figure 4.1 Errors in Successive Approximation and Double-Integrating Type Converters

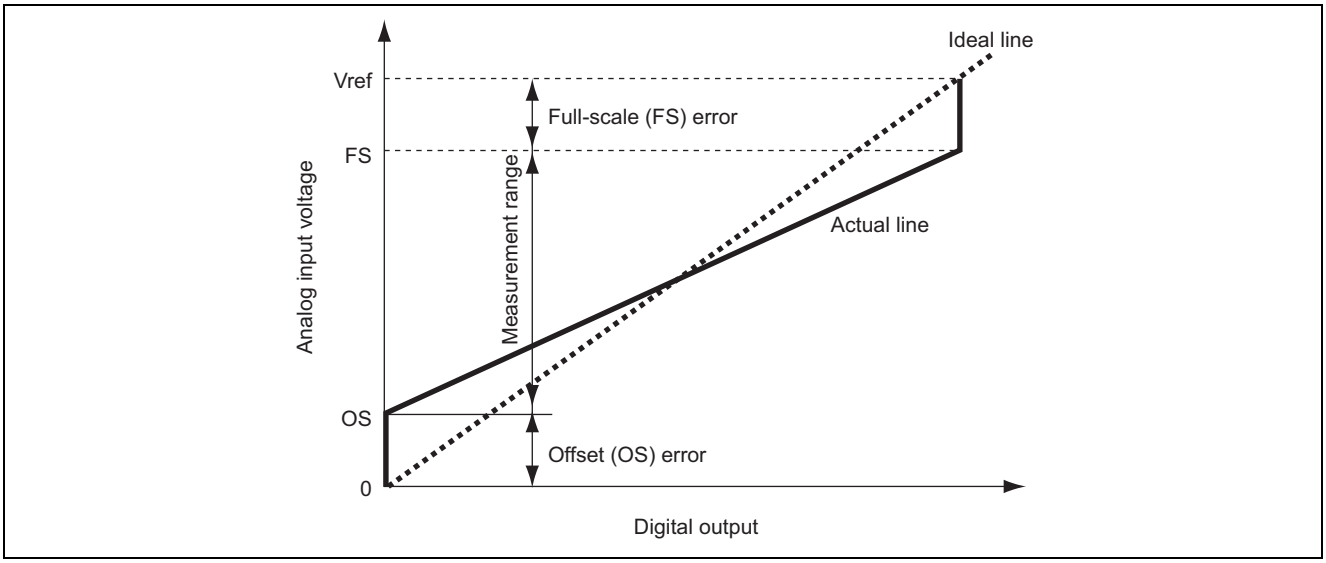


Figure 4.2 Errors in ΔΣ A/D Converters

4.1.4 Differential Nonlinearity Error

The differential nonlinearity error, as shown in figure 4.3, is the differences between the ideal value corresponding to one LSB and the actual analog step sizes. When the step size is exactly equivalent to the ideal value for one LSB, the differential nonlinearity error is zero. When the differential nonlinearity exceeds one LSB, the proportionality of output to input is further reduced. Furthermore, code loss may occur. That is, the converter becomes incapable of producing one or more of the 2n codes.

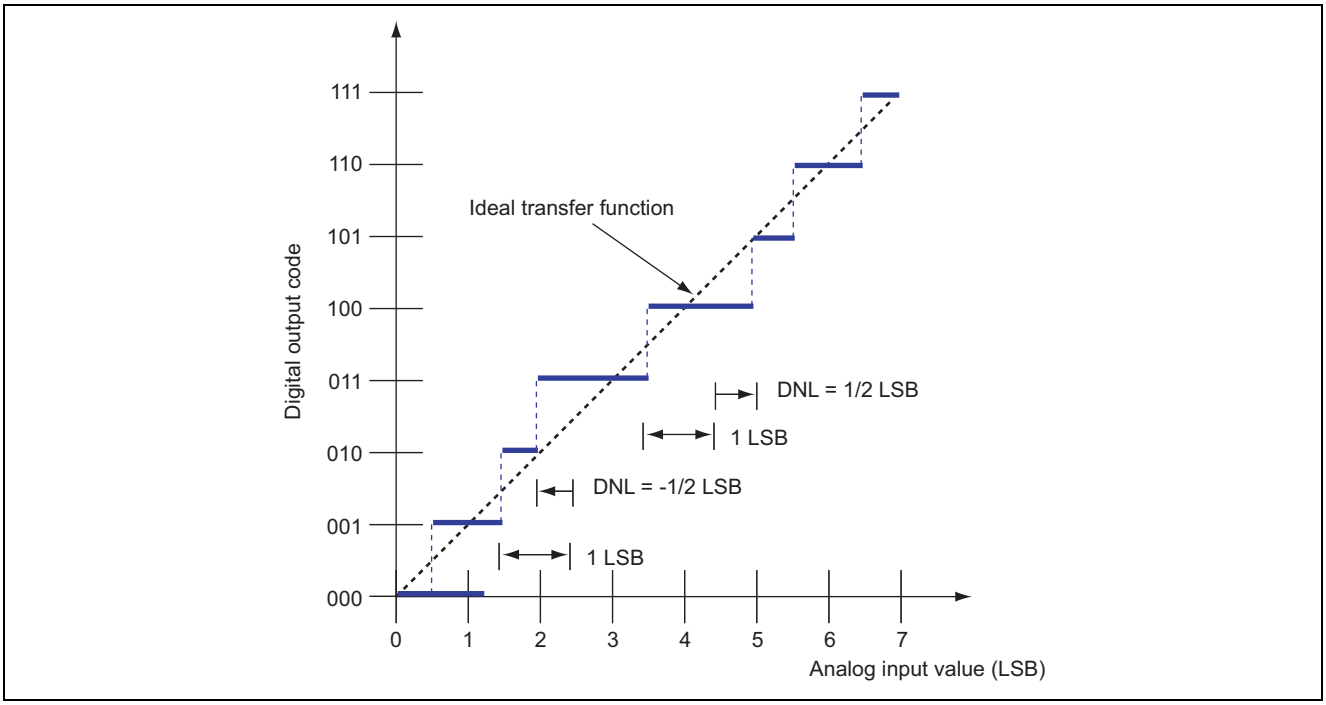


Figure 4.3 Differential Nonlinearity Error

4.1.5 Integral Nonlinearity Error

The deviation of the actual result of conversion from the value given by the ideal line is referred to as integral nonlinearity (see figure 4.4). This deviation is measured by the step.

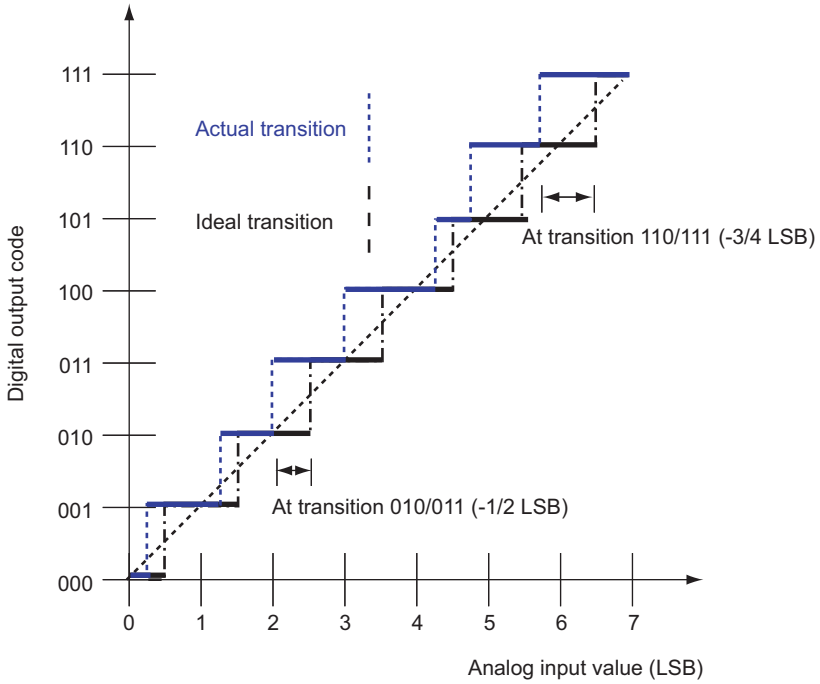


Figure 4.4 Integral Nonlinearity Error

4.2 Correction of Offset and Full-Scale Errors

4.2.1 Approach to Correction

Figure 4.5 shows the relation between digital values (ADDR values) and analog values (to be measured) of the ΔΣ A/D converter.

The response of an ideal A/D converter, as shown as a dashed line in figure 5.5, is linear from the origin to the full-scale voltage. Since offset (OS) error and full-scale (FS) error are produced, the actual relation is portrayed by the solid line. Consequently, offset/full-scale error correction should be applied to derive more accurate values from the measured digital values.

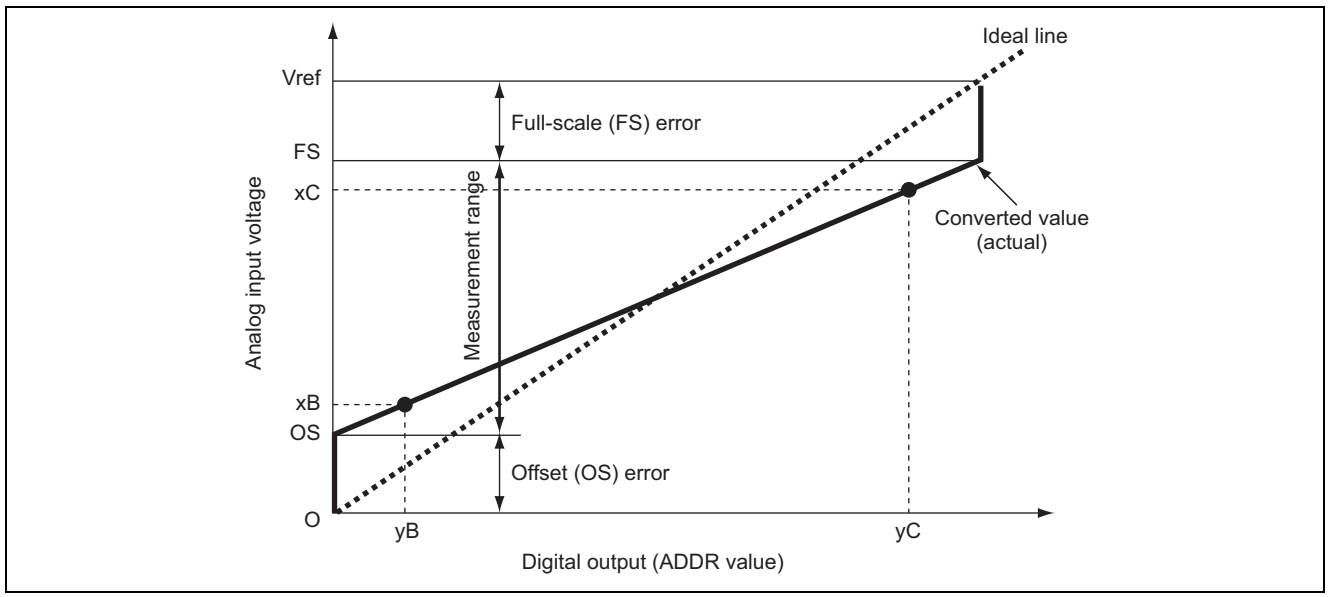


Figure 4.5 Relation of Analog Value (to be Measured) and Digital Value (ADDR Value)

The following equations describe the relations between x and y in the solid line of Fig 4.5.

$$lsb = (xC - xB) / (yC - yB) \quad \cdots(1)$$
$$x = (xC - xB) / (yC - yB) * y + OS \quad \cdots(2)$$
$$OS = xB - (xC - xB) / (yC - yB) * yB \quad \cdots(3)$$

and from (1), (2), and (3), we have:

$$x = lsb * y + xB - lsb * yB = lsb * (y - yB) + xB$$

4.2.2 Correcting Offset and Full-Scale Errors

The procedure for offset/full-scale error correction is as follows.

1. Measure x and y values at the four points A, B, C, and D shown in figure 4.5.
2. Calculate the slope (lsb) by determining x and y values at points B and C.
3. Calculate the target value from the digital value (the value in ADDR).

$$\text{Target value} = \text{Slope (lsb)} * (\text{ADDR value} - yB) + xB$$

5. Functional Description of the H8SX Family ΔΣ A/D

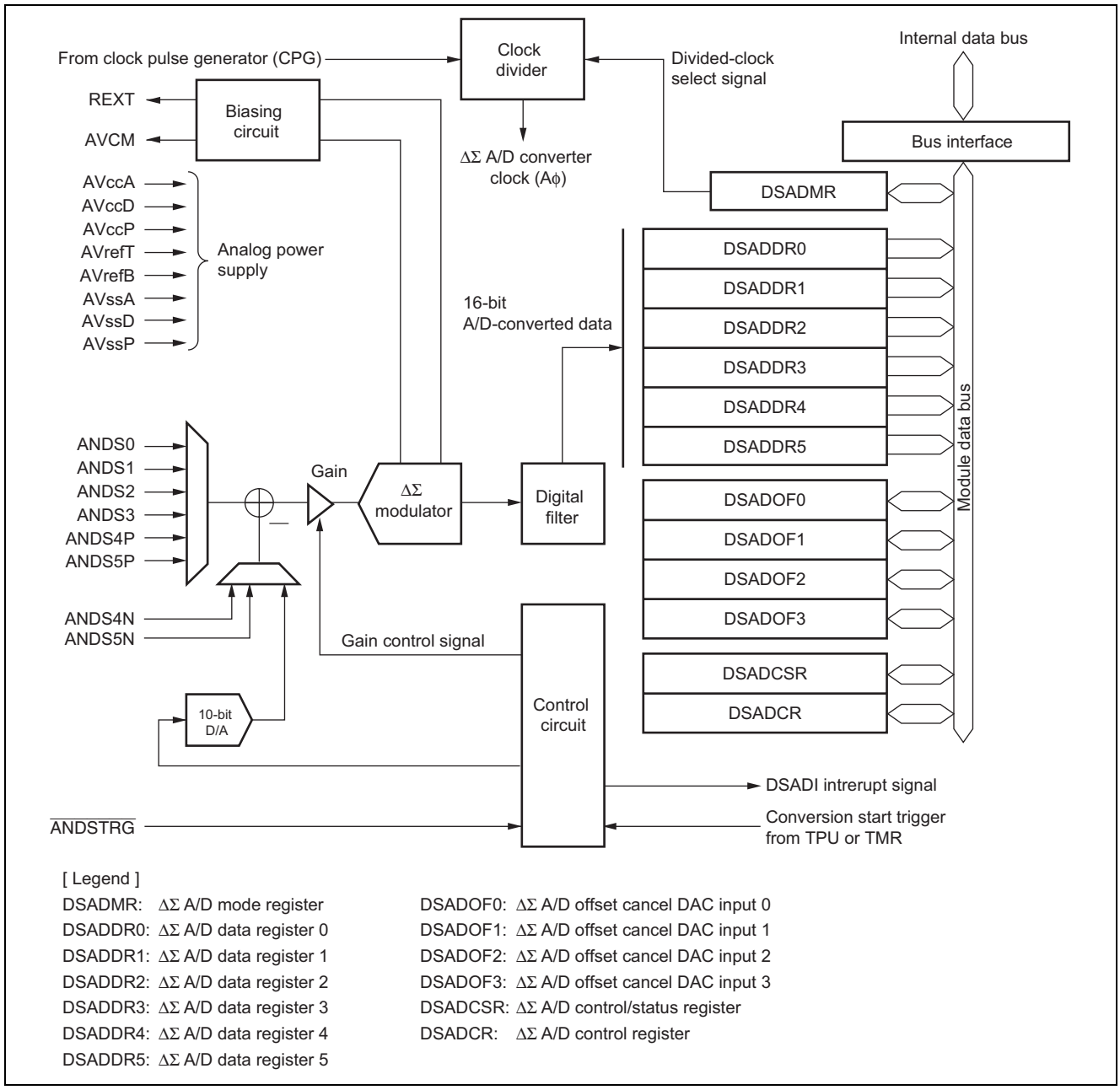
5.1 Basic Operations

The ΔΣ A/D converter of the H8SX Family uses a ΔΣ modulator to convert analog input voltages within the range specified by the voltages on the AVrefT and AVrefB pins into digital values with a resolution of 16-bits. The ΔΣ A/D converter is composed of an analog block with a ΔΣ modulator as the main component, and a digital filter, and a control blocks.

In the analog block, the DS modulator amplifies the input signals (eight-fold when the GAIN1 and GAIN0 bits in DSADCR is set to B'11) and converts them. During this process, the ΔΣ offsets of the signals input from the single-ended input signal pins (ANDS0, ANDS1, ANDS2, ANDS3) are cancelled by setting offset values in the DSADOF0 to DSADOF3 registers. In addition differential input are supported on pins (ANDS4P, ANDS4N and ANDS5P, ANDS5N). The voltage of a selected analog input signal is sampled at the Aϕ/8 clock frequency (oversampling frequency) and converted to a series of digital values by the second-order ΔΣ modulator. The result of conversion is passed through a decimation filter (digital filter) and stored in the corresponding ΔΣ A/D data register as a 16-bit signed binary number (two's complement).

The ΔΣ A/D converter operates in either single mode or scan mode. Multiple channels are specified by selecting multiple A/D conversion channel-selection bits.

Figure 5.1 shows a block diagram of the ΔΣ A/D converter and table 5.1 shows its pin configuration.



[Legend]

DSADMR: ΔΣ A/D mode register
DSADDR0: ΔΣ A/D data register 0
DSADDR1: ΔΣ A/D data register 1
DSADDR2: ΔΣ A/D data register 2
DSADDR3: ΔΣ A/D data register 3
DSADDR4: ΔΣ A/D data register 4
DSADDR5: ΔΣ A/D data register 5
DSADOF0: ΔΣ A/D offset cancel DAC input 0
DSADOF1: ΔΣ A/D offset cancel DAC input 1
DSADOF2: ΔΣ A/D offset cancel DAC input 2
DSADOF3: ΔΣ A/D offset cancel DAC input 3
DSADCSR: ΔΣ A/D control/status register
DSADCR: ΔΣ A/D control register

Figure 5.1 Block Diagram of the ΔΣ A/D Converter

Table 5.1 Pin Configuration

Pin Name	Abbreviation	I/O	Function
Analog input pin 0	ANDS0	Input	Analog input pins: Single-ended input
Analog input pin 1	ANDS1	Input	
Analog input pin 2	ANDS2	Input	
Analog input pin 3	ANDS3	Input	
Analog input pin 4-P	ANDS4P	Input	Analog input pins: Differential input
Analog input pin 4-N	ANDS4N	Input	
Analog input pin 5-P	ANDS5P	Input	Analog input pins: Differential input
Analog input pin 5-N	ANDS5N	Input	
External trigger input pin for ΔΣ A/D converter	$\overline{\text{ANDSTRG}}$	Input	External trigger input pin for starting ΔΣ A/D conversion
Analog power supply pin	AVccA*[1]	Input	Power supply pin for the analog section of the ΔΣ A/D converter
Analog power supply pin	AVccD*[1]	Input	Power supply pin for the control circuit of the ΔΣ A/D converter
Analog power supply pin	AVccP*[1]	Input	Power supply pin for the input pin control circuit of the ΔΣ A/D converter
Analog ground pin	AVssA	Input	Ground pin for the analog section of the ΔΣ A/D converter
Analog ground pin	AVssD	Input	Ground pin for the control circuit of the ΔΣ A/D converter
Analog ground pin	AVssP	Input	Ground pin for the input pin control circuit of the ΔΣ A/D converter
ΔΣ reference voltage (high)	AVrefT*[2]	Input	Stabilizing capacitors connected (between $AV_{ref}B$ and $AV_{ref}T$; 10 µF + 0.1 µF)
ΔΣ reference voltage (low)	AVrefB*[2]	Input	
Reference voltage pin	AVCM	Output	Stabilizing capacitor connected (0.1µF between AVCM and $AV_{SS}A$)
Reference current pin	REXT	Output	External resistor connected between REXT and $AV_{SS}A$. (51 kΩ with ±1% tolerance)

Notes: 1. Always ensure that AVccA = AVccD = AvccP holds.
2. Furthermore ensure that AVccA = AVrefT, AVrefT > AVrefB, AVrefB = AVssA hold.

5.2 Offset Cancellation Function

For single-ended input signal, the DC component in the analog signal can be cancelled (subtracted) by setting the offset canceling value in the internal registers of DSADOF0 to DSADOF3. Be aware that this function does not cancel offset error in A/D conversion or offset in the amplifier.

The offset-canceling analog level corresponding to the register setting can be illustrated as in the figure below. The possible offset-canceling analog level varies depending on the GAIN setting. Table 5.2 shows the corresponding relation between GAIN and DSADOFn settings.

DOF = DSADOF/210 × (AVrefT – AVrefB)

DOF : Offset canceling analog level (V)
DSADOF : Register value set in DSADOFn[9:0] corresponding to the channel (DSADOF = 0 to 1023)
AvrefT : ΔΣ voltage reference high (V) (AvrefT = AVccA)
AvrefB : ΔΣ voltage reference low (V) (AvrefB = AvssA = 0V)

Table 5.2 Setting Values of Gain and DSADOFn

	DSADOFn (n = 0 to 3)	
GAIN1, GAIN0	**Settable Range**	**Remarks**
B'00	H'0200	Always set to H'0200.
B'01	H'0200	Always set to H'0200.
B'10	H'0000 to H'03FE	Bit 0 must be clear to 0
B'11	H'0000 to H'03FF	—

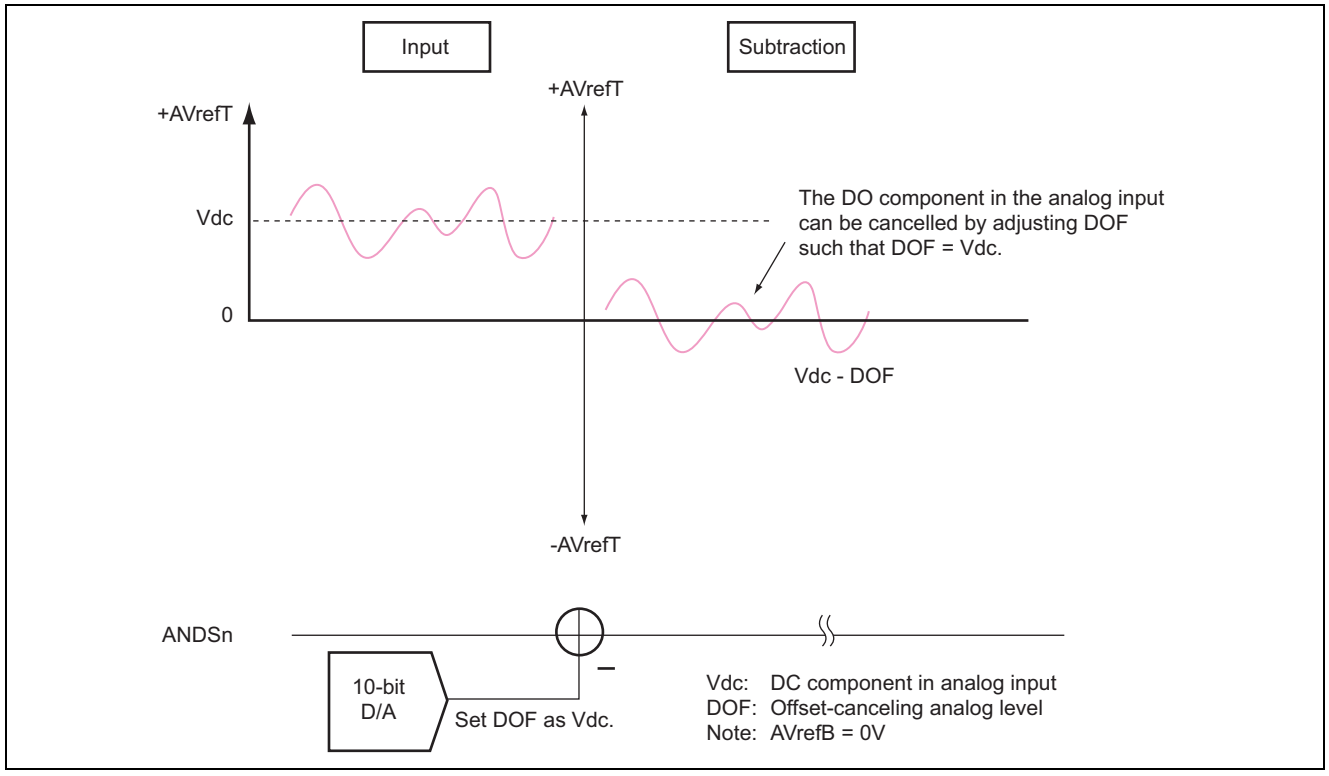


Figure 5.2 Offset Cancellation Function

5.3 Gain Function

An analog signal is amplified and input to the ΔΣA/D converter by setting the gain level (8-, 4-, 2-, or 1-fold) in the GAIN1 and GAIN0 bits of DSADCR internal register.

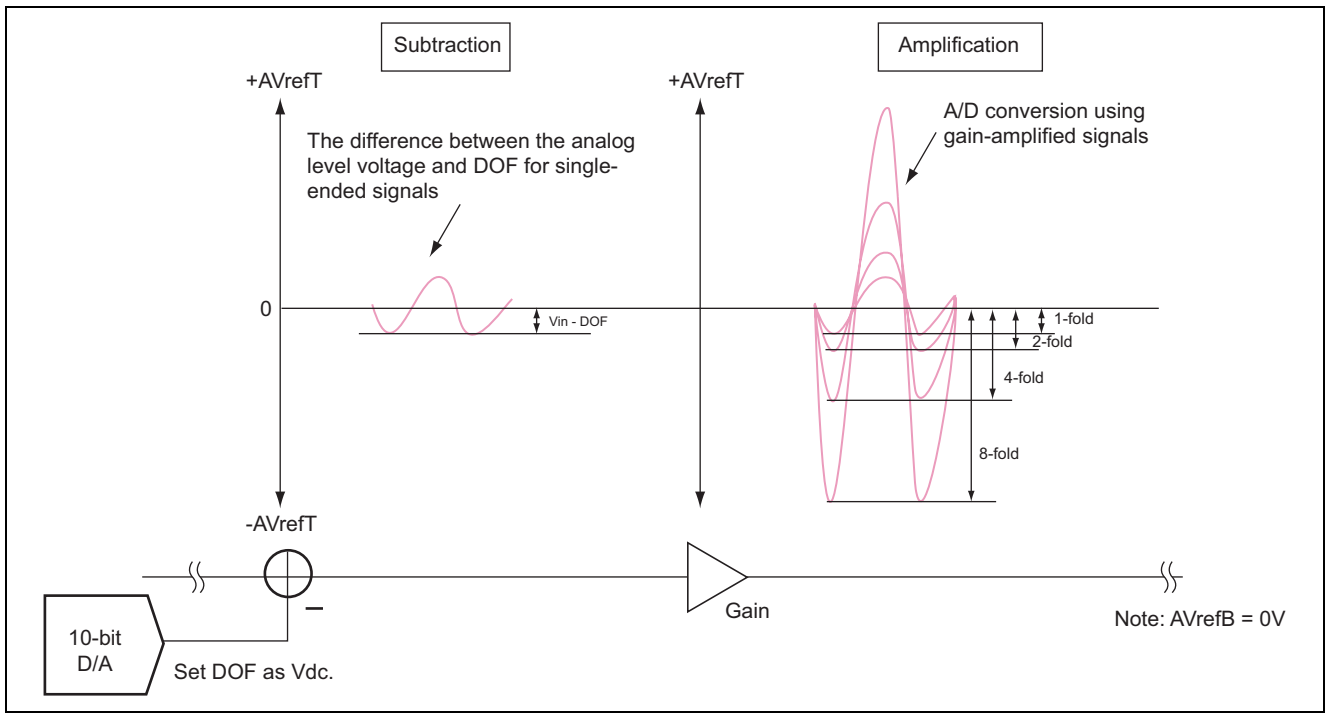


Figure 5.3 GAIN Function (For Single-Ended Inputs)

5.4 Single-Ended Input

For single-ended input, one analog level Vin (pin name: ANDS0, ANDS1, ANDS2, or ANDS3) and the offset-canceling analog level DOF that is set in the DSADOFn corresponding to an analog input channel are used. The ΔΣADC performs the subtraction "Vin – DOF" and uses the voltage difference between the analog level and DOF as the input signal.

Then, the input signal is amplified according to the gain setting (8- to 1-fold) to be input to the ΔΣ modulator.

The ΔΣ modulator converts the analog voltage within the range determined by the AVrefT and AVrefB pins into a digital value with 16-bit resolution. The A/D conversion result should be a positive value (H'0000 to H'7FFF) if Vin – DOF ≥ 0 (V), and be a negative value (H'FFFF to H'8000) if Vin – DOF < 0 (V).

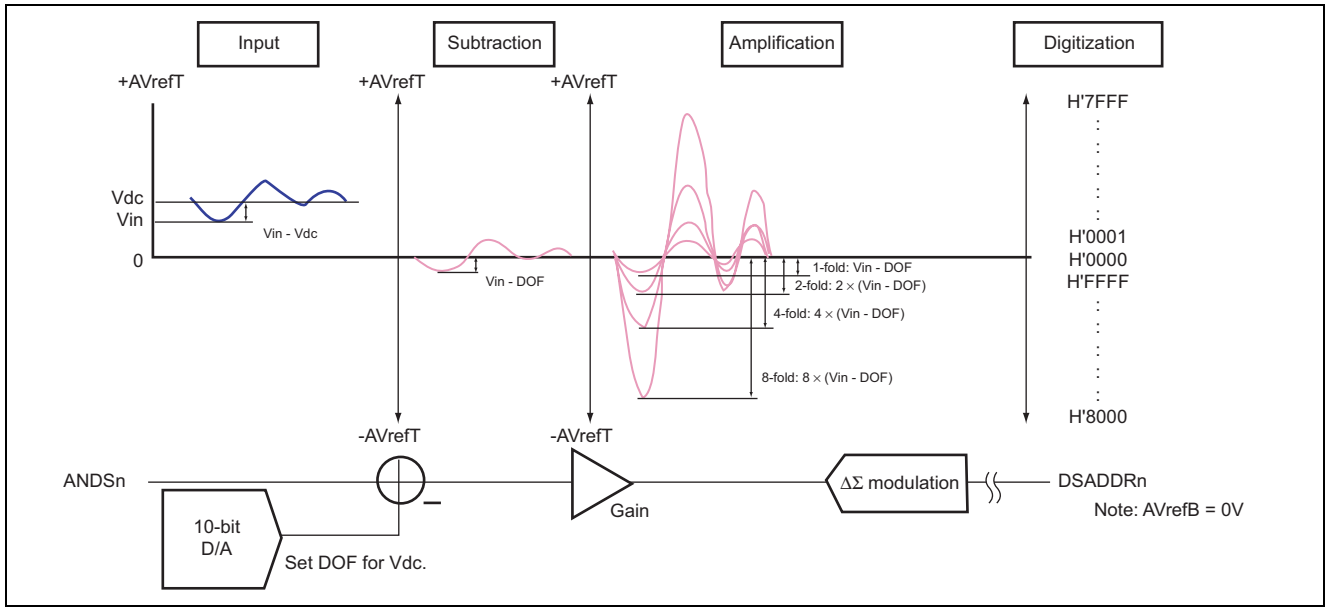


Figure 5.4 Single-Ended Input

5.5 Differential Input

For differential input, two analog levels VinP – VinN (pin name: ANDS4P–ANDS4N, ANDS5P–ANDS5N) are used.

The ΔΣADC performs the subtraction "VinP – VinN" and uses the voltage difference between the ANDSnP and ANDSnN analog levels as the input signal.

Then, the input signal is amplified according to the gain setting (8- to 1-fold) to be input to the ΔΣ modulator.

The ΔΣ modulator converts the analog voltage range determined by the AVrefT and AVrefB pins into a digital value with 16-bit resolution. The A/D conversion result should be a positive value (H'0000 to H'7FFF) if VinP – VinN ≥ 0 (V), and be a negative value (H'FFFF to H'8000) if VinP – VinN < 0 (V).

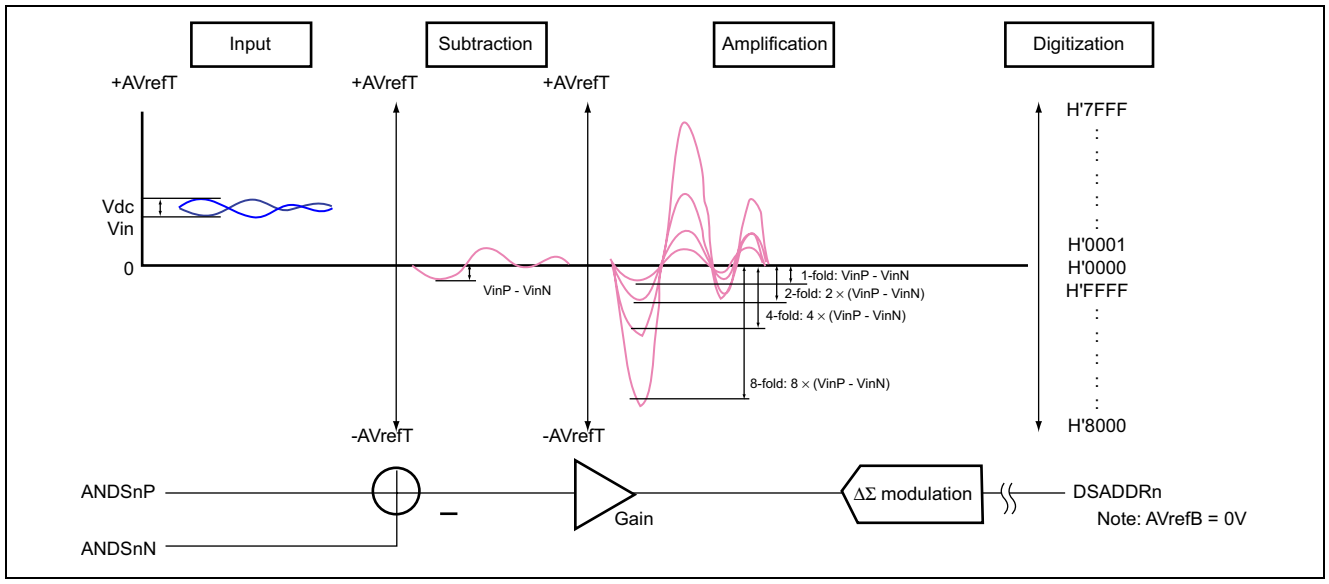


Figure 5.5 Differential Input

5.6 Operating Modes

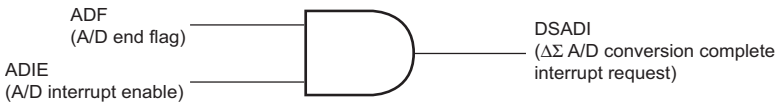
5.6.1 Single Mode (Single Channel)

The operation in single mode is described below. Figure 5.6 shows an example of ΔΣ A/D converter operation in single mode (single-value channel: channel 1 selected).

[Operating Conditions]

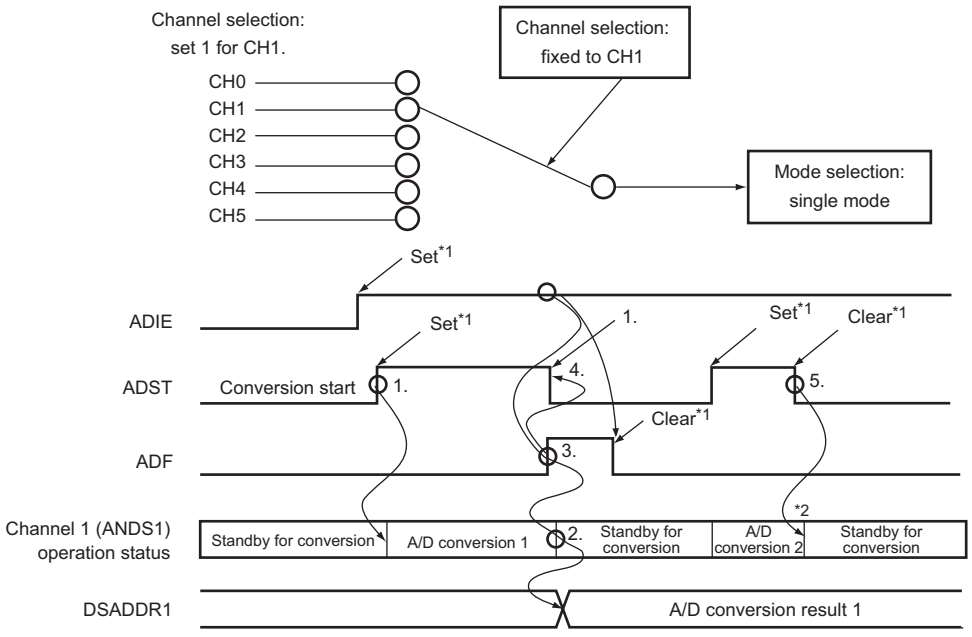
- Use channel 1.
- Enable ΔΣ A/D interrupts
- Generate ΔΣ A/D conversion complete interrupt requests (DSADI) * (starting DMA by DSADI is disabled)

Note: * The source of DSADI is as follows:



[Description of Operation]

1. When the A/D start (ADST) bit in the ΔΣ A/D control/status register (DSADCSR) is set to 1 by software or the trigger selected in the timer trigger select (TRGS1, TRGS0) bits of DSADCSR, A/D conversion on the selected channel is started.
2. When the A/D conversion is complete, the A/D conversion result data is transferred to the ΔΣ A/D data register (DSADDR1) that corresponds to channel 1.
3. When the A/D conversion result is transferred to the register and the ΔΣ A/D converter stops, the ADF bit in DSADCSR is set to 1. At this time, a DSADI interrupt request is generated (by clearing the ADF flag during the interrupt) since the ADIE bit is set to 1.
4. The ADST bit holds 1 during A/D conversion and is cleared automatically when the conversion is complete. Subsequently when the ADST bit is set to 1, A/D conversion on the selected channel is started again.
5. When the ADST bit is cleared during A/D conversion, the A/D conversion is aborted and the ΔΣ A/D converter enters the standby state.



Notes: 1. Set by software
2 . The on-going conversion data is discarded.

Figure 5.6 Example of ΔΣ A/D Converter Operation in Single Mode (Single Channel: Channel 1 Selected)

5.6.2 Single Mode (Multiple Channels)

The operation in single mode is described below. Figure 5.7 shows an example of ΔΣ A/D converter operation in single mode (multiple channels: channels 1, 2, 4 selected).

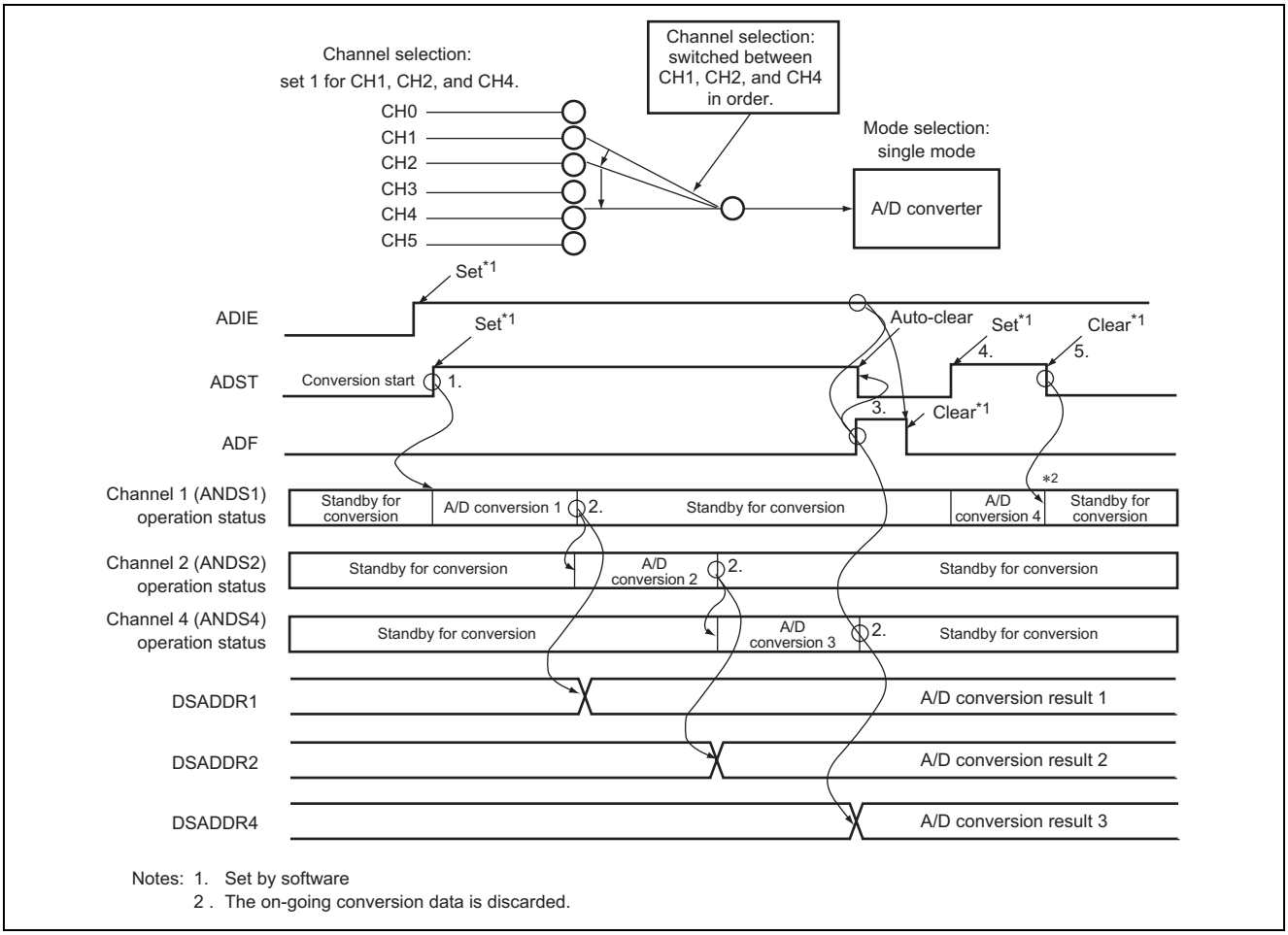
[Operating Conditions]

- Use channels 1, 2, and 4.
- Enable ΔΣ A/D interrupts
- Generate ΔΣ A/D conversion complete interrupt requests (DSADI) * (starting DMA by DSADI is disabled).

Note: * Refer to section 5.6.1 for Operating Conditions for the source of DSADI.

[Description of Operation]

1. When the ADST bit in DSADCSR is set to 1 by software or the trigger selected in the timer trigger select (TRGS1, TRGS0) bits of DSADCSR, A/D conversions on channels 1, 2 and 4 starts. The start of A/D conversion on the individual channels is in accord with the order of execution for the channel, with selection proceeding in an order of precedence from channel1.
2. When the A/D conversion on each channel is complete, the A/D conversion result data is transferred to the ΔΣ A/D data register (DSADDRn: n = 1, 2, 4).
3. When the A/D conversions on all selected channels are complete, the ADF bit is set to 1. At this time, a DSADI interrupt request is generated (by clearing the ADF flag during the interrupt) since the ADIE bit is set to 1.
4. The ADST bit holds 1 during A/D conversion and is cleared automatically when the conversion is complete. Subsequently when the ADST bit is set to 1, A/D conversion is started on the selected channel from channel 1 according to the order of channel execution.
5. When the ADST bit is cleared to 0during A/D conversion, the A/D conversion is aborted and the ΔΣ A/D converter enters the standby state.



Notes: 1. Set by software
2 . The on-going conversion data is discarded.

Figure 5.7 Example of ΔΣ A/D Converter Operation in Single Mode (Multiple Channels: Channel 1, 2, 4 Selected)

5.6.3 Scan Mode (Single Channel)

The operation in scan mode is described below. Figure 5.8 shows an example of ΔΣ A/D converter operation in scan mode (channel 0 selected).

The operating conditions are simplified as follows for more understandable description of the scan mode. Normally, it is recommended that starting DMA by DSADI should be enabled when the A/D conversion data is expanded into RAM.

[Operating Conditions]

- Use channel 0.
- Enable ΔΣ A/D interrupts.
- Generate ΔΣ A/D conversion complete interrupt requests (DSADI) *(starting DMA by DSADI is disabled).

Note: * Refer to section 5.6.1 for Operating Conditions of the source of DSADI.

[Description of Operation]

1. When the ADST bit in the DSADCSR is set to 1 by software or the trigger selected in the timer trigger select (TRGS1, TRGS0) bits of DSADCSR, A/D conversion is started.
2. When the A/D conversion on channel 0 is complete, the A/D conversion result data is transferred to the ΔΣA/D data register (DSADDR0.
3. When the A/D conversion on channel 0 is complete, the ADF bit is set to 1. At this time, a DSADI interrupt request is generated (by clearing the ADF flag in the interrupt) since the ADIE bit is set to 1.
4. The ΔΣA/D converter performs A/D conversion on channel 0 again. The ADST bit is not cleared automatically and the steps from 2 to 4 are repeated while it is set to 1.
5. When the ADST bit is cleared to 0, the A/D conversion is aborted and the ΔΣA/D converter enters the standby state. After that, then the ADST bit is set to 1, A/D conversion is started on channel 0 again.

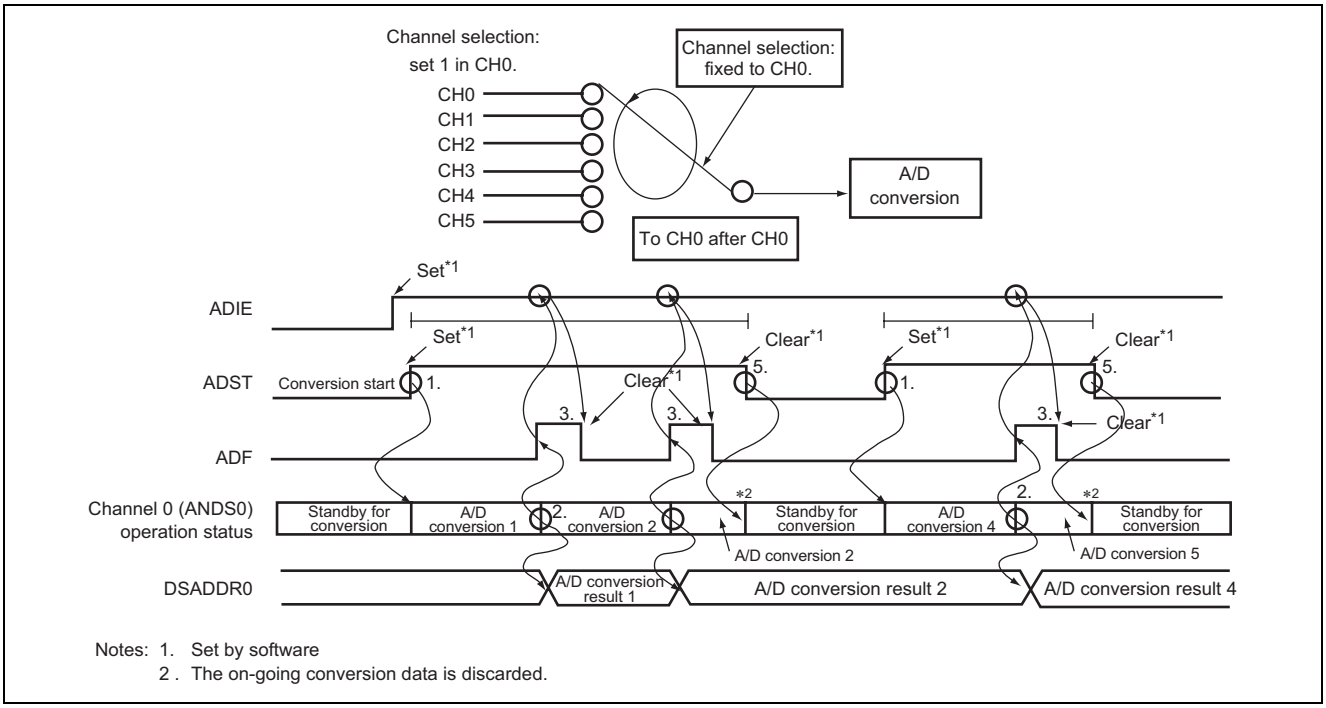


Figure 5.8 Example of ΔΣA/D Converter Operation in Scan Mode (Single Channel: Channel 0)

5.6.4 Scan Mode (Multiple Channels)

The operation in the scan mode is described below. Figure 5.9 shows an example of ΔΣA/D converter operation in the scan mode (channels 0 to 2 selected).

The operating conditions are as follows for more understandable description of the scan mode. Normally, it is recommended that starting DMA by DSADI should be enabled if the A/D conversion data is expanded into RAM.

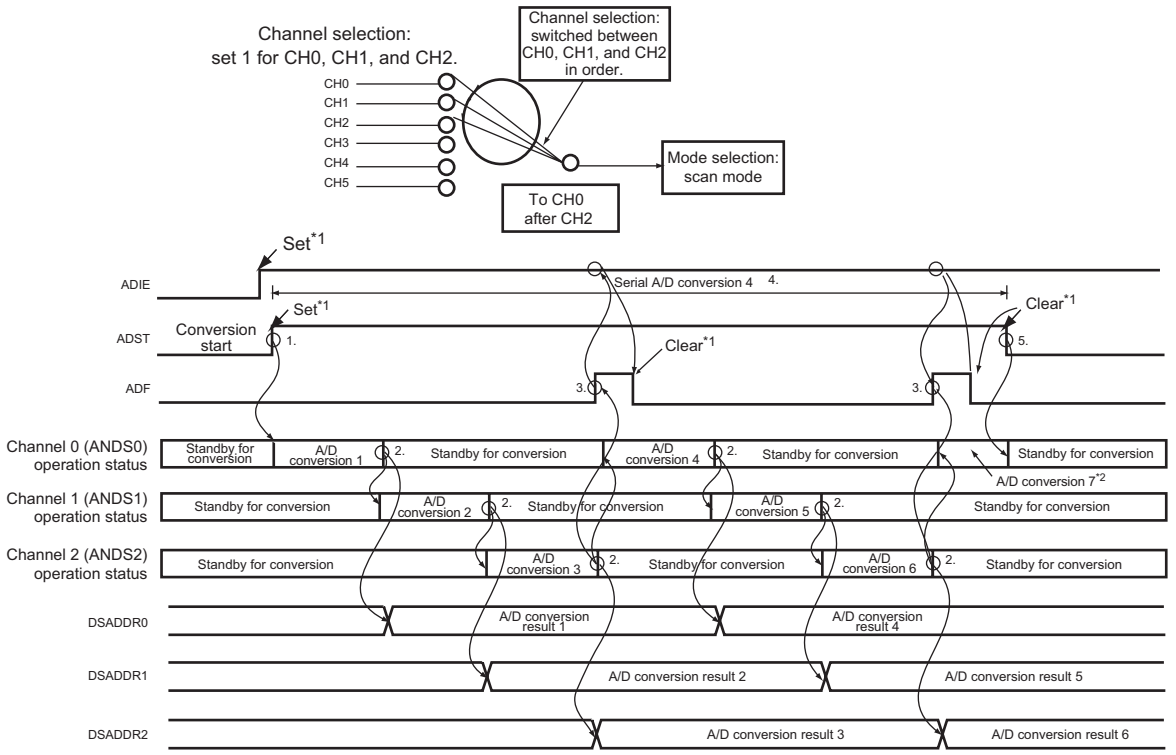
[Operating Conditions]

- Use channels 0 to 2.
- Enable ΔΣ A/D interrupts.
- Generate ΔΣ A/D conversion complete interrupt requests (DSADI) *(starting DMA by DSADI is disabled).

Note: * Refer to section 5.6.1 for Operating Conditions on the source of DSADI.

[Description of Operation]

1. When the ADST in DSADCSR is set to 1 by software or the trigger selected in the timer trigger select (TRGS1, TRGS0) bits of DSADCSR, A/D conversion is started. The channel on which A/D conversion is started is selected in accord with the order of execution for the channel with selection proceeding in an order of precedence from channel 0.
2. When the A/D conversion on each channel is complete, the A/D conversion result data is transferred to the ΔΣ A/D data register (DSADDRn: n = 0-2).
3. When the A/D conversions on all selected channels are complete, the ADF bit is set to 1. At this time, a DSADI interrupt request is generated (by clearing the ADF flag in the interrupt) since the ADIE bit is set to 1.
4. The ΔΣ A/D converter performs A/D conversion on the selected channel from channel 0 in the order of channel execution again. The ADST bit is not cleared automatically and the steps from 2 to 4 are repeated while it is set to 1.
5. When the ADST bit is cleared to 0, the A/D conversion is aborted and the ΔΣ A/D converter enters the standby state. After that, when the ADST bit is set to 1, A/D conversion on selected channel is started from channel 0 in the order of channel execution again.



Notes: 1. Set by software
2 . The on-going conversion data is discarded.

Figure 5.9 Example of ΔΣ A/D Converter Operation in Scan Mode (Scan Mode: Channels 0 to 2 Selected)

6. Recommended External Circuit and Considerations

6.1 Recommended External Circuit (Single-Ended Input, Differential Input)

Figure 6.1 shows an example of external circuit for the H8SX family ΔΣ A/D converter (single-ended input, differential input). When you design boards, note that a voltage drop may occur in analog signals based on the relationship between the resistance value in the low pass filter and the input impedance.

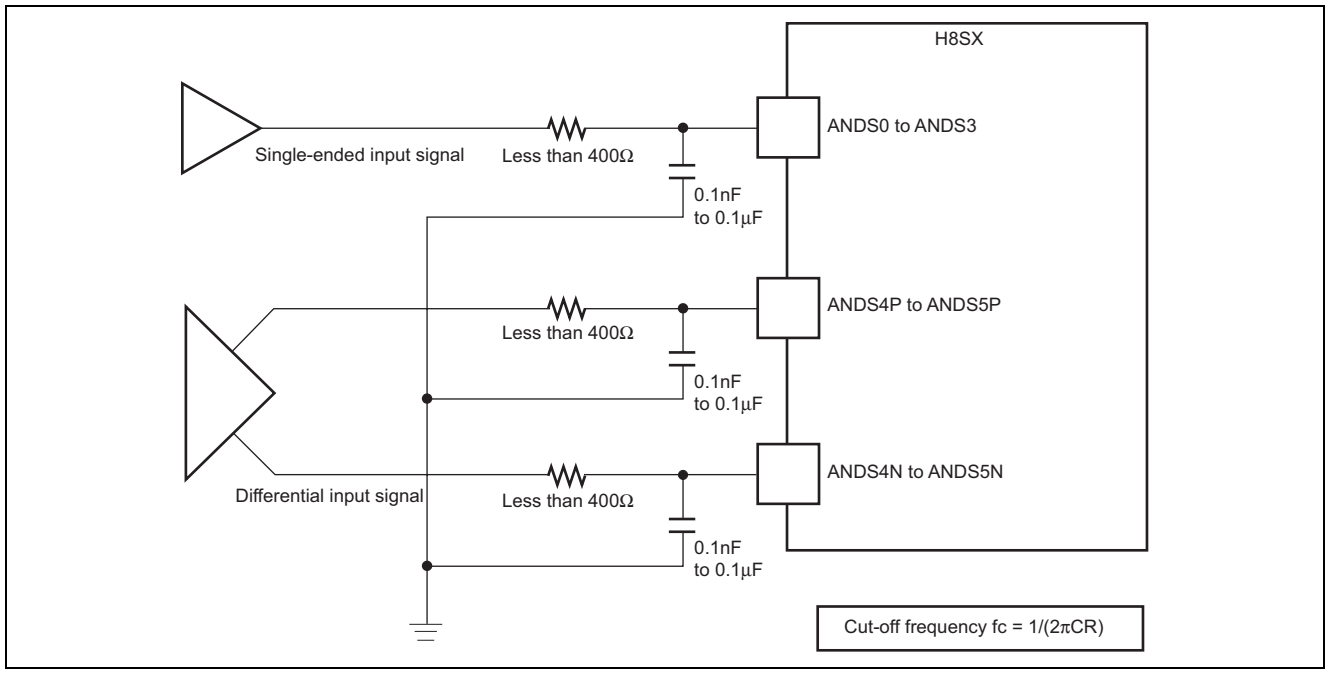


Figure 6.1 Example of External Circuit for ΔΣ A/D Converter (Single-Ended Input, Differential Input)

6.2 Recommended External Circuit (Power Supply)

Figure 6.2 shows an example of external circuit (power supply) for the H8SX family ΔΣ A/D converter. Make sure to provide stable voltage levels to each power supply and ground pins. When you design boards, extra care for AVrefT–AVrefB must be taken because it is used as the ΔΣ reference voltage.

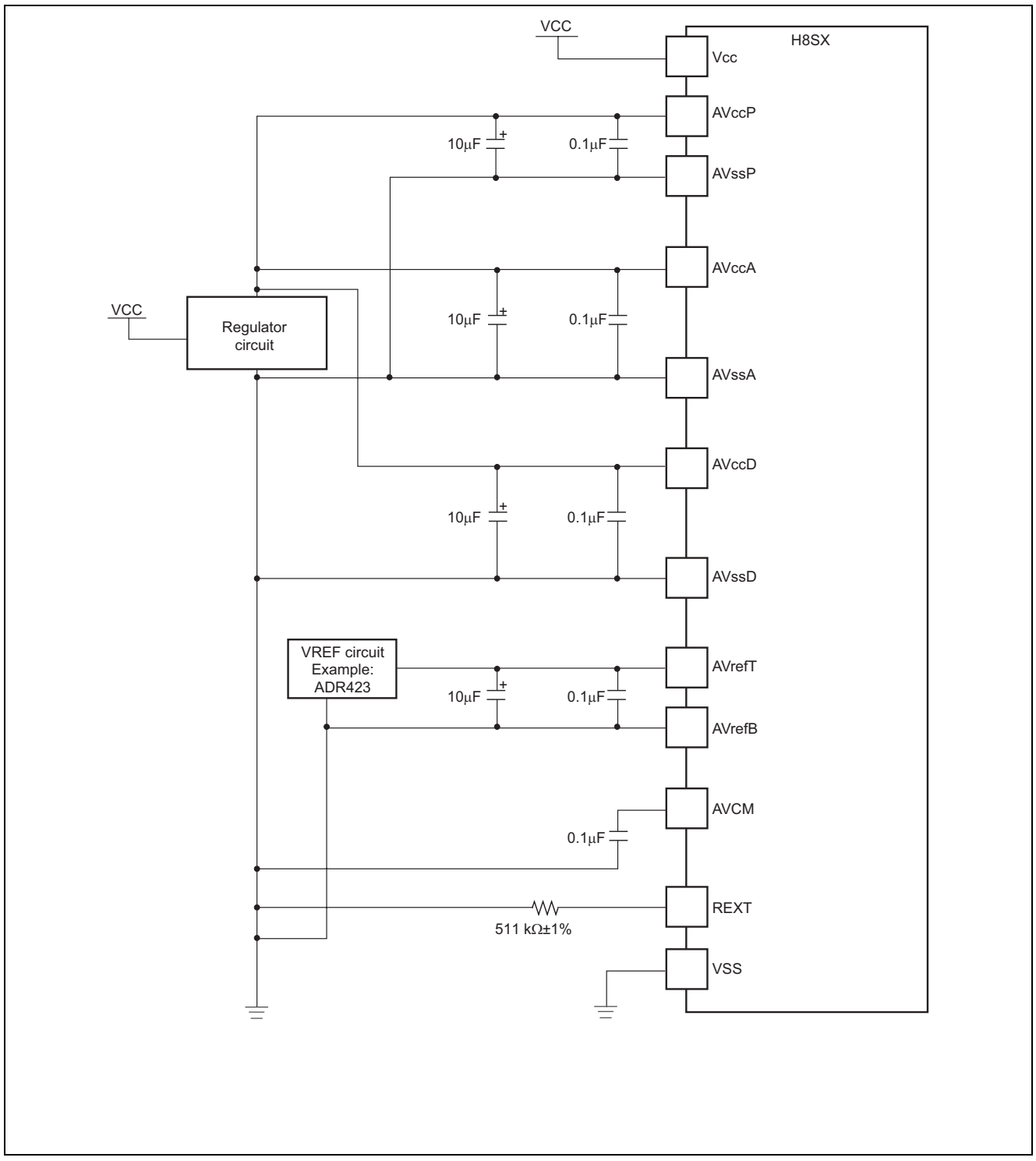


Figure 6.2 Example of External Circuit for ΔΣ A/D Converter (Power Supply)

6.3 Considerations

To use the ΔΣ A/D converter with better accuracy, consider the followings:

Notes on designing boards

1. For noise reason, separate the VCC layer from the GND layer in a multi-layer board to reduce noise on input lines.
2. Separate the analog power supplies (AvccD, AvccA, AvccP, AVrefT) from the digital power supply so far as cost and board space permits.
3. Note that locating digital circuit patterns below the analog circuit may cause mutual interference.

Setting ranges for analog power supply pins and others

Using the LSI with voltages outside the following ranges may degrade the reliability of the LSI.

- AvccA = AvccD = AvccP, AvssA = AvssD = AVssP must always hold.
- AvccA = AVrefT, AVrefT > AvrefB, AvrefB = 0V must always hold.

7. Documents for Reference

7.1 Calculation Formula for A/D Conversion Result

The ΔΣ A/D converter stores the results of A/D conversion in 16-bit data registers. For single-ended inputs, the setting for offset canceling DAC and gain selection are involved when the result value of A/D conversion is represented in a calculation formula. For differential inputs, the result of A/D conversion is obtained by calculation, so the error in the precision of conversion generates errors in the actual result of A/D conversion.

In the calculation formula, the variables shown in the following table are used.

Table 7.1 List of Variables in the Calculation Formula

Variable	Unit	Range	Description	Setting
gain	Time	1 to 8	Amplification ratio selected by the gain setting	Bits GAIN1 and GAIN0 in DSADCR
DSADOFn	Hex	H'000 to H'3FFF	Offset canceling DAC input	DSADOFn corresponding to the channel
DOF	V	0 to AvrefT (V)	Analog level set by DSADOFn	Set by DSADOFn and AVrefT
ANDSn	V	0 to AvrefT (V)	Single-ended analog input level	ANDSn pin for the channel
ANDSnP	V	0 to AvrefT (V)	Positive side of differential analog input	ANDSnP pin for the channel
ANDSnN	V	0 to AvrefT (V)	Negative side of differential analog input	ANDSnN pin for the channel
result	Numeric value	Up to ±262144	The result of A/D conversion on the channel (integer)	Values in the formula

7.1.1 For Single-Ended Inputs

For single-ended inputs, DOF is obtained by integrating the voltage level of AVrefT over DSADOFn/1024. A/D conversion is of the analog level obtained by subtracting DOF from the analog input level on the ANDSn pin and multiplying the result by the gain.

$$DOF = \frac{DSADOFn}{1024} \times (AVrefT - AVrefB)$$

$$result = \frac{(ANDSn - DOF) \times gain}{AVrefT - AVrefB} \times 2^{15}$$

Note: AVrefB = 0V

7.1.2 For Differential Input

For differential input, the analog level of the ANDSnP pin is subtracted from that of the ANDSnN pin. This voltage level difference is amplified by gain times and then the resulting level is A/D converted.

$$result = \frac{(ANDSnP - ANDSnN) \times gain}{AVrefT - AVrefB} \times 2^{15}$$

Note: AVrefB = 0V

7.1.3 Storing the Calculated Value in the Register

The result can be either positive or negative. It is stored in DSADDRn as a 16-bit signed binary number (two's complement). When the result exceeds the maximum positive value, +32767 (H'7FFF) is stored in DSADDRn. Similarly, when the result exceeds the negative range of 16-bit values, -32768 (H'8000) is stored in DSADDRn.

When result > +32768: DSADDRn = H'7FFF

When +32768 > result > 0 : DSADDRn = result

When 0 > result > -32768 : DSADDRn = result + 65536

When -32768 > result: DSADDRn = H'8000

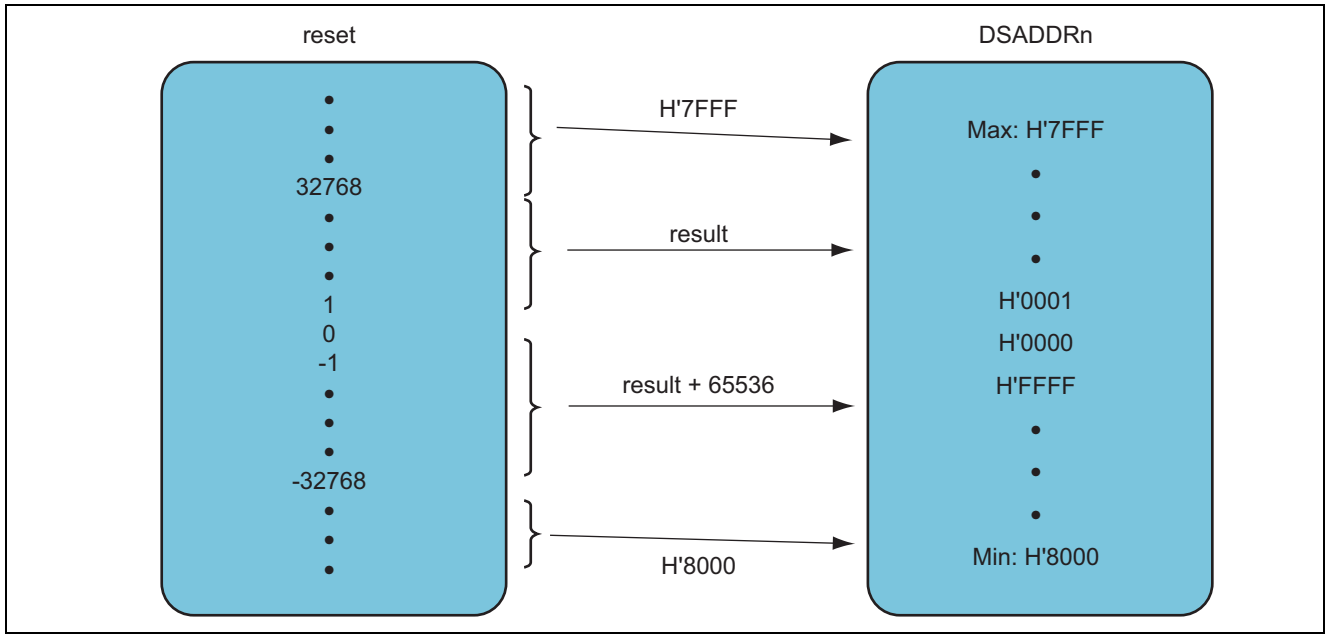


Figure 7.1 Storing the Calculated Value in the Register

7.2 Setting the Divided Clock for the ΔΣ A/D Converter

There is a limitation on the oversampling frequency (fos) for the ΔΣ A/D converter as follows:

Min: 2.5 MHz to Max: 3.3 MHz

Use the following table to set Aϕ according to the EXTAL input clock.

Table 7.2 ΔΣ A/D Converter Clock (Aϕ) Frequency against EXTAL Frequency

EXTAL Input Clock Frequency (MHz)	Aϕ Setting			
	ACK2–0 Setting	Multiplication Factor	Aϕ Frequency (MHz)	fos (MHz)
8.0 to 9.9	B'011	EXTAL × 8 × (1/3)	21.3 to 26.4	2.7 to 3.3
10.0 to 13.2	B'010	EXTAL × 8 × (1/4)	20.0 to 26.4	2.5 to 3.3
13.2 to 16.5	B'001	EXTAL × 8 × (1/5)	21.1 to 26.4	2.6 to 3.3
16.5 to 18.0	B'000	EXTAL × 8 × (1/6)	22.0 to 26.4	2.8 to 3.3

7.3 Recommended Input Range and Digital Values

The following figure shows the recommended input range in which the ΔΣ A/D converter can perform conversion with a high accuracy.

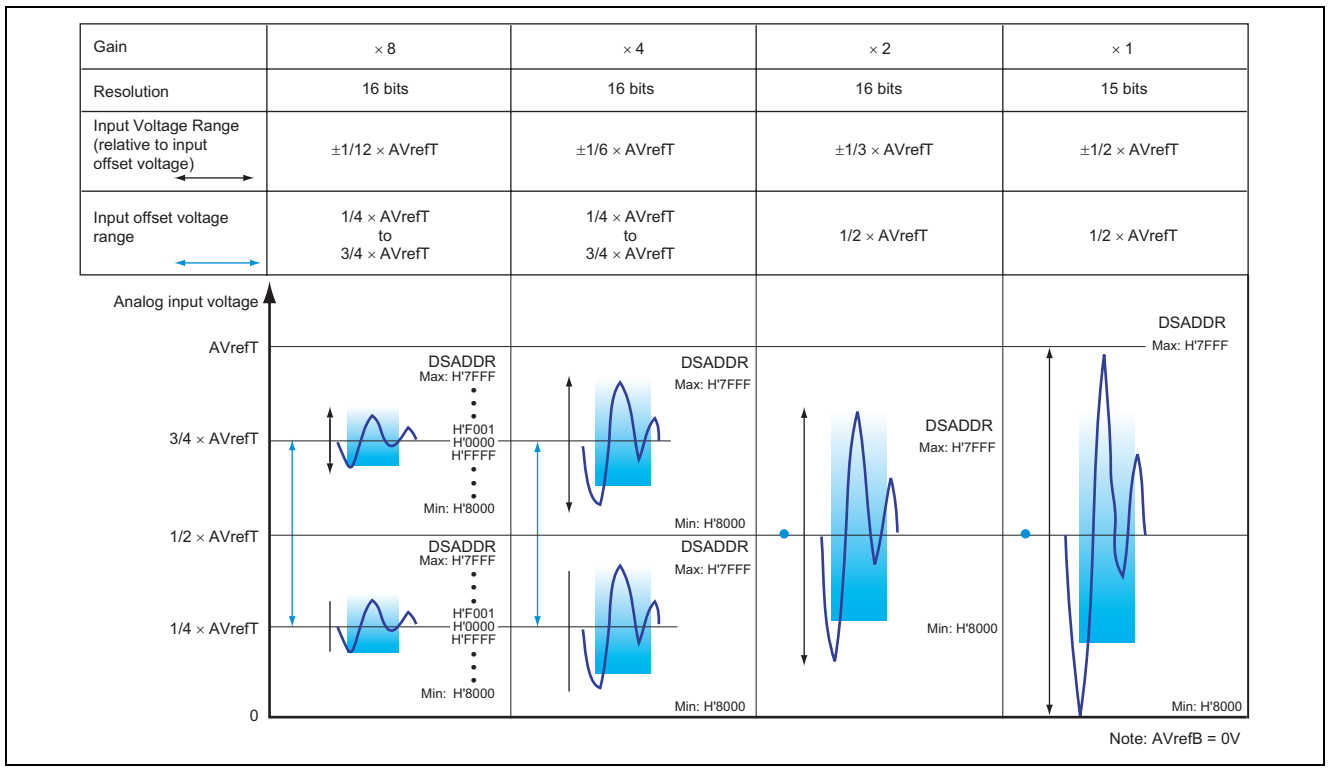


Figure 7.2 Recommended Input Range and Digital Values (Single-Ended Inputs)

Gain	× 8	× 4	× 2	× 1
Resolution	16 bits	16 bits	16 bits	15 bits
Input Voltage Range (relative to input offset voltage) ◄——►	±1/12 × AVrefT	±1/6 × AVrefT	±1/3 × AVrefT	±1/2 × AVrefT
Input offset voltage range ◄——►	1/4 × AVrefT to 3/4 × AVrefT	1/4 × AVrefT to 3/4 × AVrefT	1/2 × AVrefT	1/2 × AVrefT

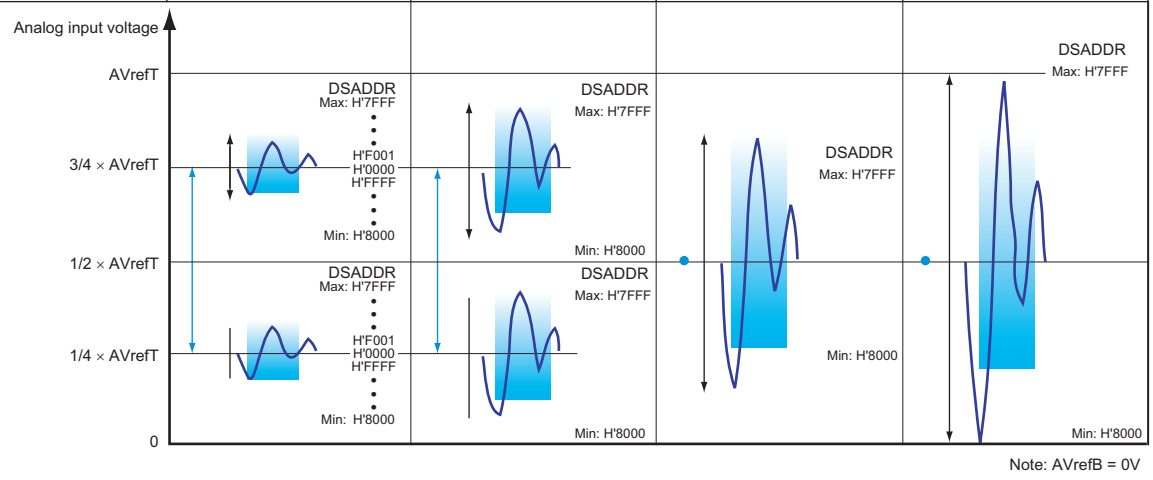


Figure 7.3 Recommended Input Range and Digital Values (Differential Inputs)

Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	May 20, 08	—	First edition issued

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