Brushed DC Motor Programmable Speed Regulator SLG47004

This application note describes how to design and build a low noise high performance low cost brushed DC motor programable speed regulator. The regulator is immune to the temperature, voltage, and motor load variation. Also, this circuit does not care about the motor coil resistance which allows using different motors in the same application without any adjustments.

The application note comes complete with a design file that can be found in the Reference section.

Contents

1. Terms and Definitions

DC	Direct Current
GPO	General Purpose Output
IC	Integrated Circuit
I/O	Input / Output
I2C	Inter-Integrated Circuit Protocol
LSB	Less Significant Bit
MSB	Most Significant Bit
MOSFET	Metal-oxide Semiconductor Field-effect Transistor
OPAMP	Operational Amplifier
OSC	Oscillator
PWM	Pulse Width Modulation
P-FET	P-type Field-effect Transistor
RPM	Revolution Per Second
SCL	Signal Clock
SDA	Signal Data
VREF	Voltage Reference

2. References

For related documents and software, please visit:

https://www.dialog-semiconductor.com/configurable-mixed-signal

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] AN-CM-338 Brushed DC Motor Programmable Speed Regulator.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

[5] SLG47004 Datasheet, Renesas Electronics

3. Introduction

The circuit described in this document is designed for devices where a low-power brushed DC motor is used. Where the stability of the motor speed and low noise are critical. The regulator is immune to the temperature, voltage, and motor load variation. Also, this circuit is not sensitive to the motor coil resistance which allows using different motors in the same application without any adjustments. The motor speed is pre-programmed and does not require trimming after assembly. Although, it is possible to re-program it to a different speed via I²C.

Unlike traditional circuits (see Figure 1) this design does not require any feedback sensor. In this case, the motor itself is a sensor. Other, traditional designs (see Figure 2) are dependent on the motor coil resistance. Both require post-production trimming.

Some applications (audio, for example) are very noise sensitive. That makes any PWM motor controllers not suitable.

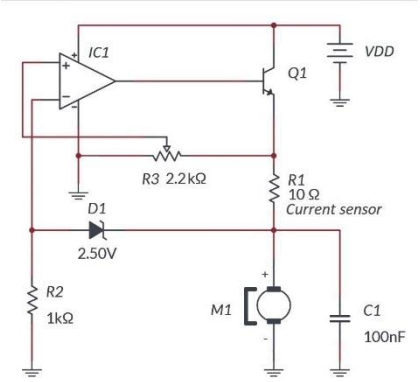

Figure 1: Traditional DC Motor Speed Controller with Current Sensor

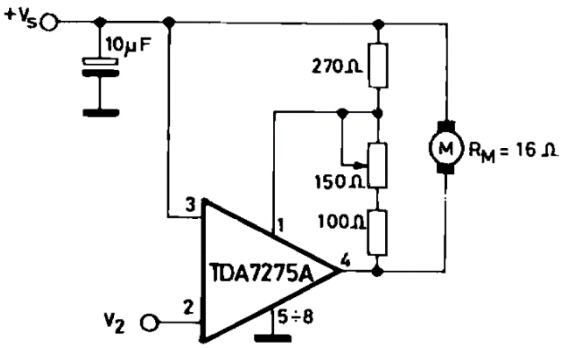

Figure 2: Traditional DC Motor Speed Controller Based on TDA7275A

Every brushed DC motor produces interference when brushes switch from coil to coil. This is considered one of the biggest downsides of such a motor. Unfiltered it is capable to interrupt the normal work of the circuits powered from the same power source or simply situated close by. While it is possible to filter out to an acceptable level the interference using a capacitor connected in parallel to the motor (in some cases ferrite coil in series), it is impossible to get rid of it completely.

In the case of the design described in this document, the small leftover interference is used to determine the motor speed. In most cases, cheap low voltage low power brushed DC motors have three moving coils. Each of them produces interference in a form of spikes, thus the frequency of the spikes is three times the revolutions of

the rotor. So, by counting the spikes it is possible to not only determine the speed but also control it by automatically adjusting to a pre-programmed value. All this (and more) can be achieved by using the SLG47004 a versatile programable mixed IC with only basic external components. See the schematic diagram in Figure 3.

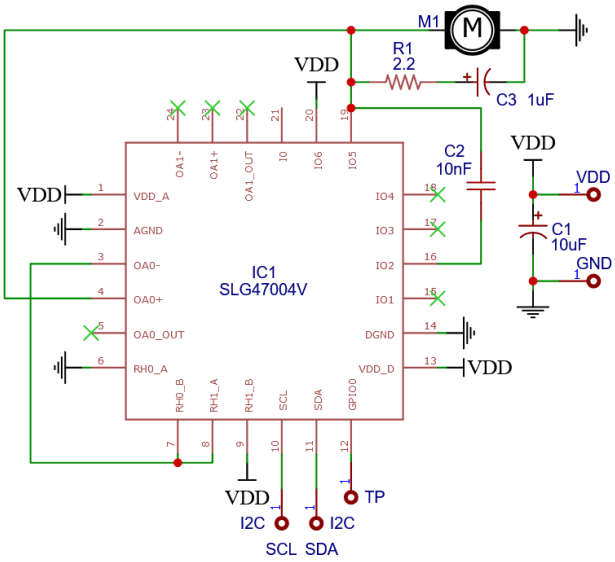

Figure 3: Brushed DC Motor Programmable Speed Regulator Schematic Diagram

4. Design Operation

4.1 Schematic Design

As previously mentioned, only one chip is used in this design. The SLG47004 IC combines all necessary analog and digital macrocells in a tiny 3 x 3 mm STQFN-24 package. See Figure 4 for a complete schematic diagram in the GreenPAK Designer project.

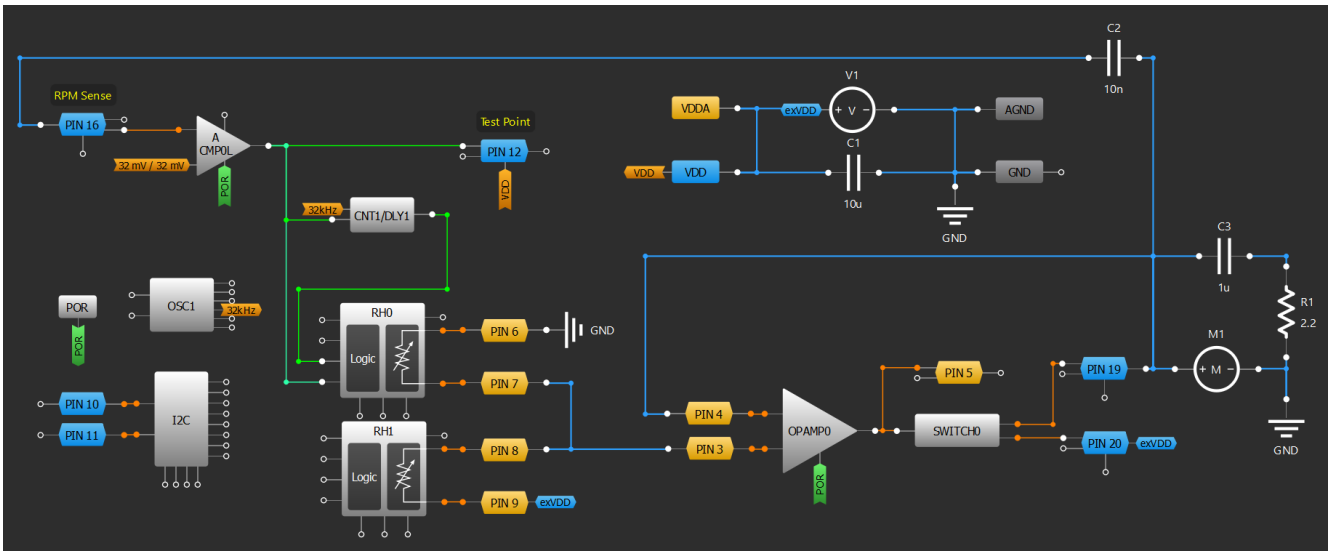

Figure 4: Brushed DC Motor Programmable Speed Regulator Project

To understand how it works, see the simplified schematic diagram in Figure 5.

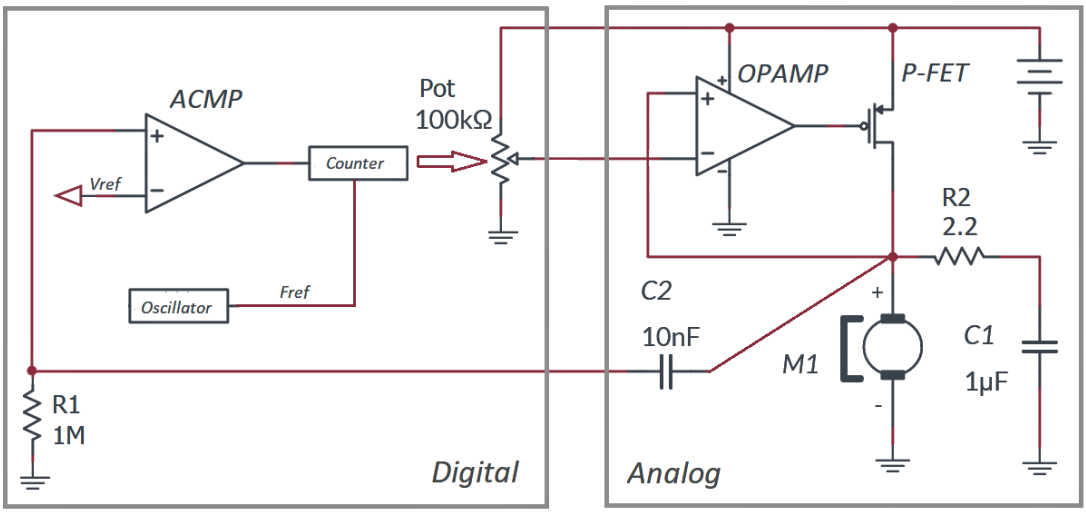

Figure 5: Simplified Schematic Diagram

The analog part is a simple voltage regulator with a power P-channel MOSFET on the output. But instead of a voltage reference, it has a digital potentiometer controlled by a digital part of the device.

The digital part consists of the ACMP which detects the small spikes coming from motor brushes. Capacitor C2 blocks DC voltage but lets through the spikes. Amplified to a VDD level they go to the Counter, which is set to a frequency detection mode, where the spike frequency is compared to a reference frequency coming from the oscillator.

When the device is powered on the resistance of the digital potentiometer is as pre-set, so some small voltage goes through a current amplifier (voltage regulator) built out of the OPAMP and P-FET and comes to the motor. It starts rotating and produces spikes. With each detected spike the digital pot resistance will increase by one bit slowly increasing the motor voltage. As a result, the motor speed will be rising until the spike frequency matches the reference frequency. And when it does, the counter will signal the potentiometer to decrease its resistance by one bit with each spike. The voltage will drop along with the motor speed. The counter will detect the frequency drop and signal the pot to increase its resistance and the cycle does on.

In other words, the voltage on the motor rises while the spike frequency is lower than the reference frequency, and vice versa. Once the motor speed settles the potentiometer will go up and down one step (1 LSB) keeping the speed stable within ±1 LSB.

Ideally, it would take ±1 LSB to settle the motor speed, but due to the inertia, it may take up to ±50 LSB. The heavier the motor load, the more LSB it takes to settle the speed.

The frequency detector period can be calculated using the formula below:

$$\boldsymbol{T} = \frac{\mathbf{1}}{\boldsymbol{RPS}\times\boldsymbol{n}} \times \mathbf{1000} \text{ (ms)},$$

Where:

T – period
RPS – revolutions per second ($\boldsymbol{RPS} = \frac{\boldsymbol{RPM}}{\mathbf{60}}$)
n – number of motor coils

Should be noted that the oscillator frequency must be selected so the counter data is close to half the counter resolution given the desired RPM (for instance, 127 for the 8-bit counter). Leaving maximum headroom for regulating the motor speed.

Using P-FET on the output of the regulator has a benefit of a very low voltage drop, allowing the VDD margin as low as 100 mV.

See figures 6 to 9 for oscilloscope screenshots demonstrating the stability of the device at different VDD levels.

Legend:

- Yellow – test point output (Pin 12)
- Blue – ACMP input
- Purple – motor DC voltage

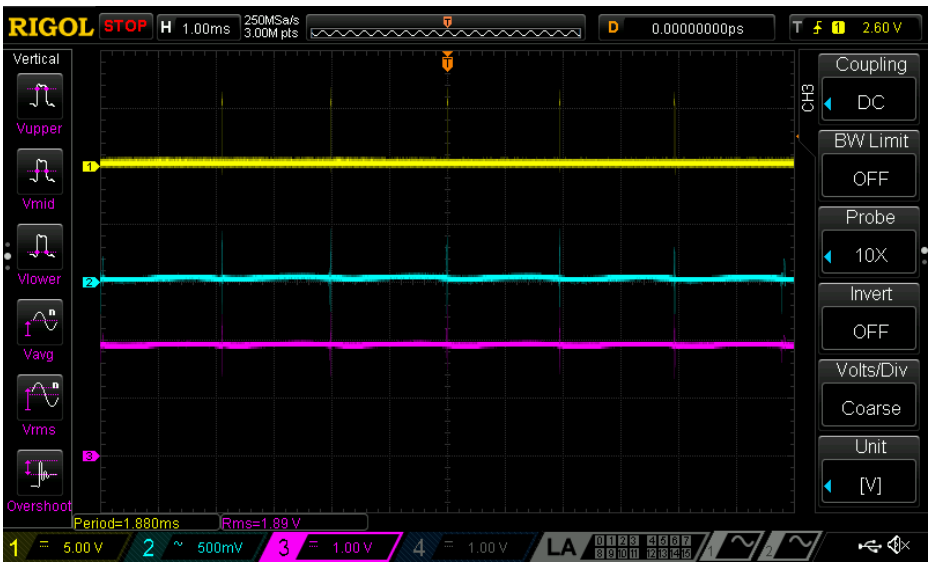

Figure 6: VDD = 5 V

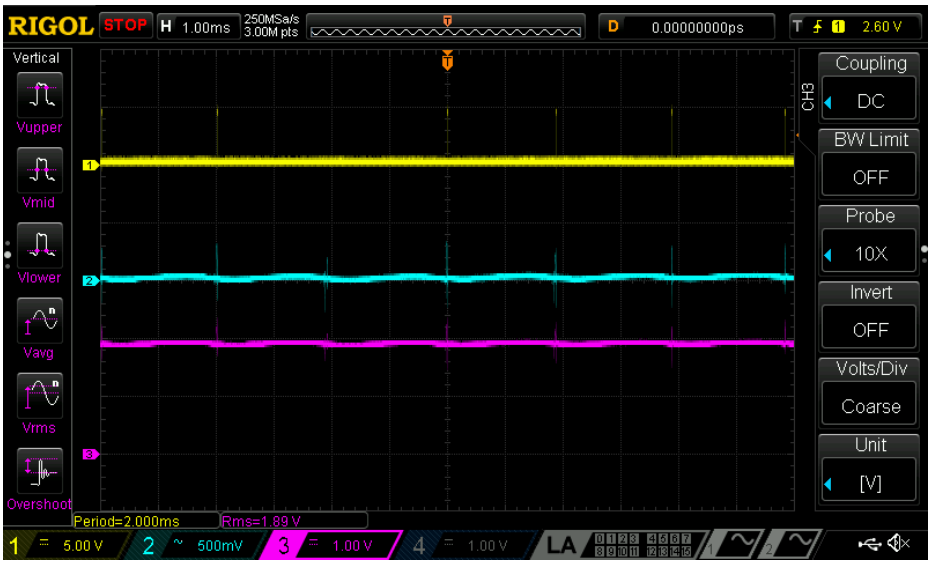

Figure 7: VDD = 4 V

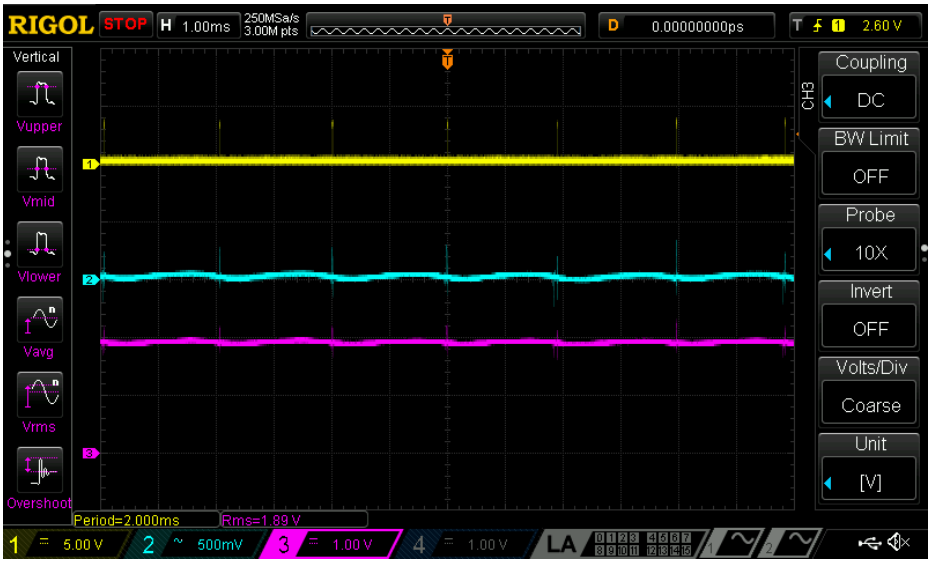

Figure 8: VDD = 3 V

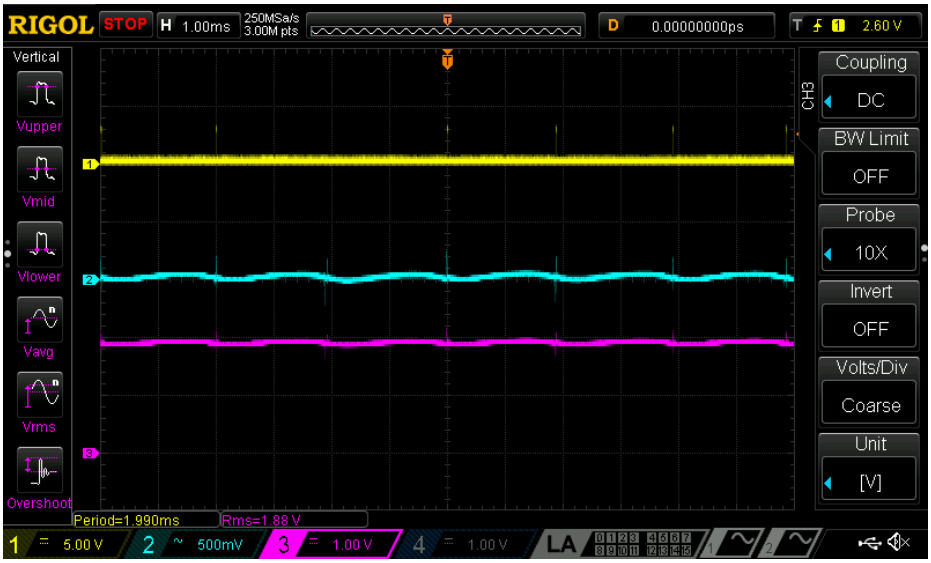

Figure 9: VDD = 2.5 V

As an alternative design, an optical RPM feedback sensor can be used, see Figure 10. This method ensures greater motor speed accuracy and stability as there are more pulses per revolution. The frequency detector and ACMP Vref should be adjusted accordingly. In this case, in the formula for calculating the period «N», stands for the number of the gear tooths. The downside of this design is the cost of an extra sensor and increased power consumption.

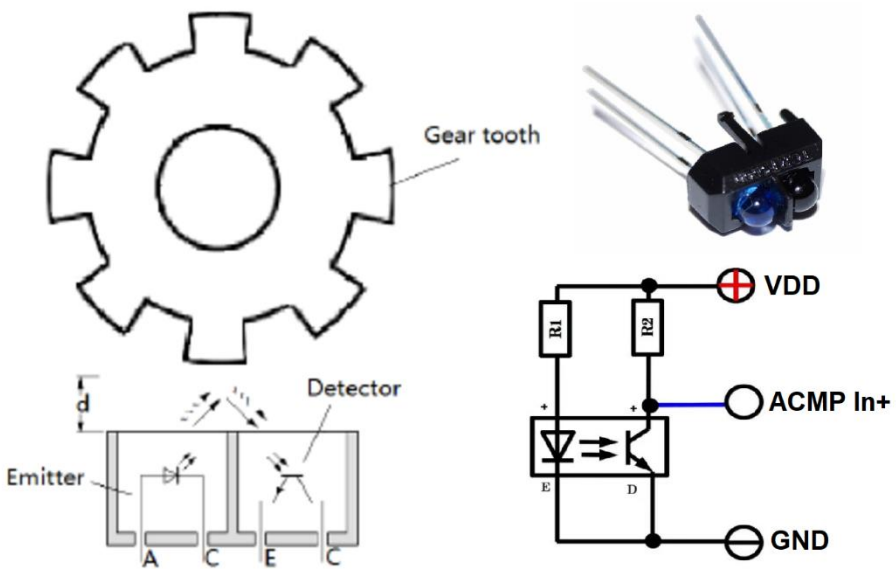

Figure 10: Optical RPM Feedback Sensor

In both designs, PIN 12 is used as a test point. Using an oscilloscope with probes connected to PIN 16 and PIN 12 it is possible to check if all input spikes are picked up by the ACMP. In some cases, the ACMP Vref should be adjusted so every input spike is picked up and converted to a logic-level pulse.

4.2 Additional Design Features

The suggested design is the simplest one. Its main goal is to explain its principles.

However, the SLG47004 has plenty of unused macrocells which allow for improving performance and adding new features to the design.

For example, instead of the 8-bit counter, the 16-bit counter can be used. This will drastically improve the frequency measuring accuracy and allow fine-tuning of the motor speed. In this case, the oscillator frequency should be increased accordingly.

Another improvement can be made by adding a feature of selecting different motor speeds. By adding more frequency detect macrocells and switching between them using simple logic (LUTs and DFFs), it is possible to create a device with user-selectable pre-programmed motor speeds.

4.3 Macrocell Configuration

Table 1: PIN settings

Properties	PIN 3 to 9, 16, 19, and 20	PIN 16	PIN 10 and 11	PIN 12
I/O selection	Analog input/output	Analog input/output	Digital input	Digital output
Input mode OE=0	Analog input/output	Analog input/output	Digital in without Schmitt trigger	None
Output mode OE=1	Analog input/output	Analog input/output	None	2x push pull
Resistor	Floating	Pull Down	Floating	Floating
Resistor value	Floating	1M	Floating	Floating

Table 2: OPAMP Settings

Properties	OPAMP0
Mode	OpAmp mode
Bandwidth Selection	128 kHz
Charge Pump	Enable CP
Supporting Blocks On/Off	Follows OpAmp
Vref connection	Disconnected
Vref	32 mV

Table 3: Oscillator

Properties	OSC1
Control pin mode	Power down
OSC power mode	Force Power On
Clock selector	OSC
CLK predivider by:	8
OUT0 second divider by:	8
OUT1 second divider by:	1

Table 4: Digital Rheostat Settings

Properties	RH0	RN1
Mode	None	Potentiometer
Charge Pump Enable	From matrix	From matrix
Charge Pump Clock	Auto selection	Auto selection

Properties	RH0	RN1
Auto-Trim	Disable	Disable
Active level for UP/DOWN	Up when HIGH	Up when HIGH
Resistance (initial data)	512	512
UP/DOWN source	Ext. (From matrix)	Ext. (From matrix)
Clock	Ext. Clock (From matrix)	Ext. Clock (From matrix)

Table 5: Analog Switch Settings

Properties	SWITCH0
Mode	Analog Switch
Big PMOS control	By OPAMP
Small NMOS enable	Disable
Half Bridge Dead Time Select	Bypass

Table 6: CNT/DLY Settings

Properties	8-bit CNT1/DLY1 (MF1)
Mode	Frequency detect
Counter data	63
Edge select	Rising
DLY IN init. value	Bypass the initial
Output polarity	Inverted (nOUT)
Mode signal sync.	Bypass
Clock	OSC1/8

I2C Settings: default

5. Conclusions

As can be seen, designing and building a low noise high performance low cost brushed DC motor programable speed regulator using the OPAMP PAK is very easy. The SLG47004 turned out to be the perfect IC for the design containing all necessary analog and digital macrocells. The design shown in this document is one of many versions of the device that can be built based on the SLG47004. Some unused macrocells can be used to design additional functions as suggested in section 4.2.

This slightly modified design was used as a DC motor speed regulator for a high-performance vinyl turntable. An optical feedback sensor and a 16-bit counter were used to sense and stabilize the speed. As a result, the rotating speed of the turntable was measured at exactly $33\frac{1}{3}$ RPM with a deviation of less than ±0.15%. Which far exceeds hi-fi requirements.

6. Revision History

Revision	Date	Description
1.00	May 2, 2022	Initial release.

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