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April 1st, 2010
Renesas Electronics Corporation

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M16C/64 Group

A/D Converter Operation (Repeat Mode)

1. Abstract

In repeat mode, any desired function can be selected from those listed in Table 1. In this application note, the operation of the function selected from the items in Table 1 (marked with a circle) is described.

Table 1. Contents of Settings

Set item	Content of setting		Set item	Content of setting	
Operating clock ϕ_{AD}	○	fAD divided by 12/ fAD divided by 6 /fAD divided by 4/ fAD divided by 3/ fAD divided by 2/ fAD	Analog input pin	○	One from AN0–AN7
					One from AN0_0–AN0_7
					One from AN2_0–AN2_7
A/D conversion start condition	○	Software trigger	Extension analog input pin	○	Unused
		\overline{ADTRG} trigger			ANEX0 pin
					ANEX1 pin

2. Introduction

The application example presented in this document applies to the microcomputers listed below.

- Microcomputers: M16C/64 group

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

- Operation
- (1) When the ADCON0 register's ADST bit is set to 1 (A/D conversion start), the A/D converter starts operating.
 - (2) After the A/D conversion is finished, the content of the successive approximation register (conversion result) is transferred to the ADi register (i = 0–7). (The ADIC register's IR bit is not set to 1 (interrupt requested).)
 - (3) The A/D converter continues operating until the ADCON0 register's ADST bit is cleared by writing 0 in a program. Each time an A/D conversion is finished, the conversion result is transferred to the ADi register.

Figure 1 shows an operation timing of the A/D converter.

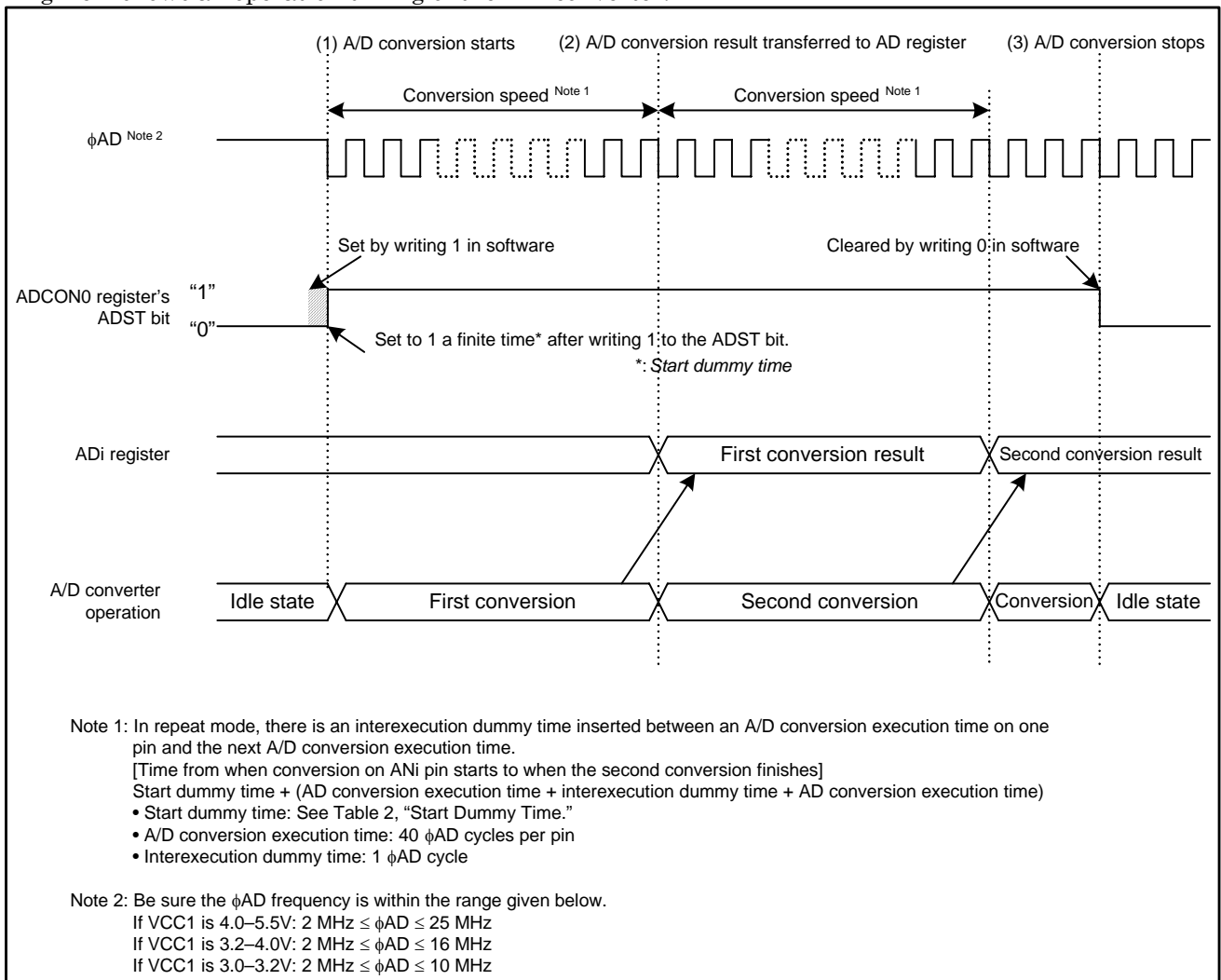


Figure 1. Operation Timing in Repeat Mode

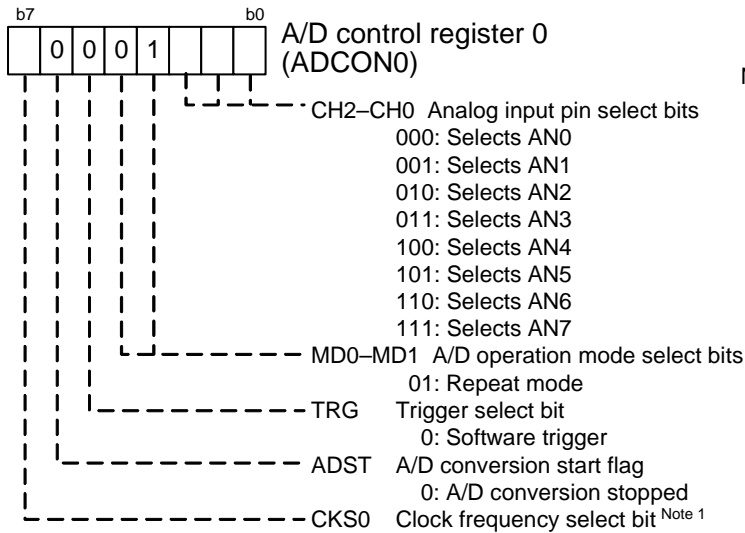
Table 2. Start Dummy Time

Selected ϕ_{AD}	Start dummy time
f_{AD}	1 to 2 f_{AD} cycles
f_{AD} divided by 2	2 to 3 f_{AD} cycles
f_{AD} divided by 3	3 to 4 f_{AD} cycles
f_{AD} divided by 4	3 to 4 f_{AD} cycles
f_{AD} divided by 6	4 to 5 f_{AD} cycles
f_{AD} divided by 12	7 to 8 f_{AD} cycles

4. How to Set Up

The following shows how to set up the registers to accomplish the operation described in Section 3, "Application Example." For details about each register, see the hardware manual of the M16C/64 group.

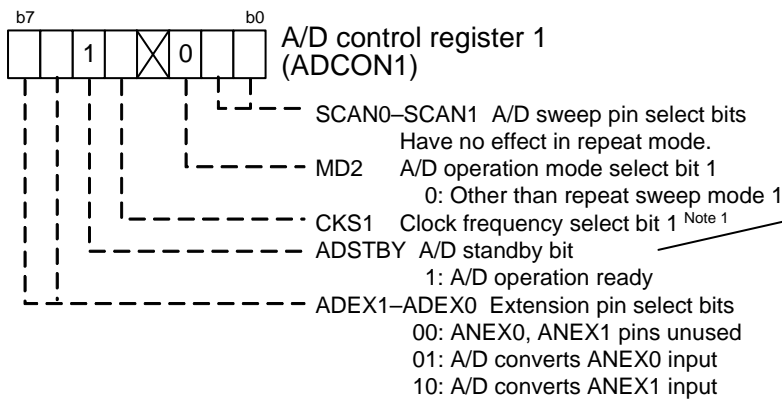
(1) Set up the A/D control register 0, A/D control register 1, and A/D control register 2.



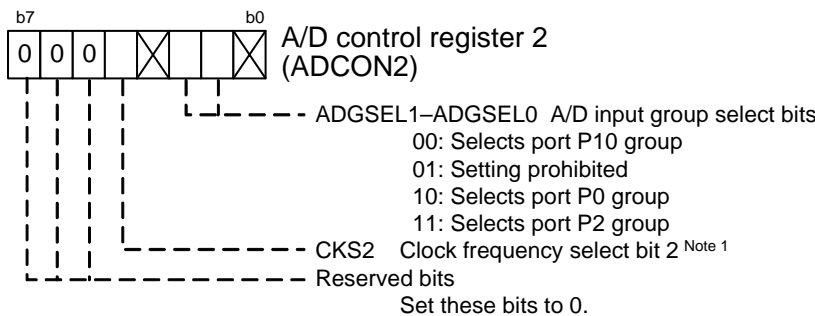
Note 1: Selection of the operating clock, ϕ_{AD}
The clock ϕ_{AD} is selected using the following register bits in combination.

- ADCON0 register's CKS0 bit
- ADCON1 register's CKS1 bit
- ADCON2 register's CKS2 bit

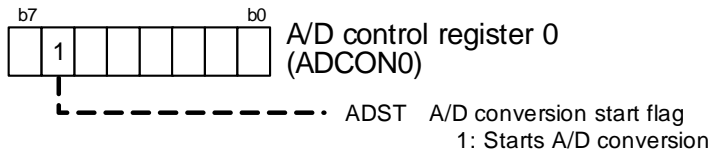
CKS2	CKS1	CKS0	ϕ_{AD}
0	0	0	f_{AD} divided by 4
0	0	1	f_{AD} divided by 2
0	1	0	f_{AD}
0	1	1	
1	0	0	f_{AD} divided by 12
1	0	1	f_{AD} divided by 6
1	1	0	f_{AD} divided by 3
1	1	1	



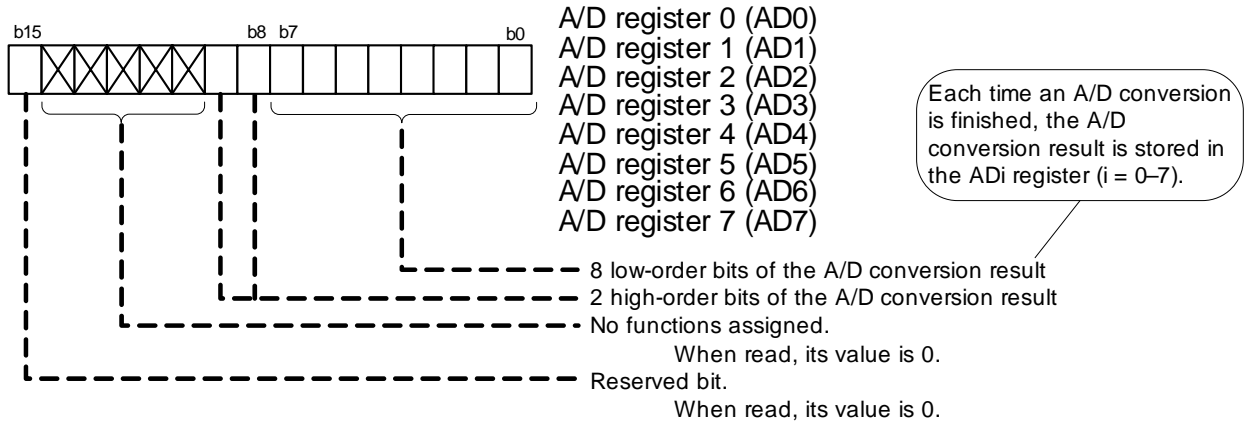
If the ADSTBY bit is changed from 0 (A/D operation stopped) to 1 (A/D operation ready), wait 1 ϕ_{AD} cycle or more before starting A/D conversion.



(2) Start A/D conversion.



(3) Read out the A/D conversion result.



5. Reference Sample Programs

Download reference sample programs from the Renesas Technology website.

Click the screen menu “Application Note” on the left side of the M16C family top page.

6. Reference Documents

Hardware manuals

M16C/64 Group Hardware Manual

(Obtain the latest edition from the Renesas Technology website.)

Technical updates and technical news

(Obtain the latest information from the Renesas Technology website.)

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REVISION HISTORY

Rev.	Issue date	Content of revision	
		Page	Points
1.00	Mar 23,2009	–	First edition issued

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