

Introduction

This application note will discuss layout recommendations for IDT clock generators with the goal of keeping EMI as low as possible. Automotive standards mostly speak about EMC (Electro Magnetic Compatibility) versus the more popular EMI (Electro Magnetic Interference). EMC is a broader term and includes sensitivity to (strong) electromagnetic fields.

Reliability is extremely important in automotive applications. For this reason, the EMC/EMI requirements are tightened, generally by 10dB to 40dB versus most non automotive EMC/EMI requirements. The requirements are also legislated by international laws and standards.

This application note will focus on EMI or the emission of electromagnetic radiation.

When working with IDT timing devices, you can divide the origin of EMI in two areas:

- 1) Clock and Data paths
- 2) Power Supply

Clocks and Data are signals and they need to be contained to prevent EMI. The higher the clock frequency or the higher the data rate, the more electromagnetic energy in the signal so the more risk of EMI. Below 10MHz or 10Mb/s can be considered low risk, 10MHz ~ 100MHz intermediate risk and >100MHz high risk. Automotive standards describe testing in the range 30MHz to 1GHz. Clock and data signals are square waves with harmonics of the main or carrier frequency spreading across the whole 30MHz ~ 1GHz spectrum.

The power supply may also be a source of EMI. Power supply filters are used to prevent power rail noise from interfering with the timing device functionality and performance, but another job for the power supply filter is to prevent noise from the timing device to get injected into the power rail and cause EMI. Actual emission of EMI is mostly from PCB traces. It is all about of the size of the 'antenna'. The timing device is relatively small so it will not emit much radiation itself but the power supply filter and specific design of the timing device can also help reduce EMI from the timing device.

IDT timing devices are designed with features to help reduce EMI. Features like slew rate throttling, slew rate programmability, on-chip termination, spread spectrum modulation and more.

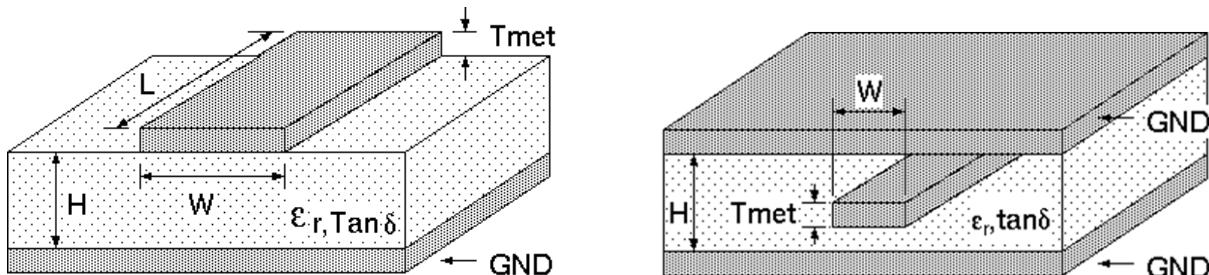
Background: PCB Trace Design

To minimize EMI, Clock and Data traces need to be designed as transmission lines. Theoretically, a properly designed transmission line does not radiate. Transmission lines usually consist of two conductors. Currents in the two conductors are equal but flow in opposite directions and cancel each other's electromagnetic field. In case of a single PCB trace, the second conductor is the ground plane underneath the trace. A so called "Return Current" flows in the ground plane directly below the PCB trace, giving the trace transmission line properties.

The design where a PCB trace runs above a ground plane layer is called a "micro strip". An alternative design to better shield the PCB trace is to run it inside the PCB, between two ground planes. This design is called a "strip line". The ground planes can be power planes and the strip line can for example use a VDD plane on one side and a GND plane on the other side.

In this application note, the term "ground plane" is used as a generic term for a plane that can be used with Micro Strips and Strip Lines. The terms "GND plane" for a negative power plane and "VDD plane" for a positive power plane are also used, and both terms qualify for use as a "ground plane".

Figure 1. PCB Trace Transmission Line Examples – Micro Strip (left) and Strip Line (right)



Clock and Data Paths

The ideal clock/data trace makes a straight line from the driver to the target input. The ground plane underneath the trace is wide and in one piece from the driver to the target input. The driver ground connects to the ground plane and the target input ground also connects to the ground plane. EMI and waveform distortion happens when deviated from this ideal situation.

Guideline #1: Termination Matching is Important to Minimize EMI

Transmission lines have a specific characteristic impedance. The most common value is 50Ω . It is important to terminate the transmission line with the characteristic impedance, at least on one of the two ends. This preserves signal integrity and avoids reflections oscillating up and down the transmission line or clock trace, designed as a transmission line in this case. A termination at the side of the clock driver is called a source termination and a termination at the receive side is called an end termination. The logic types used for the clock or data signals each have their specific methods for implementing the termination. When the termination is not a good match with the transmission line characteristic impedance, the resulting oscillating reflections in combination with an unbalance between trace current and return current, causes EMI.

Guideline #2: Do Not Interrupt the Ground Plane(s) Underneath and/or Above the Clock Trace

This can happen for example when we pass a miscellaneous trace through the ground plane layer and pass this trace underneath the clock trace. Another example is combining ground and power plane in the same layer and the clock trace changes from running over the GND plane to running over the VDD plane when these planes are in the same layer. The problem is that the ground plane interruption is a barrier for the return current. The return current will flow away from the clock trace to pass around the barrier and the two opposing currents will no longer cancel each other's field. The ground plane interruption essentially creates an antenna.

- Do not pass miscellaneous traces in ground plane layers. If this cannot be avoided, at least do not route these traces underneath or near clock traces.
- Use separate layers for ground and power and keep these layers as uninterrupted as possible.
- Make sure the ground plane(s) around the clock trace is a relatively wide area without obstructions to allow the return current to stay with the trace and not be 'pushed' away.

Guideline #3: Round the Corners

Obviously it is not always possible to route a clock or data trace in a straight line. When changing direction, do it gradually. The best way to change direction is to use an arc shape with a diameter as large as possible. Do not use straight (90°) angles. At least cut into two 135° angles or three 150° angles. A straight angle cannot maintain the intended characteristic impedance at the corner. The current in the trace will be forced to take the straight corner but the return current follows more of an arc path. This means that the two currents separate somewhat and radiate from the area of the straight corner.

Guideline #4: Try to Avoid Using Vias in a Clock or Data Trace

The situation is similar to the straight angle, where there is a local interruption of the characteristic impedance that causes EMI and signal integrity issues.

Differential Clock / Data Traces

A perfect differential clock trace does not need a ground plane. The return current for one of the traces in the differential pair will be the current in the other trace of the pair. Most designs will have ground planes anyway to distribute power (GND and VDD planes), causing the differential trace design to be a compromise between two 'independent' single ended traces and the perfect differential pair. It is essentially a 3-wire design. Part of the return currents will be in a ground plane. Because a ground plane is still involved, the above recommendations still apply.

Calculators

To perform additional modeling, the internet has ample calculators for Micro Strips and Strip Lines. Calculators for differential traces usually are 3-wire models that include a ground plane.

Power Supply

In a timing device there can be many signals toggling at any time, which can couple into the power pins of the device. A power filter is generally designed to prevent signals (ripple) in the power supply or power planes from interfering with the operation of the timing device. Another important function of a power filter is to prevent the timing device's signals from penetrating the power planes and interfering with other devices. Once signals get onto power planes, they will also emit.

The most likely power pins on a timing device to cause interference are power pins for the output driver circuitry. Output drivers need to boost clock or data signals to the required levels for the specific logic type. As a result output drivers generally have the highest currents in the timing device. The current in the VDD pin for an output driver tends to switch fast and this is what is causing the EMI.

Bypassing vs Decoupling

Bypassing is a technique for avoiding interference by “passing it by” a device that may be sensitive to the interference. The best example is a bypass capacitor on a power pin, passing possibly interfering currents to ground. A large value capacitor presents a low impedance to interference causing signals while not affecting the DC voltage or DC current at the power pin.

Decoupling is a technique for avoiding interference by stopping or blocking the interfering signal currents. The best example is a ferrite bead that presents a high impedance to interference causing signals while passing DC currents to a power pin. Often a combination of a ferrite bead and capacitor is used to both block and bypass the remaining interference.

The above definitions are from the undesired signal or interference point of view, and for consistency purposes, these definitions will be used for the following notes below.

Bypassing

Each power pin needs to have a bypass capacitor assembled as close as possible to the pin for shorting out the signals that try to cause EMI. There will essentially be a loop from the power pin, through the bypass capacitor and back to the timing device, through the ground plane. This loop will act as an antenna. It is very important to minimize the area of the loop (antenna) to minimize EMI. Therefore, the bypass capacitor needs to be as close as possible to the V_{DD} and V_{SS} (GND) pins of the timing device. [Figure 2](#) illustrates that C8 and C10 are the bypass capacitors most effective at preventing EMI.

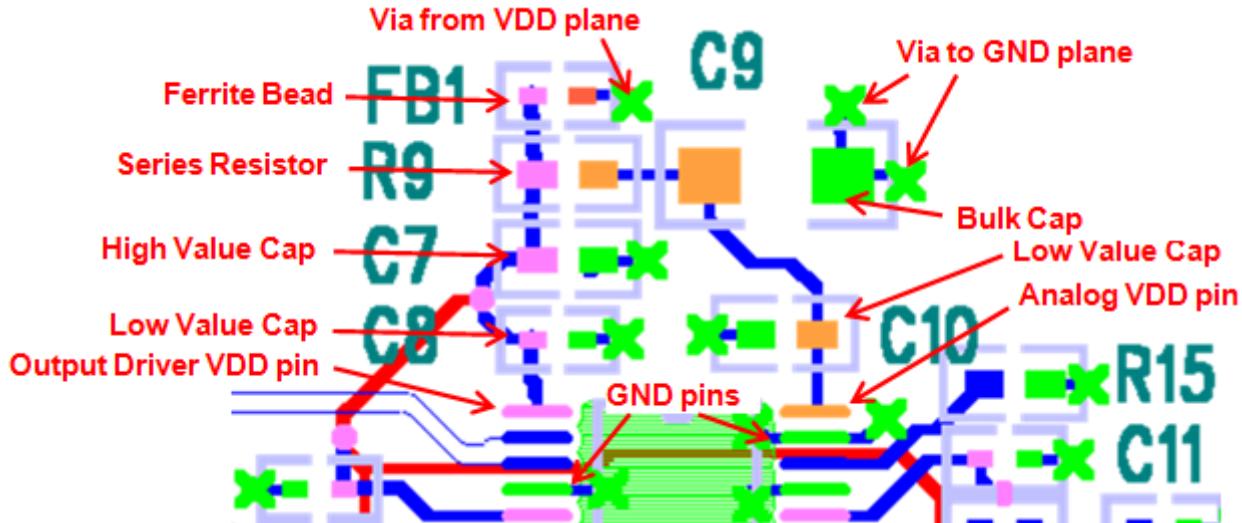
Bypass Capacitor Materials

Bypass capacitors can have different dielectric materials, each with strengths and weaknesses. Capacitors best suited for bypassing the highest frequencies use dielectrics that do not make large capacitance values. High frequencies have short wavelengths and can transmit EMI from small loop sizes. This is why the smallest value bypass capacitors usually are placed closest to the timing device power pins to make sure the highest frequencies are properly bypassed by presenting them with the smallest loop size. The NP0 dielectric material is best for bypassing high frequencies, followed by the X5R and X7R materials. X5R and X7R are good enough for the frequencies that need bypassing with timing devices, like frequencies up to the single digit GHz range. X7R can handle higher temperatures so it may be preferred for automotive applications.

Routing Recommendations

When using vias with bypass capacitors, design the vias with the lowest possible impedance. Go from the via from the power plane to the bypass capacitor and then to the power pin on the timing device. Do not place the via between the bypass capacitor and the power pin or the via will still see some of the signal from the power pin when between the capacitor and the pin.

Figure 2. Layout Example Showing Recommended Routing of Power Traces



The capacitors most effective at preventing EMI in this layout example are C8 and C10.

Decoupling

To decouple signals at the timing device power pin from the power plane (and vice versa), a ferrite bead can be used. A ferrite bead will pass DC currents and resist high frequencies. A ferrite bead essentially is a bad, lossy inductor. A ferrite bead will be mostly resistive at high frequencies and dissipate high frequency energy. The preferred ferrite bead type for IDT's timing products is a so called "signal bead". The relatively high DC resistance of the signal bead results in a low Q-factor and avoids resonances with bulk capacitors.

Selecting a Ferrite Bead

Ferrite beads are commonly specified with a certain impedance at 100MHz. We recommend at least 100Ω impedance at 100MHz. The higher the impedance, the better the decoupling. A higher impedance usually also means a higher DC resistance. We recommend a DC resistance in the range 0.3Ω to 0.5Ω. This is big enough to result in a low Q-factor and small enough to limit the DC voltage drop across the ferrite bead.

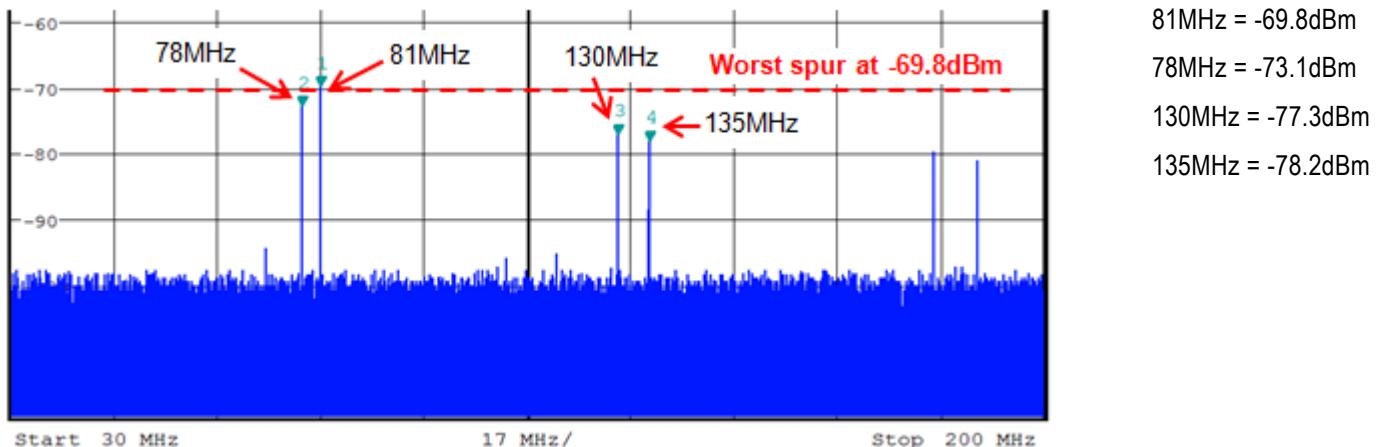
Also note the DC current capability of the ferrite bead. The problem is not so much power dissipation but rather saturation of the ferrite. When the DC current in the ferrite bead increases above its rating, the ferrite bead will lose its decoupling properties and starts passing signals.

IDT Timing Device Features for Lowering EMI

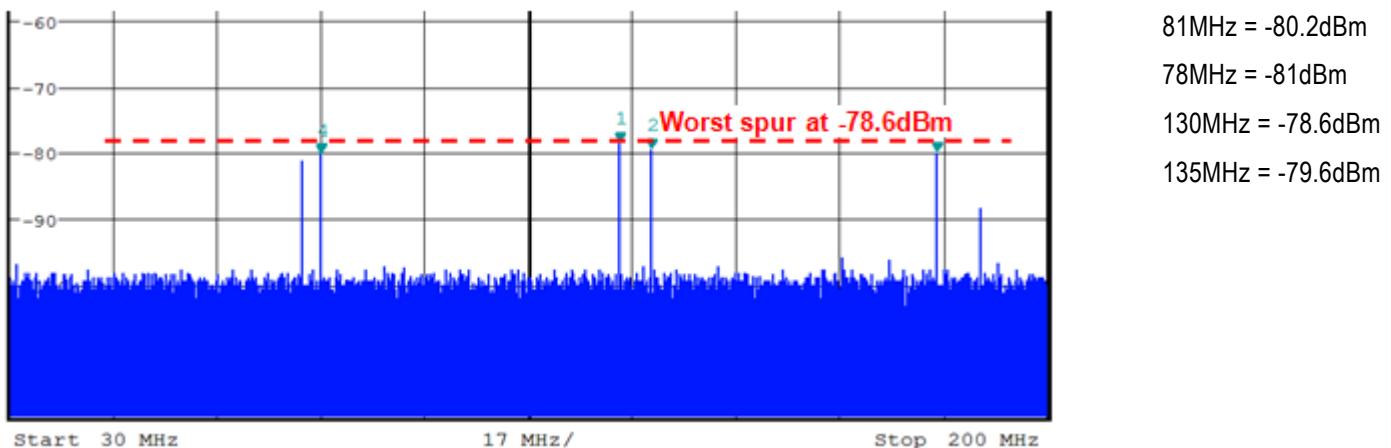
1. Spread Spectrum Modulation lowers spurs in the frequency spectrum by spreading the power of each spur. Spread Spectrum Modulation moves the clock frequency up and down with a small amount (e.g. 0.5%), with a triangular waveform and a low frequency or modulation rate, for example around 32kHz. The modulation also introduces jitter, so the amount of spreading needs to be chosen carefully.
2. A lot of timing devices have programmable features and the clock edge slew rate can be programmable. When EMI is an issue, then lowering the edge rate can help fix the issue. Lowering the edge rate can also increase overall noise (phase noise) so only reduce the edge rate enough to minimize the EMI issue and no lower.
3. IDT timing devices are staggering the edge rate at the start of each edge. The staggered wave itself lowers EMI but the staggering also softens reflections, causing extra EMI reduction.
4. IDT timing devices design V_{DD} and GND (V_{SS}) pins to be right next to each other, wherever possible. The bypass capacitor can be placed right next to the pins, creating the absolute minimum possible loop area for minimum EMI.

Appendix: EMI Issue Example

This example shows the radiation in the spectrum of 30MHz to 200MHz. The worst spur is 81MHz with a -69.8dBm level in our EMI chamber.



We discover that two clock outputs, 26MHz and 27MHz, do not match properly to the PCB trace. We improve the matching and try again.



The 78MHz and 81MHz spurs reduced significantly. Now the worst spur is 130MHz with -78.6dBm level. The improvement with fixing the matching on two clock outputs is 9dB.

Revision History

Table 1. Revision History

Revision Date	Description of Change
March 8, 2017	Corrected minor typos.
January 10, 2017	Major updates throughout document
December 20, 2016	Initial release.

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