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Application Note

78K0/Kx2-L

Sample Program (Low-Voltage Detection)

Reset Generation upon Detection of Voltage Less Than About 2.8 V

This document describes an operation overview of the sample program, as well as how to use the sample program and how to set up and use the low-voltage detector. In the sample program, the low-voltage detector is used to detect that V_{DD} is less than V_{LVI} (where V_{LVI} is 2.84 ±0.1 V), and then generate an internal reset (LVI reset). By generating an LVI reset, RAM data is retained and used to restore the LED lighting pattern immediately after the LVI reset ends to what it was immediately before the LVI reset.

Target devices

78K0/KY2-L microcontroller
78K0/KA2-L microcontroller
78K0/KB2-L microcontroller
78K0/KC2-L microcontroller

CONTENTS

Document No. U19696EJ1V0AN00 (1st edition)
Date Published September 2009 N

CHAPTER 1 OVERVIEW

In this sample program, an example of using the low-voltage detector is presented.

In the sample program, the low-voltage detector is specified to detect that V_{DD} is less than V_{LVI} (where V_{LVI} is 2.84 ±0.1 V), and then generate an internal reset (LVI reset).

After completion of the initial settings, an LED lighting pattern is displayed according to the number of switch inputs, by detecting the falling edge of the switch input and performing interrupt servicing.

When a reset is generated by other than LVI, the program is used to initialize the number of switch inputs. When an LVI reset is generated, the number of switch inputs immediately before reset generation is restored and an LED lighting pattern is displayed accordingly immediately after the LVI reset ends, because RAM retains the data immediately before the reset, unless it falls below the POC detection voltage (V_{PDR} = 1.59 ±0.09 V)[Note 1].

1.1 Primary Initial Settings

The primary initial settings are as follows:

<Option byte settings>

- Allowing the internal low-speed oscillator to be programmed to stop
- Disabling the watchdog timer
- Setting the internal high-speed oscillation clock frequency to 8 MHz
- Disabling LVI from being started by default

<Settings during initialization immediately after a reset ends>

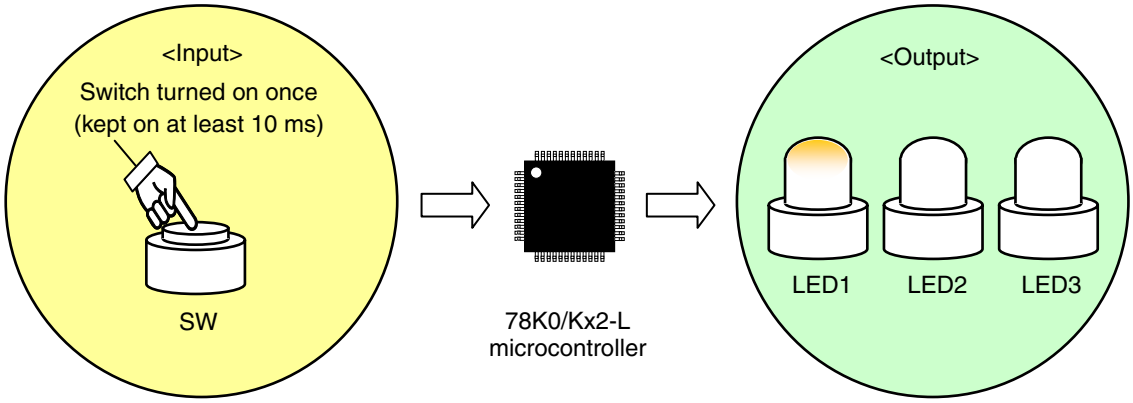
- Specifying the ROM and RAM sizes
- Setting up I/O ports
- Setting up the low-voltage detector[Note 2]
  - Setting the LVI detection voltage (V_{LVI}) to 2.84 ±0.1 V
  - Specifying that an internal reset is generated if the supply voltage (V_{DD}) is less than the LVI detection voltage (V_{LVI})
- Specifying that the CPU clock runs on the internal high-speed oscillation clock (8 MHz)
- Stopping the internal low-speed oscillator
- Disabling peripheral hardware not to be used
- Outputting the LED lighting pattern
- Setting up INTP1 interrupts (by using the falling edge)
- Enabling interrupts

Notes 1. For details about the POC detection voltage, refer to the chapter about the power-on-clear circuit in the 78K0/Kx2-L User's Manual.

2. Set up the low-voltage detector only if generating a reset other than an LVI reset.

1.2 Processing After Main Loop

Interrupt servicing is performed by detecting the falling edge of the INTP1 pin, caused by switch input. In interrupt servicing, the LED lighting pattern is changed by confirming that the switch is on, after about 10 ms have elapsed after the falling edge of the INTP1 pin was detected. If the switch is off, after about 10 ms have elapsed, processing is identified as chattering and the LED lighting pattern is not changed.



Number of Switch Inputs[Note]	LED Lighting Pattern		
	LED1	LED2	LED3
0	Off	Off	Off
1	On	Off	Off
2	Off	On	Off
3	On	On	Off
4	Off	Off	On
5	On	Off	On
6	Off	On	On
7	On	On	On

Note The lighting patterns from the zeroth switch input are repeated after the eighth switch input.

Caution For cautions when using the device, refer to the 78K0/Kx2-L User's Manual.

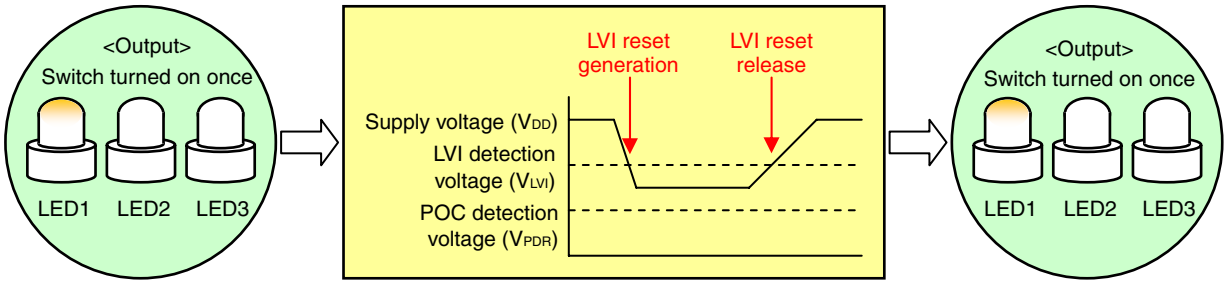
[Column] Chattering

Chattering is a phenomenon in which the electric signal repeats turning on and off due to a mechanical flip-flop of the contacts, immediately after the switch has been pressed.

1.3 Operation upon LVI Reset

In this sample program, an internal reset (LVI reset) is generated by the low-voltage detector when V_{DD} becomes less than V_{LVI}. At this time, RAM retains the data immediately before the reset, unless it falls below the POC detection voltage (V_{PDR} = 1.59 ±0.09 V)[Note 1]. The number of switch inputs immediately before the reset is retained until immediately after the reset ends and an LED lighting pattern can therefore be displayed accordingly when an LVI reset is generated[Note 2]. When a reset is generated by other than LVI, the program is used to initialize the number of switch inputs and all LEDs are turned off.

Figure 1-1. Overview of Operation upon LVI Reset



Notes 1. For details about the POC detection voltage, refer to the chapter about the power-on-clear circuit in the 78K0/Kx2-L User's Manual.

2. As mentioned in [Column] below, when a standard startup routine is used in a C language program, RAM data is initialized (cleared to 0) before the main function. To avoid this, a section of the standard startup routine is commented out in this C language version sample program, so that RAM data without initial values is not initialized.

[Column] Processing of the startup routine

A standard startup routine mainly performs the following processing.

- Stack pointer setting
- Hardware initialization (needed to be performed at an early stage)
- Initialization of variables to be used with a library
- Transferring from ROM to RAM the initial values of external variables with initial values, and sreg variables
- Assigning 0 to RAM of external variables without initial values, and sreg variables[Note]

Note This processing is commented out in the source file (cstart.asm) of the startup routine included in this C language version sample program.

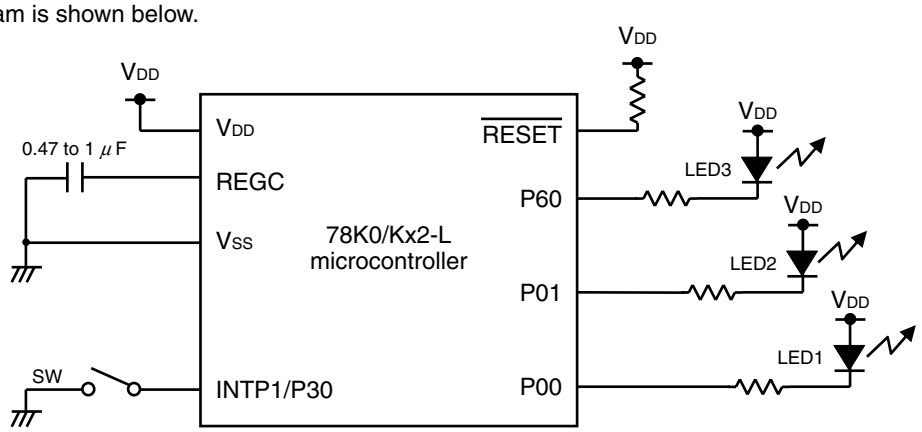
For details, refer to the chapter regarding the startup routine of the **CC78K0 C Compiler Operation User's Manual**.

CHAPTER 2 CIRCUIT DIAGRAM

This chapter provides a circuit diagram and describes the devices used in this sample program other than the microcontroller.

2.1 Circuit Diagram

A circuit diagram is shown below.



Cautions 1. Use V_{DD} in the following voltage range:

During normal operation: $2.94\ V < V_{DD} \leq 5.5\ V$

When generating an LVI reset: $1.68\ V < V_{DD} \leq 2.74\ V$

2. Connect the AV_{REF} pin directly to V_{DD}.

3. Connect the AV_{SS} pin directly to GND (only for the 78K0/KC2-L and 78K0/KB2-L microcontrollers).

4. Connect REGC to V_{SS} via a capacitor (0.47 to 1 μF).

5. For the 78K0/KY2-L and 78K0/KA2-L, V_{SS} is also used as the ground potential for the A/D converter. Be sure to connect V_{SS} to a stable GND.

6. Handle unused pins that are not shown in the circuit diagram as follows:

- **I/O ports: Set them to output mode and leave them open (unconnected).**
- **Input ports: Connect them independently to V_{DD} or V_{SS} via a resistor.**

7. In this sample program, the P121/X1/TOOLC0 and P122/X2/EXCLK/TOOLD0 pins are used for on-chip debugging.

2.2 Used Devices Other than Microcontroller

The following devices are used in addition to the microcontroller:

(1) Switch (SW)

A switch is used as an input to control the lighting of an LED.

(2) LEDs (LED1, LED2, LED3)

The LEDs are used as outputs corresponding to switch inputs.

CHAPTER 3 SOFTWARE

This chapter describes the files included in the compressed file to be downloaded, internal peripheral functions of the microcontroller to be used, and initial settings and provides an operation overview of the sample program and the flow charts.

3.1 Included Files

The following table shows the files included in the compressed file to be downloaded.

(1) Assembly language version

File Name	Description	Compressed (*.zip) File Included	
		ZIP	PM 32
main.asm	Source file for hardware initialization processing and main processing of microcontroller	●	●
op.asm	Assembler source file for setting the option byte (This file is used for setting up the watchdog timer and internal low-speed oscillator and selecting the internal high-speed oscillation clock frequency.)	●	●
Kx2-L_LVI.prw	Work space file for integrated development environment PM+		●
Kx2-L_LVI.prj	Project file for integrated development environment PM+		●

(2) C language version

File Name	Description	Compressed (*.zip) File Included	
		ZIP	PM 32
main.c	Source file for hardware initialization processing and main processing of microcontroller	●	●
op.asm	Assembler source file for setting the option byte (This file is used for setting up the watchdog timer and internal low-speed oscillator and selecting the internal high-speed oscillation clock frequency.)	●	●
cstart.asm	Startup routine source file (comments out a section of ROM processing)	●	●
def.inc	Library type setting file (include file of “cstart.asm”)	●	●
macro.inc	Macro definition file regarding various template patterns (include file of “cstart.asm”)	●	●
Kx2-L_LVI.prw	Work space file for integrated development environment PM+		●
Kx2-L_LVI.prj	Project file for integrated development environment PM+		●

Remark ZIP : Only the source files are included.

PM 32 : The files to be used with integrated development environment PM+ are included.

3.2 Internal Peripheral Functions to Be Used

The following internal peripheral functions of the microcontroller are used in this sample program.

- Low-voltage detector: Used to detect that V_{DD} is less than V_{LVI} and generate an LVI reset.
- INTP1: Used for switch input.
- P00, P01, and P60: Used to turn on or off three LEDs (LED1, LED2, and LED3).

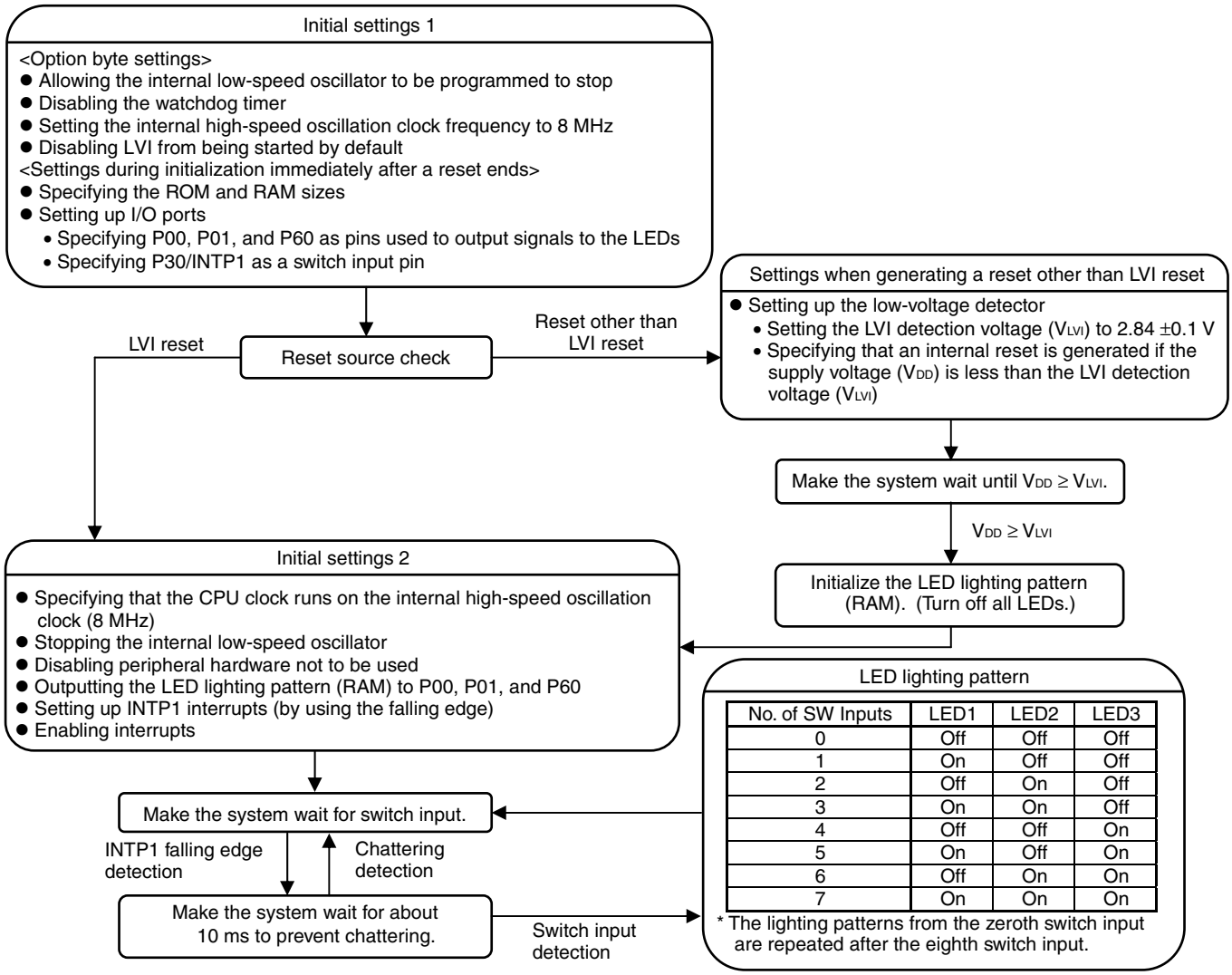
3.3 Initial Settings and Operation Overview

In this sample program, the selection of the clock frequency, setting of the I/O ports, setting of interrupt, and setting of the low-voltage detector are performed in the initial settings.

After completion of the initial settings, interrupt servicing is performed by detecting the falling edge of the switch input (SW) and the lighting of the three LEDs (LED1, LED2, and LED3) is controlled according to the number of switch inputs.

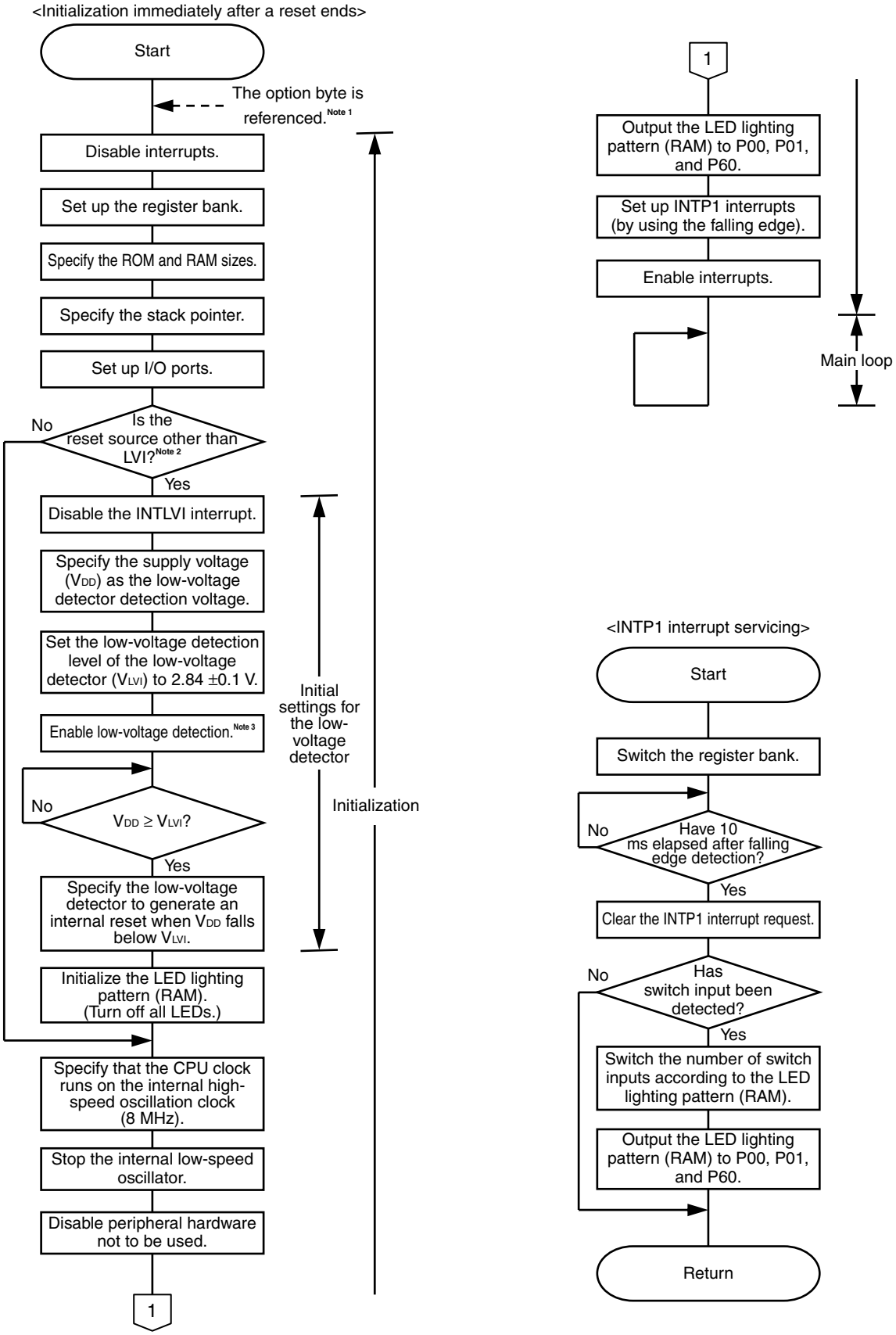
When a reset is generated by other than LVI, the program is used to initialize the number of switch inputs. When an LVI reset is generated, the number of switch inputs immediately before reset generation is restored and an LED lighting pattern is displayed accordingly immediately after the LVI reset ends, because RAM retains the data immediately before the reset, unless it falls below the POC detection voltage (V_{PDR} = 1.59 ±0.09 V).

The details are described in the state transition diagram shown below.



3.4 Flow Charts

The flow charts for the sample program are shown below.



Notes 1. The option byte is automatically referenced by the microcontroller immediately after a reset ends. In this sample program, the following settings are specified using the option byte:

- Allowing the internal low-speed oscillator to be programmed to stop
- Disabling the watchdog timer
- Setting the internal high-speed oscillation clock frequency to 8 MHz
- Disabling LVI from being started by default

2. Use the reset control flag register (RESF) to check the reset source. For details about RESF, refer to the chapter about the reset function in the 78K0/Kx2-L User's Manual.

3. The low-voltage detector is enabled, and then the system is made to wait at least 10 μs until the low-voltage detector stabilizes.

CHAPTER 4 SETTING METHODS

This chapter describes how to set up the low-voltage detector and the startup routine and provides a software coding example.

For other initial settings, refer to the 78K0/Kx2-L Sample Program (Initial Settings) LED Lighting Switch Control Application Note.

For how to set registers, refer to the 78K0/Kx2-L User's Manual.

For assembler instructions, refer to the 78K/0 Series Instructions User's Manual.

4.1 Setting up Low-Voltage Detector

The low-voltage detector is mainly controlled by the following two types of registers:

- Low-voltage detection register (LVIM)
- Low-voltage detection level select register (LVIS)

[Example of the setup procedure when using the low-voltage detector to generate a reset]

(The same procedure is used in the sample program.)

<1> Mask LVI interrupts (LVIMK = 1).

<2> Clear bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 0 (to detect the supply voltage (V_{DD}) level).

<3> Specify the LVI detection voltage by using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level select register (LVIS).

<4> Set bit 7 (LVION) of LVIM to 1 (to enable LVI).

<5> Program the system to wait for the operation stabilization time (about 10 μs).

<6> Make the system wait until the supply voltage (V_{DD}) is confirmed to be equal to or greater than the LVI detection voltage (V_{LVI}) by using bit 0 (LVIF) of LVIM.

<7> Set bit 1 (LVIMD) of LVIM to 1 (to generate a reset when the specified level is detected).

Cautions 1. This is the setup procedure when LVI is disabled to start by default (LVISTART = 0) by using the option byte.

2. Be sure to perform step <1>. If LVIMK is 0, an interrupt might be generated after step <4> is performed.

3. No internal reset signal is generated if the supply voltage (V_{DD}) is equal to or greater than the LVI detection voltage (V_{LVI}) when LVIMD has been set to 1.

(1) Low-voltage detection register (LVIM)

This register sets low-voltage detection and the operation mode.

Figure 4-1. Format of Low-Voltage Detection Register (LVIM)

LVION	0	0	0	0	LVISEL[Note 3]	LVIMD	LVIF

LVIF	Low-voltage detection flag
0	• LVISEL = 0: Supply voltage (V_{DD}) ≥ LVI detection voltage (V_{LVI}), or when LVI operation is disabled • LVISEL = 1: Input voltage from external input pin (EXLVI) ≥ LVI detection voltage (V_{EXLVI}), or when LVI operation is disabled
1	• LVISEL = 0: Supply voltage (V_{DD}) < LVI detection voltage (V_{LVI}) • LVISEL = 1: Input voltage from external input pin (EXLVI) < LVI detection voltage (V_{EXLVI})

LVIMD[Note 1]	Low-voltage detection operation mode (interrupt/reset) selection
0	• LVISEL = 0: Generates an internal interrupt signal when the supply voltage (V_{DD}) drops lower than the LVI detection voltage (V_{LVI}) (V_{DD} < V_{LVI}) or when V_{DD} becomes V_{LVI} or higher (V_{DD} ≥ V_{LVI}). • LVISEL = 1: Generates an interrupt signal when the input voltage from an external input pin (EXLVI) drops lower than the LVI detection voltage (V_{EXLVI}) (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}).
1	• LVISEL = 0: Generates an internal reset signal when the supply voltage (V_{DD}) < the LVI detection voltage (V_{LVI}) and releases the reset signal when V_{DD} ≥ V_{LVI}. • LVISEL = 1: Generates an internal reset signal when the input voltage from an external input pin (EXLVI) < the LVI detection voltage (V_{EXLVI}) and releases the reset signal when EXLVI ≥ V_{EXLVI}.

LVISEL[Notes 1, 3]	Voltage detection selection
0	Detects level of supply voltage (V_{DD})
1	Detects level of input voltage from external input pin (EXLVI)

LVION[Notes 1, 2]	Enables low-voltage detection operation
0	Disables operation
1	Enables operation

Notes 1. LVION, LVIMD, and LVISEL are cleared to 0 in the case of a reset other than an LVI reset. These are not cleared to 0 in the case of an LVI reset.

2. When LVION is set to 1, operation of the comparator in the LVI circuit is started. Use software to wait for an operation stabilization time (10 μs (MAX.)) from when LVION is set to 1 until operation is stabilized. After the operation stabilizes, an external input (minimum pulse width: 200 μs) of 200 μs or more is required until LVIF is set (1) after the voltage drops to the LVI detection voltage or less.

3. 78K0/KB2-L and 78K0/KC2-L only.

Cautions 1. To stop LVI, follow either of the procedures below.

- **When using 8-bit memory manipulation instruction: Write 00H to LVIM.**
- **When using 1-bit memory manipulation instruction: Clear LVION to 0.**

2. Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.

3. If LVI operation is disabled (clears LVION) when LVI is used in interrupt mode (LVIMD = 0), LVISEL is set to 0, and the supply voltage (V_{DD}) is less than or equal to the detection voltage (V_{LVI}), or when LVI is used in interrupt mode (LVIMD = 0), LVISEL is set to 1, and input voltage of external input pin (EXLVI) is less than or equal to the detection voltage (V_{EXLVI})), an interrupt request signal (INTLVI) is generated and LVIIF may be set to 1.

4. Be sure to clear the following bits to 0:

- **78K0/KY2-L, 78K0/KA2-L: Bits 6 to 2**
- **78K0/KB2-L, 78K0/KC2-L: Bits 6 to 3**

5. The LVIM reset value varies depending on the reset source and option byte setting and is as follows:

- **For an LVI reset: The value specified before the reset is retained.**
- **For a reset other than an LVI reset:**
  - **(a) If the LVISTART option byte is 1: 82H**
  - **(b) If the LVISTART option byte is 0: 00H**

6. Bit 0 is read-only.

Remark The values written in red in the above figure are specified in this sample program.

(2) Low-voltage detection level select register (LVIS)

This register selects the low-voltage detection level.

Figure 4-2. Format of Low-Voltage Detection Level Select Register (LVIS)

0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0

LVIS3	LVIS2	LVIS1	LVIS0	Detection level
0	0	0	0	V_{LVI0} (4.22 ±0.1 V)[Note]
0	0	0	1	V_{LVI1} (4.07 ±0.1 V)[Note]
0	0	1	0	V_{LVI2} (3.92 ±0.1 V)[Note]
0	0	1	1	V_{LVI3} (3.76 ±0.1 V)[Note]
0	1	0	0	V_{LVI4} (3.61 ±0.1 V)[Note]
0	1	0	1	V_{LVI5} (3.45 ±0.1 V)[Note]
0	1	1	0	V_{LVI6} (3.30 ±0.1 V)[Note]
0	1	1	1	V_{LVI7} (3.15 ±0.1 V)[Note]
1	0	0	0	V_{LVI8} (2.99 ±0.1 V)[Note]
1	**0**	**0**	**1**	V_{LVI9} (2.84 ±0.1 V)[Note]
1	0	1	0	V_{LVI10} (2.68 ±0.1 V)[Note]
1	0	1	1	V_{LVI11} (2.53 ±0.1 V)[Note]
1	1	0	0	V_{LVI12} (2.38 ±0.1 V)[Note]
1	1	0	1	V_{LVI13} (2.22 ±0.1 V)[Note]
1	1	1	0	V_{LVI14} (2.07 ±0.07 V)[Note]
1	1	1	1	V_{LVI15} (1.91 ±0.1 V)[Note]

Note These are preliminary values and subject to change.

Cautions 1. Be sure to clear bits 7 to 4 to "0".

2. Do not change the value of LVIS during LVI operation.

3. When an input voltage from the external input pin (EXLVI) is detected, the LVI detection voltage (V_{EXLVI} = 1.21 V (TYP.)) is fixed. Therefore, setting of LVIS is not necessary.

4. The LVIS reset value varies depending on the reset source and option byte setting and is as follows:

- **For an LVI reset: The value specified before the reset is retained.**
- **For a reset other than an LVI reset:**
  - **(a) If the LVISTART option byte is 1: 0FH**
  - **(b) If the LVISTART option byte is 0: 00H**

Remark The values written in red in the above figure are specified in this sample program.

4.2 Software Coding Example

The settings to be specified for the low-voltage detector in the 78K0/KC2-L sample program are shown below as a software coding example.

(1) Assembly language

```
XMAIN  CSEG   UNIT
RESET_START:
···(Omitted)···
        SET1   LVIMK                ; Disable the INTVLI interrupt
        MOV    LVIM,  #00000000B    ; Low-voltage detection register
···(Omitted)···
        MOV    LVIS,  #00001001B    ; Low-voltage detection level select register
···(Omitted)···
        SET1   LVION                ; Enable low-voltage detection

        ; Make the system wait until the low-voltage detector stabilizes (10 us
or more)
        MOV    B,     #5            ; Specify the count value
HRES100:
        NOP
        DBNZ   B,     $HRES100      ; Has the operation stabilization wait time
elapsed? No,

        ; Make the system wait until VDD becomes equal to or greater than VLVI
HRES110:
        NOP
        BT     LVIF,  $HRES110      ; Has VDD become equal to or greater than VLVI?
No,

        SET1   LVIMD                ; Specify an internal reset to be generated
when VDD falls below VLVI
```

Mask LVI interrupts.

Specify the supply voltage (V_{DD}) as the detection voltage.

Set the LVI detection voltage to 2.84 ±0.1 V.

Enable low-voltage detection.

The system waits at least 10 μs.

The system waits until $V_{DD} \geq V_{LVI}$.

Specify a reset to be generated when $V_{DD} < V_{LVI}$.

(2) C language

```
void hdwinit(void)
{
 ···(Omitted)···
        LVIMK  = 1;    /* Disable the INTVLI interrupt */
        LVIM   = 0b00000000; /* Low-voltage detection register */
 ···(Omitted)···
        LVIS   = 0b00001001; /* Low-voltage detection level select register */
 ···(Omitted)···
        LVION  = 1;    /* Enable low-voltage detection */

        /* Make the system wait until the low-voltage detector stabilizes (10 us
or more) */
        for ( ucCounter = 0; ucCounter < 2; ucCounter++){
                NOP();
        }

        /* Make the system wait until VDD becomes equal to or greater than VLVI
*/
        while( LVIF ){
                NOP();
        }

        LVIMD = 1;     /* Specify an internal reset to be generated when VDD falls
below VLVI */
```

Mask LVI interrupts.

Specify the supply voltage (V_{DD}) as the detection voltage.

Set the LVI detection voltage to 2.84 ±0.1 V.

Enable low-voltage detection.

The system waits at least 10 μs.

The system waits until $V_{DD} \geq V_{LVI}$.

Specify a reset to be generated when $V_{DD} < V_{LVI}$.

Remark In this sample program, f_{CPU} (the CPU clock frequency) is 4 MHz when the low-voltage detector is set up. Therefore, the wait time above (10 μs) is calculated based on f_{CPU} being 4 MHz.

4.3 Setting up Startup Routine

In the C language version of this sample program, a startup routine defined for this sample program is used instead of a standard startup routine. To use a user-defined startup routine, that startup routine must be set up using PM+.

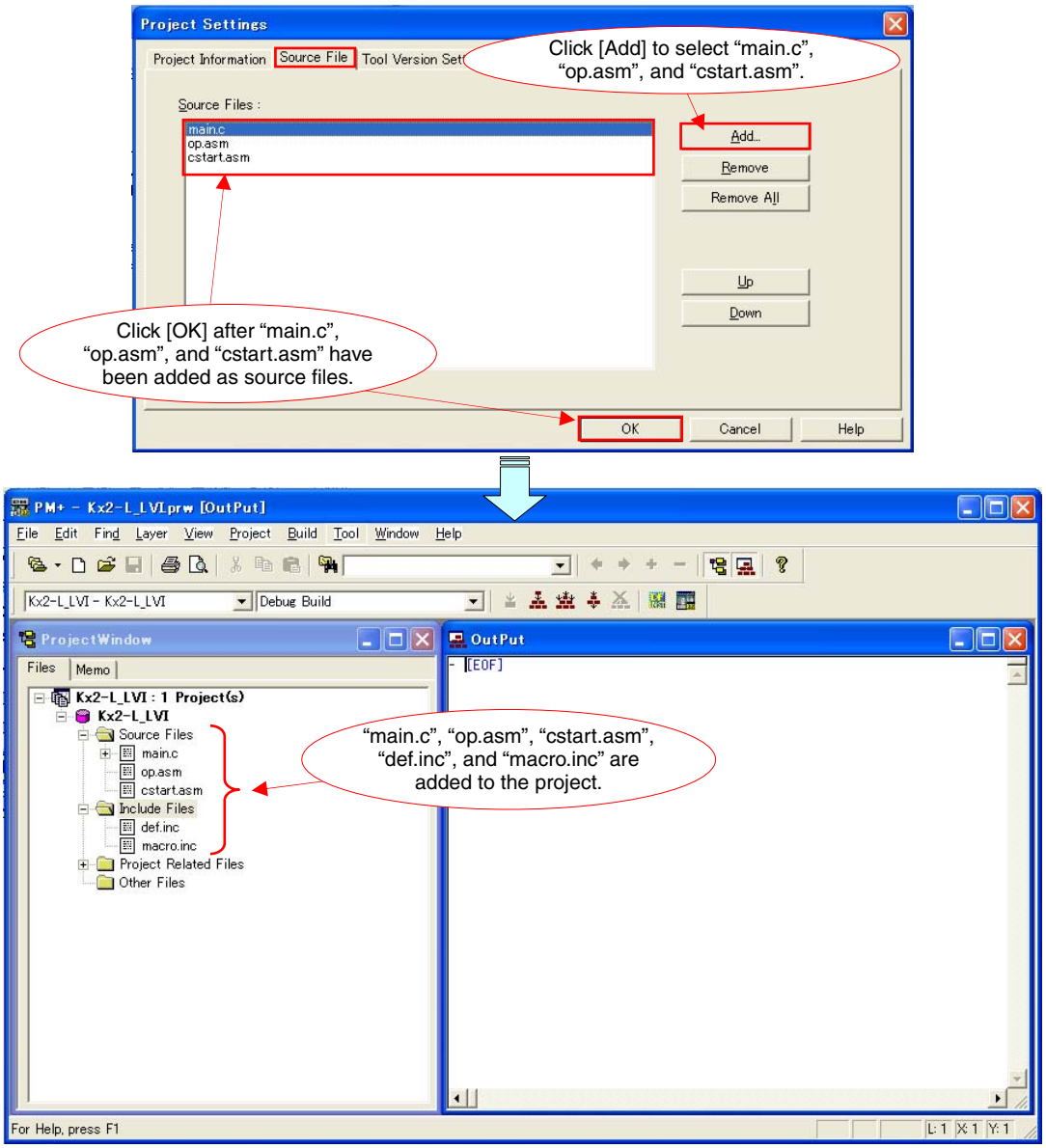
How to set up the startup routine used in the C language version of this sample program is described below.

For details about how to use PM+, refer to the PM+ Project Manager User's Manual. For details about startup routines, refer to the chapter about startup routines in the CC78K0 C Compiler Operation User's Manual.

(1) Setting up source files

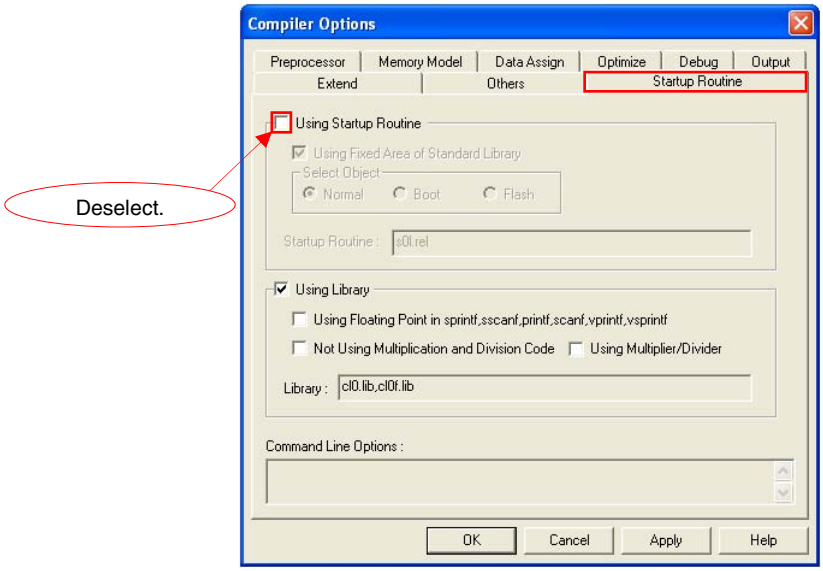
In the C language version of this sample program, the startup routine source file "cstart.asm", library type specification file "def.inc", and macro definition file "macro.inc" are used in addition to "main.c" and "op.asm".

Open the [Project] menu in PM+ and select [Project Settings]. The Project Settings dialog box opens. In this dialog box, select "main.c", "op.asm", and "cstart.asm" as the source files.



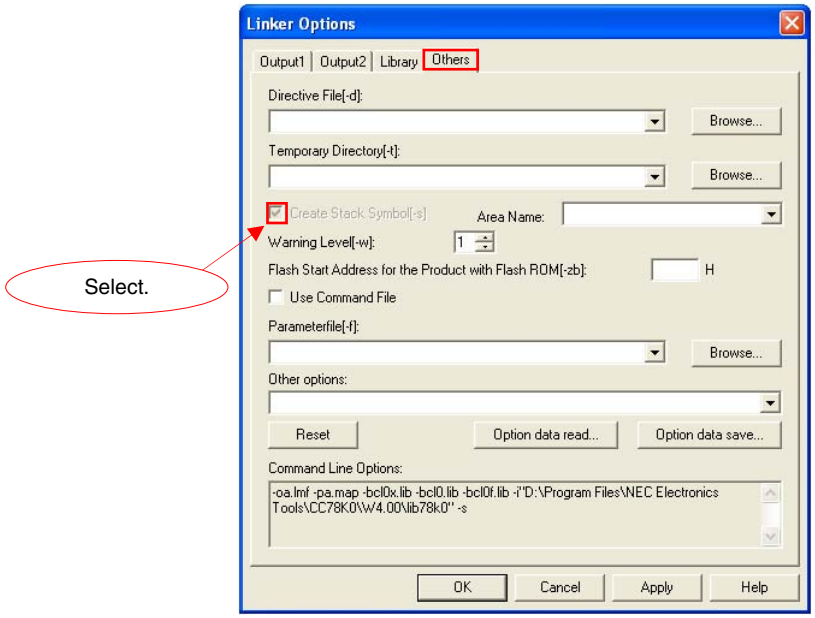
(2) Specifying compiler options

Open the [Tool] menu in PM+ and select [Compiler Options]. The Compiler Options dialog box opens. In this dialog box, deselect the [Using Startup Routine] checkbox.



(3) Specifying linker options

Open the [Tool] menu in PM+ and select [Linker Options]. The Linker Options dialog box opens. In this dialog box, select the [Create Stack Symbol [-s]] checkbox.



CHAPTER 5 RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name			English
78K0/Kx2-L User's Manual			PDF
78K/0 Series Instructions User's Manual			PDF
RA78K0 Assembler Package User's Manual		Language	PDF
		Operation	PDF
CC78K0 C Compiler User's Manual		Language	PDF
		Operation	PDF
PM+ Project Manager User's Manual			PDF
78K0/Kx2-L Application Note	Sample Program (Initial Settings) LED Lighting Switch Control		PDF

APPENDIX A PROGRAM LIST

As a program list example, the 78K0/KC2-L microcontroller source program is shown below.

● main.asm (assembly language version)

```
;*****************************************************************************
;
;    NEC Electronics     78K0/KC2-L Series
;
;*****************************************************************************
;    78K0/KC2-L Series   Sample Program (Low-Voltage Detection)
;*****************************************************************************
;    Reset Generation upon Detection of Voltage Less Than About 2.8 V
;*****************************************************************************
;<<History>>
;    2009.1.--    Release
;*****************************************************************************
;
;<<Overview>>
;
; This sample program presents an example of using the low-voltage detector.
; In the sample program, the low-voltage detector is specified to detect that VDD is
; less than VLVI (where VLVI is 2.84 ±0.1 V), and then generate an internal reset
; (LVI reset).  After completion of the initial settings, an LED lighting pattern is
; displayed according to the number of switch inputs, by detecting the falling edge
; of the switch input and performing interrupt servicing.  When a reset is generated
; by other than LVI, the program is used to initialize the number of switch inputs.
; When an LVI reset is generated, the number of switch inputs immediately before
; reset generation is restored and an LED lighting pattern is displayed accordingly
; immediately after the LVI reset ends, because RAM retains the data immediately
; before the reset, unless it falls below the POC detection voltage (VPDR = 1.59
; ±0.09 V).
;
;
; <Primary initial settings>
; (Option byte settings)
; - Allowing the internal low-speed oscillator to be programmed to stop
; - Disabling the watchdog timer
; - Setting the internal high-speed oscillation clock frequency to 8 MHz
; - Disabling LVI from being started by default
; (Settings during initialization immediately after a reset ends)
; - Specifying the ROM and RAM sizes
; - Setting up I/O ports
; - Setting up the low-voltage detector
;   → Setting the LVI detection voltage (VLVI) to 2.84 ±0.1 V
;   → Specifying that an internal reset is generated if the supply voltage (VDD) is
less than the LVI detection voltage (VLVI)
```

```
; - Specifying that the CPU clock runs on the internal high-speed oscillation clock
(8 MHz)
; - Stopping the internal low-speed oscillator
; - Disabling peripheral hardware not to be used
; - Outputting the LED lighting pattern
; - Setting up INTP1 interrupts (by using the falling edge)
; - Enabling interrupts
;
;
; <LED lighting pattern immediately after the reset ends>
;
; - Reset generated by other than the low-voltage detector:      Turn off all LEDs
; - Reset generated by the low-voltage detector:                 Retain    the    LED
lighting pattern before the reset
;
;
; <Number of switch inputs and LED lighting patterns>
;
; +---------------------------------------+
; | SW Inputs      | LED1  | LED2  | LED3  |
; | (P30/INTP1)    | (P00) | (P01) | (P60) |
; |----------------|-----------------------|
; | 0 times        | Off   | Off   | Off   |
; | 1 time         | On    | Off   | Off   |
; | 2 times        | Off   | On    | Off   |
; | 3 times        | On    | On    | Off   |
; | 4 times        | Off   | Off   | On    |
; | 5 times        | On    | Off   | On    |
; | 6 times        | Off   | On    | On    |
; | 7 times        | On    | On    | On    |
; +---------------------------------------+
; * The lighting patterns from the zeroth switch input are repeated after the eighth
switch input.
; * If the switch is turned on, 0 is input to the ports.  If the switch is turned off,
1 is input to the ports.
; * The LEDs turn off if 1 is output from the ports and turn on if 0 is output from
the ports.
;
;
; <I/O port settings>
;  Output: P00, P01, P60
;  Input:  P30
;  * Set all unused ports that can be specified as output ports as output ports.
;
;*****************************************************************************


;=============================================================================
```

```
;
;    Vector table
;
;==============================================================================
XVECT1            CSEG   AT     0000H
     DW     RESET_START         ;0000H RESET input, POC, LVI, WDT
XVECT2            CSEG   AT     0004H
     DW     IINIT               ;0004H INTLVI
     DW     IINIT               ;0006H INTP0
     DW     IINT_P1             ;0008H INTP1
     DW     IINIT               ;000AH INTP2
     DW     IINIT               ;000CH INTP3
     DW     IINIT               ;000EH INTP4
     DW     IINIT               ;0010H INTP5
     DW     IINIT               ;0012H INTSRE6
     DW     IINIT               ;0014H INTSR6
     DW     IINIT               ;0016H INTST6
     DW     IINIT               ;0018H INTCSI10
     DW     IINIT               ;001AH INTTMH1
     DW     IINIT               ;001CH INTTMH0
     DW     IINIT               ;001EH INTTM50
     DW     IINIT               ;0020H INTTM000
     DW     IINIT               ;0022H INTTM010
     DW     IINIT               ;0024H INTAD
     DW     IINIT               ;0026H INTP6
     DW     IINIT               ;0028H INTRTCI
     DW     IINIT               ;002AH INTTM51
     DW     IINIT               ;002CH INTKR
     DW     IINIT               ;002EH INTRTC
     DW     IINIT               ;0030H INTP7
     DW     IINIT               ;0032H INTP8
     DW     IINIT               ;0034H INTIICA0
     DW     IINIT               ;0036H INTCSI11
     DW     IINIT               ;0038H INTP9
     DW     IINIT               ;003AH INTP10
     DW     IINIT               ;003CH INTP11
     DW     IINIT               ;003EH BRK

;==============================================================================
;
;    Define the RAM data table
;
;==============================================================================
DLED DSEG   SADDR
RLEDBUF:    DS     1            ; Area in which to save the LED lighting pattern


;==============================================================================
```

```
;
;    Define the memory stack area
;
;==============================================================================
DSTK DSEG   IHRAM
STACKEND:
            DS     20H          ; Memory stack area = 32 bytes
STACKTOP:                       ; Start address of the memory stack area


;******************************************************************************
;
;    Servicing interrupts by using unnecessary interrupt sources
;
;******************************************************************************
XMAIN       CSEG   UNIT
IINIT:
;    If an unnecessary interrupt occurred, the processing branches to this line.
;    The processing then returns to the initial original processing because no
processing is performed here.

     RETI

;******************************************************************************
;
;    Initialization after RESET
;
;******************************************************************************
RESET_START:

;------------------------------------------------------------------------------
;    Disable interrupts
;------------------------------------------------------------------------------
     DI                         ; Disable interrupts

;------------------------------------------------------------------------------
;    Set up the register bank
;------------------------------------------------------------------------------
     SEL    RB0                 ; Set up the register bank

;------------------------------------------------------------------------------
;    Specify the ROM and RAM sizes
;------------------------------------------------------------------------------
;    Note that the values to specify vary depending on the model.
;    Enable the settings for the model to use. (The uPD78F0588 is the default model.)
;------------------------------------------------------------------------------
     ; Setting when using uPD78F0581 or uPD78F0586
     ;MOV   IMS,   #042H        ; Specify the ROM and RAM sizes
```

```
      ; Setting when using uPD78F0582 or uPD78F0587
      ;MOV   IMS,   #004H        ; Specify the ROM and RAM sizes

      ; Setting when using uPD78F0583 or uPD78F0588
      MOV    IMS,   #0C8H        ; Specify the ROM and RAM sizes

;-------------------------------------------------------------------------------
;    Initialize the stack pointer
;-------------------------------------------------------------------------------
      MOVW   SP,    #STACKTOP    ; Initialize the stack pointer

;-------------------------------------------------------------------------------
;    Initialize port 0
;-------------------------------------------------------------------------------
      MOV    P0,    #00000011B   ; Set the P00 and P01 output latches to high level
                                  ; Set the P02 output latch to low level
      MOV    PM0,   #11111000B   ; Specify P00 to P02 as output ports
                                  ; P00: Use to output a signal to LED1
                                  ; P01: Use to output a signal to LED2
                                  ; P02: Unused

;-------------------------------------------------------------------------------
;    Initialize port 1
;-------------------------------------------------------------------------------
      MOV    ADPC1, #00000111B   ; Specify P10 to P12 as digital I/O ports
      MOV    P1,    #00000000B   ; Set the P10 to P17 output latches to low level
      MOV    PM1,   #00000000B   ; Specify P10 to P17 as output ports
                                  ; P10 to P17: Unused

;-------------------------------------------------------------------------------
;    Initialize port 2
;-------------------------------------------------------------------------------
      MOV    ADPC0, #11111111B   ; Specify P20 to P27 as digital I/O ports
      MOV    P2,    #00000000B   ; Set the P20 to P27 output latches to low level
      MOV    PM2,   #00000000B   ; Specify P20 to P27 as output ports
                                  ; P20 to P27: Unused

;-------------------------------------------------------------------------------
;    Initialize port 3
;-------------------------------------------------------------------------------
      MOV    P3,    #00000000B   ; Set the P30 to P33 output latches to low level
      MOV    PM3,   #11110001B   ; Specify P30 as an input port
                                  ; Specify P31 to P33 as output ports
      MOV    PU3,   #00000001B   ; Connect an internal pull-up resistor to P30
                                  ; Do not connect internal pull-up resistors to P31 to
P33
                                  ; P30: Use as a switch input pin (INTP1)
```

```
                                ; P31 to P33: Unused

;-----------------------------------------------------------------------------
;    Initialize port 4
;-----------------------------------------------------------------------------
     MOV    P4,    #00000000B   ; Set the P40 to P42 output latches to low level
     MOV    PM4,   #11111000B   ; Specify P40 to P42 as output ports
                                ; P40 to P42: Unused

;-----------------------------------------------------------------------------
;    Initialize port 6
;-----------------------------------------------------------------------------
     MOV    P6,    #00000001B   ; Set the P60 output latch to high level
                                ; Set the P61 to P63 output latches to low level
     MOV    PM6,   #11110000B   ; Specify P60 to P63 as output ports
                                ; P60: Use to output a signal to LED3
                                ; P61 to P63: Unused

;-----------------------------------------------------------------------------
;    Initialize port 7
;-----------------------------------------------------------------------------
     MOV    P7,    #00000000B   ; Set the P70 to P75 output latches to low level
     MOV    PM7,   #11000000B   ; Specify P70 to P75 as output ports
                                ; P70 to P75: Unused

;-----------------------------------------------------------------------------
;    Initialize port 12
;-----------------------------------------------------------------------------
     MOV    P12,   #00000000B   ; Set the P120 output latch to low level
     MOV    PM12,  #11111110B   ; Specify P120 as an output port
                                ; P120 to P125: Unused

;-----------------------------------------------------------------------------
;    Set up the low-voltage detector
;-----------------------------------------------------------------------------
     ; Check the reset source (Omit this setting for a reset generated by the low-
voltage detector)
     MOV    A,     RESF         ; Read the reset source
     BT     A.0,   $HRES120     ;  Has  a  reset  been  generated  by  the  low-voltage
detector? Yes,

     ; Set up the low-voltage detector
     SET1   LVIMK               ; Disable the INTVLI interrupt
     MOV    LVIM,  #00000000B   ; Low-voltage detection register
;                  |||||||+------- LVIF
;                  |||||||        [Low-voltage detection flag]
;                  |||||||         0: - LVISEL = 0: Supply voltage (VDD) >= LVI
;                  |||||||              detection voltage (VLVI), or when LVI
```

```
;                   |||||||             operation is disabled
;                   |||||||           - LVISEL = 1: Input voltage from external input
;                   |||||||              pin (EXLVI) >= LVI detection voltage
;                   |||||||             (VEXLVI), or when LVI operation is disabled
;                   |||||||        1: - LVISEL = 0: Supply voltage (VDD) < LVI
;                   |||||||             detection voltage (VLVI)
;                   |||||||           - LVISEL = 1: Input voltage from external input
;                   |||||||             pin (EXLVI) < LVI detection voltage (VEXLVI)
;                   ||||||+-------- LVIMD
;                   ||||||        [Low-voltage      detection      operation      mode
(interrupt/reset) selection]
;                   ||||||         0: - LVISEL = 0: Generate an internal interrupt
;                   ||||||              signal when the supply voltage (VDD) drops
;                   ||||||              lower than the LVI detection voltage (VLVI)
;                   ||||||              (VDD < VLVI) or when VDD becomes VLVI or
;                   ||||||              higher (VDD >= VLVI)
;                   ||||||            - LVISEL = 1: Generate an interrupt signal when
;                   ||||||              the input voltage from an external input pin
;                   ||||||              (EXLVI) drops lower than the LVI detection
;                   ||||||              voltage (VEXLVI) (EXLVI < VEXLVI) or when
;                   ||||||              EXLVI becomes VEXLVI or higher (EXLVI >=
;                   ||||||              VEXLVI)
;                   ||||||         1: - LVISEL = 0: Generate an internal reset signal
;                   ||||||              when the supply voltage (VDD) < the LVI
;                   ||||||              detection voltage (VLVI) and releases the
;                   ||||||              reset signal when VDD >= VLVI
;                   ||||||            - LVISEL = 1: Generate an internal reset signal
;                   ||||||              when the input voltage from an external input
;                   ||||||              pin (EXLVI) < the LVI detection voltage
;                   ||||||              (VEXLVI) and releases the reset signal when
;                   ||||||              EXLVI >= VEXLVI
;                   |||||+--------- LVISEL
;                   |||||         [Voltage detection selection]
;                   |||||          0: Detect level of supply voltage (VDD)
;                   |||||          1: Detect level of input voltage from external
;                   |||||             input pin (EXLVI)
;                   |++++---------- Be sure to clear this bit to 0
;                   +-------------- LVION
;                                 [Enable low-voltage detection operation]
;                                  0: Disable operation
;                                  1: Enable operation

      MOV    LVIS,  #00001001B    ; Low-voltage detection level select register
;                   ||||++++------- LVIS3 to LVIS0
;                   ||||          0000: VLVI0 (4.22 ±0.1 V)
;                   ||||          0001: VLVI1 (4.07 ±0.1 V)
;                   ||||          0010: VLVI2 (3.92 ±0.1 V)
;                   ||||          0011: VLVI3 (3.76 ±0.1 V)
```

```
;                   ||||          0100: VLVI4 (3.61 ±0.1 V)
;                   ||||          0101: VLVI5 (3.45 ±0.1 V)
;                   ||||          0110: VLVI6 (3.30 ±0.1 V)
;                   ||||          0111: VLVI7 (3.15 ±0.1 V)
;                   ||||          1000: VLVI8 (2.99 ±0.1 V)
;                   ||||          1001: VLVI9 (2.84 ±0.1 V)
;                   ||||          1010: VLVI10 (2.68 ±0.1 V)
;                   ||||          1011: VLVI11 (2.53 ±0.1 V)
;                   ||||          1100: VLVI12 (2.38 ±0.1 V)
;                   ||||          1101: VLVI13 (2.22 ±0.1 V)
;                   ||||          1110: VLVI14 (2.07 ±0.1 V)
;                   ||||          1111: VLVI15 (1.91 ±0.1 V)
;                   ++++----------- Be sure to clear this bit to 0

      SET1   LVION               ; Enable low-voltage detection

      ; Make the system wait until the low-voltage detector stabilizes (10 us or more)
      MOV    B,     #5           ; Specify the count value
 HRES100:
      NOP
      DBNZ   B,     $HRES100     ; Has the operation stabilization wait time elapsed?
No,

      ; Make the system wait until VDD becomes equal to or greater than VLVI
 HRES110:
      NOP
      BT     LVIF,  $HRES110     ; Has VDD become equal to or greater than VLVI? No,

      SET1   LVIMD               ; Specify an internal reset to be generated when VDD
falls below VLVI
      MOV    RLEDBUF,#00000111B  ; Initialize the LED lighting pattern

 HRES120:
 ;-----------------------------------------------------------------------------
 ;    Specify the clock frequency
 ;-----------------------------------------------------------------------------
 ;    Specify the clock frequency so that the device can run on the internal high-
speed oscillation clock.
 ;-----------------------------------------------------------------------------
      MOV    OSCCTL,#00000000B   ; Clock operation mode
 ;                   ||||+||+------- Be sure to clear this bit to 0
 ;                   |||| ++-------- RSWOSC/AMPHXT
 ;                   ||||          [XT1 oscillator oscillation mode selection]
 ;                   ||||           00: Low power consumption oscillation
 ;                   ||||           01: Normal oscillation
 ;                   ||||           1x: Ultra-low power consumption oscillation
 ;                   ||++----------- EXCLKS/OSCSELS
 ;                   ||            [Subsystem clock pin operation setting]
```

```
  ;                   ||            (P123/XT1,P124/XT2/EXCLKS)
  ;                   ||             Specify the use of the pin as an I/O port pin by
specifying 000 by also using XTSTART
  ;                  ++------------- EXCLK/OSCSEL
  ;                                 [High-speed system clock pin operation setting]
  ;                                 (P121/X1,P122/X2/EXCLK)
  ;                                  00: Input port
  ;                                  01: X1 oscillation mode
  ;                                  10: Input port
  ;                                  11: External clock input mode

      MOV    PCC,   #00000000B   ; Select the CPU clock (fCPU)
  ;                  |||+|+++------- CSS/PCC2/PCC1/PCC0
  ;                  ||| |          [CPU clock (fCPU) selection]
  ;                  ||| |           0000:fXP
  ;                  ||| |           0001:fXP/2
  ;                  ||| |           0010:fXP/2^2
  ;                  ||| |           0011:fXP/2^3
  ;                  ||| |           0100:fXP/2^4
  ;                  ||| |           1000:fSUB/2
  ;                  ||| |           1001:fSUB/2
  ;                  ||| |           1010:fSUB/2
  ;                  ||| |           1011:fSUB/2
  ;                  ||| |           1100:fSUB/2
  ;                  ||| |           (Other than the above: Setting prohibited)
  ;                  ||| +---------- Be sure to clear this bit to 0
  ;                  ||+------------ CLS
  ;                  ||            [CPU clock status]
  ;                  |+------------- XTSTART
  ;                  |             [Subsystem clock pin operation setting]
  ;                  |              Specify the use of the pin by also using EXCLKS
and OSCSELS
  ;                  +-------------- Be sure to clear this bit to 0

      MOV    RCM,   #00000010B   ;  Select  the  operating  mode  of  the  internal
oscillator
  ;                  |||||||+------- RSTOP
  ;                  |||||||       [Internal high-speed oscillator oscillating/stopped]
  ;                  |||||||        0: Internal high-speed oscillator oscillating
  ;                  |||||||        1: Internal high-speed oscillator stopped
  ;                  ||||||+-------- LSRSTOP
  ;                  ||||||        [Internal low-speed oscillator oscillating/stopped]
  ;                  ||||||         0: Internal low-speed oscillator oscillating
  ;                  ||||||         1: Internal low-speed oscillator stopped
  ;                  |+++++--------- Be sure to clear this bit to 0
  ;                  +-------------- RSTS
  ;                                 [Status of internal high-speed oscillator]
```

```
      MOV    MOC,   #10000000B   ; Select the operating mode of the high-speed system
clock
  ;                  |+++++++------- Be sure to clear this bit to 0
  ;                  +-------------- MSTOP
  ;                                 [Control of high-speed system clock operation]
  ;                                  0: X1 oscillator operating/external clock from
  ;                                     EXCLK pin is enabled
  ;                                  1: X1 oscillator stopped/external clock from
  ;                                     EXCLK pin is disabled

      MOV    MCM,   #00000000B   ; Select the clock to supply
  ;                  |||||+|+------- XSEL/MCM0:
  ;                  ||||| |       [Clock supplied to main system and
  ;                  ||||| |        peripheral hardware]
  ;                  ||||| |        00: Main system clock (fXP)
  ;                  ||||| |             = internal high-speed oscillation clock (fIH)
  ;                  ||||| |            Peripheral hardware clock (fPRS)
  ;                  ||||| |             = internal high-speed oscillation clock (fIH)
  ;                  ||||| |        01: Main system clock (fXP)
  ;                  ||||| |             = internal high-speed oscillation clock (fIH)
  ;                  ||||| |            Peripheral hardware clock (fPRS)
  ;                  ||||| |             = internal high-speed oscillation clock (fIH)
  ;                  ||||| |        10: Main system clock (fXP)
  ;                  ||||| |             = internal high-speed oscillation clock (fIH)
  ;                  ||||| |            Peripheral hardware clock (fPRS)
  ;                  ||||| |             = high-speed system clock (fIH)
  ;                  ||||| |        11: Main system clock (fXP)
  ;                  ||||| |             = high-speed system clock (fIH)
  ;                  ||||| |            Peripheral hardware clock (fPRS)
  ;                  ||||| |             = high-speed system clock (fIH)
  ;                  ||||| +-------- MCS
  ;                  |||||         [Main system clock status]
  ;                  +++++---------- Be sure to clear this bit to 0

      MOV    PER0,  #00000000B   ; Control the real-time counter control clock
  ;                  |++++++------- Be sure to clear this bit to 0
  ;                  +-------------- RTCEN:
  ;                                 [Real-time counter control clock]
  ;                                  0: Stop supply of control clock
  ;                                  1: Supply control clock

  ;-------------------------------------------------------------------------------
  ;    Disable peripheral hardware not to be used
  ;-------------------------------------------------------------------------------
      ; 16-bit timer/event counter 00
      MOV    TMC00, #00000000B   ; Disable the counter

      ; 8-bit timer/event counters 50 and 51
```

```
    MOV    TMC50, #00000000B   ; Disable timer 50
    MOV    TMC51, #00000000B   ; Disable timer 51

    ; 8-bit timers H0 and H1
    MOV    TMHMD0,       #00000000B   ; Stop timer H0
    MOV    TMHMD1,       #00000000B   ; Stop timer H1

    ; Real-time counter
    MOV    RTCC0, #00000000B   ; Stop the counter

    ; Clock output controller
    MOV    CKS,   #00000000B   ; Stop the clock frequency divider

    ; A/D converter
    MOV    ADM0,  #00000000B   ; Stop A/D conversion

    ; Operational amplifiers
    MOV    AMP0M, #00000000B   ; Stop operational amplifier 0
    MOV    AMP1M, #00000000B   ; Stop operational amplifier 1

    ; Serial interface UART6
    MOV    ASIM6, #00000001B   ; Disable the interface

    ; Serial interface IICA
    MOV    IICACTL0,#00000000B ; Disable the interface

    ; Serial interfaces CSI10 and CSI11
    MOV    CSIM10,       #00000000B   ; Disable CSI10
    MOV    CSIM11,       #00000000B   ; Disable CSI11

    ; Interrupts (The interrupts to be used are enabled later)
    MOVW   MK0,   #0FFFFH      ; Disable all interrupts
    MOVW   MK1,   #0FFFFH      ;

    ; Key interrupts
    MOV    KRM,   #00000000B   ; Disable all key interrupts

;-------------------------------------------------------------------------------
;    Output the LED lighting pattern
;-------------------------------------------------------------------------------
    MOV    A,     RLEDBUF      ; Read the LED lighting pattern
    AND    A,     #00000011B   ; Mask unnecessary sections
    MOV    P0,    A            ; Control LED1 and LED2
    MOV1   CY,    RLEDBUF.2    ; Control LED3
    MOV1   P6.0,  CY           ;

;-------------------------------------------------------------------------------
;    Set up interrupts
```

```
;-------------------------------------------------------------------------------
     MOV    EGPCTL0,#00000000B  ; Disable the INTP1 rising edge
     MOV    EGNCTL0,#00000010B  ; Enable the INTP1 falling edge
     CLR1   PIF1                ; Clear the INTP1 interrupt request
     CLR1   PMK1                ; Enable the INTP1 interrupt

;-------------------------------------------------------------------------------
;    Enable interrupts
;-------------------------------------------------------------------------------
     EI                         ; Enable interrupts

     BR     MMAIN_LOOP          ; Go to the main loop


;*******************************************************************************
;
;    Main loop
;
;*******************************************************************************
MMAIN_LOOP:
     NOP                        ; Make the system wait for an interrupt to occur
     BR     $MMAIN_LOOP

;*******************************************************************************
;
;    INTP1 interrupt servicing (by using the INTP1 falling edge)
;
;*******************************************************************************
IINT_P1:
     SEL    RB1                 ; Switch the register bank

     ; Make the system wait for about 10 ms to prevent chattering
     MOVW   AX,    #0           ; Clear the count value
HINTP100:
     INCW   AX                  ; Count the elapsed time
     CMPW   AX,    #5000        ; Determine the elapsed time
     BC     $HINTP100           ; Has the wait period ended? No,
     CLR1   PIF1                ; Clear the INTP1 interrupt request

     BT     P3.0,  $HINTP800    ; Is there continued switch input? No,

     ; Turn on the LEDs
     DEC    RLEDBUF             ; Switch the LED lighting pattern
     AND    RLEDBUF,#00000111B  ; Mask unnecessary sections

     MOV    A,     RLEDBUF      ; Read the LED lighting pattern
     AND    A,     #00000011B   ; Mask unnecessary sections
     MOV    P0,    A            ; Control LED1 and LED2
```

```
     MOV1   CY,    RLEDBUF.2     ; Control LED3
     MOV1   P6.0,  CY            ;

HINTP800:
     RETI
end
```

● main.c (C language version)

```
/*****************************************************************************

  NEC Electronics     78K0/KC2-L Series

*****************************************************************************
  78K0/KC2-L Series   Sample Program (Low-Voltage Detection)
*****************************************************************************
  Reset Generation upon Detection of Voltage Less Than About 2.8 V
*****************************************************************************
<<History>>
  2009.1.-- Release
*****************************************************************************

<<Overview>>

This sample program presents an example of using the low-voltage detector.
In the sample program, the low-voltage detector is specified to detect that VDD is
less than VLVI (where VLVI is 2.84 ±0.1 V), and then generate an internal reset
(LVI reset).  After completion of the initial settings, an LED lighting pattern is
displayed according to the number of switch inputs, by detecting the falling edge
of the switch input and performing interrupt servicing.  When a reset is generated
by other than LVI, the program is used to initialize the number of switch inputs.
When an LVI reset is generated, the number of switch inputs immediately before
reset generation is restored and an LED lighting pattern is displayed accordingly
immediately after the LVI reset ends, because RAM retains the data immediately
before the reset, unless it falls below the POC detection voltage (VPDR = 1.59
±0.09 V).


  <Primary initial settings>
  (Option byte settings)
  - Allowing the internal low-speed oscillator to be programmed to stop
  - Disabling the watchdog timer
  - Setting the internal high-speed oscillation clock frequency to 8 MHz
  - Disabling LVI from being started by default
  (Settings during initialization immediately after a reset ends)
  - Specifying the ROM and RAM sizes
  - Setting up I/O ports
  - Setting up the low-voltage detector
    → Setting the LVI detection voltage (VLVI) to 2.84 ±0.1 V
    → Specifying that an internal reset is generated if the supply voltage (VDD) is
less than the LVI detection voltage (VLVI)
  - Specifying that the CPU clock runs on the internal high-speed oscillation clock (8
MHz)
  - Stopping the internal low-speed oscillator
  - Disabling peripheral hardware not to be used
  - Outputting the LED lighting pattern
```

```
   - Setting up INTP1 interrupts (by using the falling edge)
   - Enabling interrupts


   <LED lighting pattern immediately after the reset ends>

   - Reset generated by other than the low-voltage detector: Turn off all LEDs
   - Reset generated by the low-voltage detector:           Retain  the  LED  lighting
pattern before the reset


   <Number of switch inputs and LED lighting patterns>

   +-------------------------------------+
   | SW Inputs   | LED1  | LED2  | LED3  |
   | (P30/INTP1) | (P00) | (P01) | (P60) |
   |-------------|-----------------------|
   | 0 times     | Off   | Off   | Off   |
   | 1 time      | On    | Off   | Off   |
   | 2 times     | Off   | On    | Off   |
   | 3 times     | On    | On    | Off   |
   | 4 times     | Off   | Off   | On    |
   | 5 times     | On    | Off   | On    |
   | 6 times     | Off   | On    | On    |
   | 7 times     | On    | On    | On    |
   +-------------------------------------+
   * The lighting patterns from the zeroth switch input are repeated after the eighth
switch input.
   * If the switch is turned on, 0 is input to the ports.  If the switch is turned off,
1 is input to the ports.
   * The LEDs turn off if 1 is output from the ports and turn on if 0 is output from
the ports.


   <I/O port settings>
    Output: P00, P01, P60
    Input:  P30
    * Set all unused ports that can be specified as output ports as output ports.

  ****************************************************************************/


  /*==========================================================================

    Preprocessing directive (#pragma)

  ==========================================================================*/
  #pragma  SFR          /* SFR names can be described at the C source level   */
```

```
  #pragma DI            /* DI instructions can be described at the C source level */
  #pragma EI            /* EI instructions can be described at the C source level */
  #pragma NOP           /* NOP instructions can be described at the C source level */
  #pragma interrupt INTP1 fn_intp1 RB1   /* Declare the interrupt function: INTP1 */

  /*==============================================================================

    Define the RAM data table

  ==============================================================================*/
  sreg unsigned char ucLEDBuffer; /* Area in which to save the LED lighting pattern
(defined as an area in the internal high-speed RAM) */


  /******************************************************************************

    Initialization after RESET

  ******************************************************************************/
  void hdwinit( void )
  {
    unsigned char ucCounter;   /* Count variable */

  /*------------------------------------------------------------------------------
    Disable interrupts
  ------------------------------------------------------------------------------*/
    DI();                /* Disable interrupts */

  /*------------------------------------------------------------------------------
    Specify the ROM and RAM sizes
  ------------------------------------------------------------------------------
    Note that the values to specify vary depending on the model.
    Enable the settings for the model to use. (The uPD78F0588 is the default model.)
  ------------------------------------------------------------------------------*/
    /* Setting when using uPD78F0581 or uPD78F0586 */
    /*IMS =   0x42;*/          /* Specify the ROM and RAM sizes */

    /* Setting when using uPD78F0582 or uPD78F0587 */
    /*IMS =   0x04;*/          /* Specify the ROM and RAM sizes */

    /* Setting when using uPD78F0583 or uPD78F0588 */
    IMS =  0xC8;         /* Specify the ROM and RAM sizes */

  /*------------------------------------------------------------------------------
    Initialize port 0
  ------------------------------------------------------------------------------*/
    P0     = 0b00000011; /* Set the P00 and P01 output latches to high level */
                         /* Set the P02 output latch to low level */
```

```
  PM0    = 0b11111000; /* Specify P00 to P02 as output ports */
                       /* P00: Use to output a signal to LED1 */
                       /* P01: Use to output a signal to LED2 */
                       /* P02: Unused */

/*-----------------------------------------------------------------------------
  Initialize port 1
-----------------------------------------------------------------------------*/
  ADPC1  = 0b00000111; /* Specify P10 to P12 as digital I/O ports */
  P1     = 0b00000000; /* Set the P10 to P17 output latches to low level */
  PM1    = 0b00000000; /* Specify P10 to P17 as output ports */
                       /* P10 to P17: Unused */

/*-----------------------------------------------------------------------------
  Initialize port 2
-----------------------------------------------------------------------------*/
  ADPC0  = 0b11111111; /* Specify P20 to P27 as digital I/O ports */
  P2     = 0b00000000; /* Set the P20 to P27 output latches to low level */
  PM2    = 0b00000000; /* Specify P20 to P27 as output ports */
                       /* P20 to P27: Unused */

/*-----------------------------------------------------------------------------
  Initialize port 3
-----------------------------------------------------------------------------*/
  P3     = 0b00000000; /* Set the P30 output latch to low level */
  PM3    = 0b11110001; /* Specify P30 as an input port */
                       /* Specify P31 to P33 as output ports */
  PU3    = 0b00000001; /* Connect an internal pull-up resistor to P30 */
                       /* Do not connect internal pull-up resistors to P31 to P33 */
                       /* P30: Use as a switch input pin (INTP1) */
                       /* P31 to P33: Unused */

/*-----------------------------------------------------------------------------
  Initialize port 4
-----------------------------------------------------------------------------*/
  P4     = 0b00000000; /* Set the P40 to P42 output latches to low level */
  PM4    = 0b11111000; /* Specify P40 to P42 as output ports */
                       /* P40 to P42: Unused */

/*-----------------------------------------------------------------------------
  Initialize port 6
-----------------------------------------------------------------------------*/
  P6     = 0b00000001; /* Set the P60 output latch to high level */
                       /* Set the P61 to P63 output latches to low level */
  PM6    = 0b11110000; /* Specify P60 to P63 as output ports */
                       /* P60: Use to output a signal to LED3 */
                       /* P61 to P63: Unused */
```

```
  /*-----------------------------------------------------------------------------
    Initialize port 7
  -----------------------------------------------------------------------------*/
    P7     = 0b00000000; /* Set the P70 to P75 output latches to low level */
    PM7    = 0b11000000; /* Specify P70 to P75 as output ports */
                         /* P70 to P75: Unused */

  /*-----------------------------------------------------------------------------
    Initialize port 12
  -----------------------------------------------------------------------------*/
    P12    = 0b00000000; /* Set the P120 output latch to low level */
    PM12   = 0b11111110; /* Specify P120 as an output port */
                         /* P120 to P125: Unused */

  /*-----------------------------------------------------------------------------
    Set up the low-voltage detector
  -----------------------------------------------------------------------------*/
    /* Check the reset source (Omit this setting for a reset generated by the low-
voltage detector) */
    if (!(RESF & 0b00000001)){

        LVIMK  = 1;   /* Disable the INTVLI interrupt */
        LVIM   = 0b00000000; /* Low-voltage detection register */
        /*         |||||||+---- LVIF   */
        /*         |||||||     [Low-voltage detection flag] */
        /*         |||||||      0: - LVISEL = 0: Supply voltage (VDD) >= LVI detection */
        /*         |||||||           voltage (VLVI), or when LVI operation is disabled */
        /*         |||||||         - LVISEL = 1: Input voltage from external input pin */
        /*         |||||||           (EXLVI) >= LVI detection voltage (VEXLVI), or */
        /*         |||||||           when LVI operation is disabled */
        /*         |||||||      1: - LVISEL = 0: Supply voltage (VDD) < LVI detection */
        /*         |||||||           voltage (VLVI) */
        /*         |||||||         - LVISEL = 1: Input voltage from external input pin */
        /*         |||||||           (EXLVI) < LVI detection voltage (VEXLVI) */
        /*         ||||||+----- LVIMD  */
        /*         ||||||      [Low-voltage  detection  operation  mode  (interrupt/reset)
selection] */
        /*         ||||||       0: - LVISEL = 0: Generate an internal interrupt signal */
        /*         ||||||            when the supply voltage (VDD) drops lower than */
        /*         ||||||            the LVI detection voltage (VLVI) (VDD < VLVI) or */
        /*         ||||||            when VDD becomes VLVI or higher (VDD >= VLVI) */
        /*         ||||||          - LVISEL = 1: Generate an interrupt signal when the */
        /*         ||||||            input voltage from an external input pin (EXLVI) */
        /*         ||||||            drops lower than the LVI detection voltage */
        /*         ||||||            (VEXLVI) (EXLVI < VEXLVI) or when EXLVI becomes */
        /*         ||||||            VEXLVI or higher (EXLVI >= VEXLVI) */
        /*         ||||||       1: - LVISEL = 0: Generate an internal reset signal */
        /*         ||||||            when the supply voltage (VDD) < the LVI detection */
```

```
/*         ||||||            voltage (VLVI) and releases the reset signal when */
/*         ||||||            VDD >= VLVI */
/*         ||||||          - LVISEL = 1: Generate an internal reset signal */
/*         ||||||            when the input voltage from an external input pin */
/*         ||||||            (EXLVI) < the LVI detection voltage (VEXLVI) and */
/*         ||||||            releases the reset signal when EXLVI >= VEXLVI */
/*         |||||+------ LVISEL */
/*         |||||       [Voltage detection selection] */
/*         |||||        0: Detect level of supply voltage (VDD) */
/*         |||||        1: Detect level of input voltage from external input */
/*         |||||           pin (EXLVI) */
/*         |++++------- Be sure to clear this bit to 0   */
/*         +----------- LVION */
/*                     [Enable low-voltage detection operation] */
/*                      0: Disable operation */
/*                      1: Enable operation */

LVIS   = 0b00001001; /* Low-voltage detection level select register */
/*         ||||++++---- LVIS3 to LVIS0   */
/*         ||||        0000: VLVI0 (4.22 ±0.1 V) */
/*         ||||        0001: VLVI1 (4.07 ±0.1 V) */
/*         ||||        0010: VLVI2 (3.92 ±0.1 V) */
/*         ||||        0011: VLVI3 (3.76 ±0.1 V) */
/*         ||||        0100: VLVI4 (3.61 ±0.1 V) */
/*         ||||        0101: VLVI5 (3.45 ±0.1 V) */
/*         ||||        0110: VLVI6 (3.30 ±0.1 V) */
/*         ||||        0111: VLVI7 (3.15 ±0.1 V) */
/*         ||||        1000: VLVI8 (2.99 ±0.1 V) */
/*         ||||        1001: VLVI9 (2.84 ±0.1 V) */
/*         ||||        1010: VLVI10 (2.68 ±0.1 V) */
/*         ||||        1011: VLVI11 (2.53 ±0.1 V) */
/*         ||||        1100: VLVI12 (2.38 ±0.1 V) */
/*         ||||        1101: VLVI13 (2.22 ±0.1 V) */
/*         ||||        1110: VLVI14 (2.07 ±0.1 V) */
/*         ||||        1111: VLVI15 (1.91 ±0.1 V) */
/*         ++++-------- Be sure to clear this bit to 0   */

LVION  = 1;   /* Enable low-voltage detection */

/* Make the system wait until the low-voltage detector stabilizes (10 us or
more) */
for ( ucCounter = 0; ucCounter < 2; ucCounter++){
   NOP();
}

/* Make the system wait until VDD becomes equal to or greater than VLVI */
while( LVIF ){
   NOP();
```

```
      }

      LVIMD = 1;   /* Specify an internal reset to be generated when VDD falls below
VLVI */

      ucLEDBuffer = 0b00000111;  /* Initialize the LED lighting pattern */
   }

  /*-----------------------------------------------------------------------------
    Specify the clock frequency
  -----------------------------------------------------------------------------
    Specify the clock frequency so that the device can run on the internal high-speed
oscillation clock.
  -----------------------------------------------------------------------------*/
    OSCCTL = 0b00000000; /* Clock operation mode */
    /*         ||||+||+---- Be sure to clear this bit to 0 */
    /*         |||| ++----- RSWOSC/AMPHXT */
    /*         ||||       [XT1 oscillator oscillation mode selection] */
    /*         ||||        00: Low power consumption oscillation */
    /*         ||||        01: Normal oscillation */
    /*         ||||        1x: Ultra-low power consumption oscillation */
    /*         ||++-------- EXCLKS/OSCSELS */
    /*         ||         [Subsystem clock pin operation setting] */
    /*         ||         (P123/XT1,P124/XT2/EXCLKS) */
    /*         ||          Specify the use of the pin as an I/O port pin by specifying
000 by also using XTSTART */
    /*        ++---------- EXCLK/OSCSEL */
    /*                    [High-speed system clock pin operation setting] */
    /*                     (P121/X1,P122/X2/EXCLK) */
    /*                     00: Input port */
    /*                     01: X1 oscillation mode */
    /*                     10: Input port */
    /*                     11: External clock input mode */

    PCC    = 0b00000000; /* Select the CPU clock (fCPU) */
    /*         |||+|+++---- CSS/PCC2/PCC1/PCC0 */
    /*         ||| |      [CPU clock (fCPU) selection] */
    /*         ||| |       0000:fXP */
    /*         ||| |       0001:fXP/2 */
    /*         ||| |       0010:fXP/2^2 */
    /*         ||| |       0011:fXP/2^3 */
    /*         ||| |       0100:fXP/2^4 */
    /*         ||| |       1000:fSUB/2 */
    /*         ||| |       1001:fSUB/2 */
    /*         ||| |       1010:fSUB/2 */
    /*         ||| |       1011:fSUB/2 */
    /*         ||| |       1100:fSUB/2 */
    /*         ||| |       (Other than the above: Setting prohibited) */
```

```
   /*         ||| +------- Be sure to clear this bit to 0 */
   /*         ||+--------- CLS */
   /*         ||          [CPU clock status] */
   /*         |+---------- XTSTART */
   /*         |           [Subsystem clock pin operation setting] */
   /*         |            Specify the use of the pin by also using EXCLKS and OSCSELS
*/
   /*         +----------- Be sure to clear this bit to 0 */

   RCM    = 0b00000010; /* Select the operating mode of the internal oscillator */
   /*         |||||||+---- RSTOP */
   /*         |||||||     [Internal high-speed oscillator oscillating/stopped] */
   /*         |||||||      0: Internal high-speed oscillator oscillating */
   /*         |||||||      1: Internal high-speed oscillator stopped */
   /*         ||||||+----- LSRSTOP */
   /*         ||||||      [Internal low-speed oscillator oscillating/stopped] */
   /*         ||||||       0: Internal low-speed oscillator oscillating */
   /*         ||||||       1: Internal low-speed oscillator stopped */
   /*         |+++++------ Be sure to clear this bit to 0 */
   /*         +----------- RSTS */
   /*                     [Status of internal high-speed oscillator] */

   MOC    = 0b10000000; /* Select the operating mode of the high-speed system clock */
   /*         |+++++++---- Be sure to clear this bit to 0 */
   /*         +----------- MSTOP */
   /*                     [Control of high-speed system clock operation] */
   /*                      0: X1 oscillator operating/external clock from EXCLK pin is
enabled */
   /*                      1: X1 oscillator stopped/external clock from EXCLK pin is
disabled */

   MCM    = 0b00000000; /* Select the clock to supply */
   /*         |||||+|+---- XSEL/MCM0 */
   /*         ||||| |        [Clock supplied to main system and peripheral hardware] */
   /*         ||||| |         00: Main system clock (fXP) */
   /*         ||||| |              = internal high-speed oscillation clock (fIH) */
   /*         ||||| |             Peripheral hardware clock (fPRS) */
   /*         ||||| |              = internal high-speed oscillation clock (fIH) */
   /*         ||||| |         01: Main system clock (fXP) */
   /*         ||||| |              = internal high-speed oscillation clock (fIH) */
   /*         ||||| |             Peripheral hardware clock (fPRS) */
   /*         ||||| |              = internal high-speed oscillation clock (fIH) */
   /*         ||||| |         10: Main system clock (fXP) */
   /*         ||||| |              = internal high-speed oscillation clock (fIH) */
   /*         ||||| |             Peripheral hardware clock (fPRS) */
   /*         ||||| |              = high-speed system clock (fIH) */
   /*         ||||| |         11: Main system clock (fXP) */
   /*         ||||| |              = high-speed system clock (fIH) */
```

```
  /*         ||||| |             Peripheral hardware clock (fPRS) */
  /*         ||||| |              = high-speed system clock (fIH) */
  /*         ||||| +----- MCS */
  /*         |||||      [Main system clock status] */
  /*         +++++------- Be sure to clear this bit to 0 */

  PER0   = 0b00000000; /* Control the real-time counter control clock */
  /*         |+++++++---- Be sure to clear this bit to 0 */
  /*         +----------- RTCEN: */
  /*                     [Real-time counter control clock] */
  /*                      0: Stop supply of control clock */
  /*                      1: Supply control clock */

/*-----------------------------------------------------------------------------
  Disable peripheral hardware not to be used
-----------------------------------------------------------------------------*/
  /* 16-bit timer/event counter 00 */
  TMC00  = 0b00000000; /* Disable the counter */

  /* 8-bit timer/event counters 50 and 51 */
  TMC50  = 0b00000000; /* Disable timer 50 */
  TMC51  = 0b00000000; /* Disable timer 51 */

  /* 8-bit timers H0 and H1 */
  TMHMD0 = 0b00000000; /* Stop timer H0 */
  TMHMD1 = 0b00000000; /* Stop timer H1 */

  /* Real-time counter */
  RTCC0  = 0b00000000; /* Stop the counter */

  /* Clock output controller */
  CKS    = 0b00000000; /* Stop the clock frequency divider */

  /* A/D converter */
  ADM0   = 0b00000000; /* Stop A/D conversion */

  /* Operational amplifiers */
  AMP0M  = 0b00000000; /* Stop operational amplifier 0 */
  AMP1M  = 0b00000000; /* Stop operational amplifier 1 */

  /* Serial interface UART6 */
  ASIM6  = 0b00000001; /* Disable the interface */

  /* Serial interface IICA */
  IICACTL0 = 0b00000000;  /* Disable the interface */

  /* Serial interfaces CSI10 and CSI11 */
  CSIM10 = 0b00000000; /* Disable CSI10 */
```

```
  CSIM11 = 0b00000000; /* Disable CSI11 */

  /* Interrupts (The interrupts to be used are enabled later) */
  MK0    = 0xFFFF;     /* Disable all interrupts */
  MK1    = 0xFFFF;

  /* Key interrupts */
  KRM    = 0b00000000; /* Disable all key interrupts */

/*-----------------------------------------------------------------------------
  Output the LED lighting pattern
-----------------------------------------------------------------------------*/
  P0 = ( ucLEDBuffer & 0b00000011 );          /* Control LED1 and LED2 */
  P6 = ( (ucLEDBuffer & 0b00000100) >> 2 );   /* Control LED3 */

/*-----------------------------------------------------------------------------
  Set up interrupts
-----------------------------------------------------------------------------*/
  EGPCTL0   = 0b00000000; /* Disable the INTP1 rising edge */
  EGNCTL0   = 0b00000010; /* Enable the INTP1 falling edge */
  PIF1   = 0;             /* Clear the INTP1 interrupt request */
  PMK1   = 0;             /* Enable the INTP1 interrupt */

/*-----------------------------------------------------------------------------
  Enable interrupts
-----------------------------------------------------------------------------*/
  EI();  /* Enable interrupts */

}


/*****************************************************************************

  Main loop

*****************************************************************************/
void main(void)
{
  while (1){
     NOP(); /* Make the system wait for an interrupt to occur */
  }
}

/*****************************************************************************

  INTP1 interrupt servicing (by using the INTP1 falling edge)

*****************************************************************************/
```

```
__interrupt void fn_intp1(void)
{
  unsigned short ushCounter; /* Count variable */

  /* Make the system wait for about 10 ms to prevent chattering */
  for( ushCounter = 0; ushCounter < 2850; ushCounter++ ){
     NOP();
  }
  PIF1  = 0;    /* Clear the INTP1 interrupt request */

  /* If switch input continues */
  if( !P3.0 ){
     ucLEDBuffer--;             /* Switch the LED lighting pattern */
     ucLEDBuffer &= 0b00000111; /* Mask unnecessary sections */

     P0 = ( ucLEDBuffer  & 0b00000011);         /* Control LED1 and LED2 */
     P6 = ( (ucLEDBuffer & 0b00000100) >> 2 );  /* Control LED3 */
  }
}
```

APPENDIX B USING 78K0/KC2-L 44-PIN PRODUCTS

All 78K0/KC2-L sample programs are intended for 48-pin products. To use a 78K0/KC2-L sample program for a 44-pin product, specify the following settings:

(1) Initial settings of ports

- Setting up port 0
  Change the value of bit 2 of port mode register 0 (PM0) from “0” to “1”.

- Setting up port 4
  Change the value of bit 2 of port mode register 4 (PM4) from “0” to “1”.

- Setting up port 7
  Change the values of bits 5 and 4 of port mode register 7 (PM7) from “00” to “11”.

(2) Disabling unused peripheral hardware

Delete the instruction used to set up the clock output selection register (CKS).

APPENDIX C REVISION HISTORY

Edition	Date Published	Page	Revision
1st edition	September 2009	–	–

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