NEC

Application Note

V850ES

32-Bit Single-Chip Microcontrollers

External Bus Interface

V850ES/Fx2 Series

V850ES/Hx2 Series

V850ES/Jx2 Series

V850ES/Kx1+ Series

V850ES/Sx2 Series

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NEC Electronics America Inc.
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Europe) GmbH
Duesseldorf, Germany
Tel: 0211-65 030
Fax: 0211-65 03 1327

Sucursal en España
Madrid, Spain
Tel: 091- 504 27 87
Fax: 091- 504 28 60

Succursale Française
Vélizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

Filiale Italiana
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

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Eindhoven, The Netherlands
Tel: 040-265 40 10
Fax: 040-244 45 80

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Taeby, Sweden
Tel: 08-638 7200
Fax: 08-638 7222

United Kingdom Branch
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Korea Ltd.
Seoul, Korea
Tel: 02-558-3737
Fax: 02-558-5141

NEC Electronics Singapore Pte. Ltd.
Singapore
Tel: 65-6253-8311
Fax: 65-6250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-8175-9600
Fax: 02-8175-9670

Introduction

Target Readers

This application note is intended for users who understand the functions of the V850ES/Fx2 /Hx2 /Jx2 /Kx1+ /Sx2 and will use this product to design application systems.

Purpose

The purpose of this application note is to help users to understand the functionality, benefits and how to use the external bus interface implemented in several microcontrollers of the V850ES Series. subseries. The handling and usage shown in this document are for reference only. Correct operation is not guaranteed if these techniques are implemented as they are described here.
The user has to adapt the usage and handling of the external bus interface to his application specific needs.

Organization

This manual consists of the following main sections.
- Reason for an external bus
- Functionality of a an external bus interface
- V850 external bus interface
- External bus interface in the application

How to Read This Manual

It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
→ Read this manual in the order of the **CONTENTS**. The mark “<R>” shows major revised points. The revised points can be easily searched by copying an “<R>” in the PDF file and specifying it in the “Find what:” field.

- To learn more about the V850 hardware functions:
→ See the user’s manual of each V850 product.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	xxx (overscore over pin or signal name)
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeral representation:	Binary.....xxxx or xxxxB
	Decimal xxxx
	Hexadecimal .....xxxxH

Table of Contents

List of Figures

List of Tables

CHAPTER 1 REASON FOR AN EXTERNAL BUS

1.1 Reason and benefit of an external parallel bus interface

It allows access to external devices using a fast parallel bus. External memory is a special case of using the external bus interface. The external bus interface is capable to access various devices which have an parallel 8/16/32-Bit bus interface.

Applications where the throughput of a serial interface is insufficient. Memory mapped devices like graphics controller often have a parallel bus interface to achive a huge data throughput. In addition, there is no need for a special access driver in the application to access external registers like when using a serial interface.

It can extend the internal memory.

If the device have insufficient internal memory capabilities.

For dynamic volatile data, SRAM can be attached to the bus interface. Because of the slower and smaller 16bit bus (related to the high speed internal 32bit bus), it should carefully considered to use external SRAM also for fast dynamic application data.

For non-volatile data, flash or ROM could be attached to the external bus interface. It can be used for storing a large amount of constant data like picture for graphical controllers. It should be carefully considered for code extension, because of slower access.

The application require a big amount of slow memory and a system using an external memory device is cheaper than a microcontroller with more high-speed internal memory.

CHAPTER 2 FUNCTIONALITY OF THE EXTERNAL BUS INTERFACE

2.1 Types of external bus interfaces

Every parallel bus interface need 8/16/32 data lines and a minimum of address lines. This is same for every external device at this bus. But different devices need different control signals. The simplest parallel bus interface is for an external SRAM or flash memory. The standard bus interface in a V850 microcontroler offer at least control signals for such devices.

The data bus width can usually be switched between 8-Bit and 16-Bit. If the data bus is set to 16-Bit mode, the address line A0 is never used. The selection between even and odd byted is made by control signals which select the low- or high-Byte of the 16-Bit Halfword. If a 16-Bit SRAM is connected, adress line A1 of the V850 have to be connected to the address line A0 of the SRAM.

For V850 devices, which offer a 32-Bit data bus width, adress lines A0 and A1 are not used. Therefore four control signals are used to select a Byte of a 32-Bit Word. E.g. following series: V850E/MEx

The bus controller of every V850 microcontroller allow also the access to unaligned data. That means, the a 32-Bit word do not have to be aligned to a word address where the lowest two address bits are zero. The internal bus controller would generate additional bus accesses to fetch also unaligned data. Nevertheless it is suggested to place data or code at aligned addresses. This allow a faster access to the values, while unaligned accesses may save a little bit of memory space.

More sophisticated memory devices like DRAM, EDO, SDRAM or burst mode flash memories need some special control signals for page managment and data refreshing. Only V850 microcontrollers with a dedicated memory controller offer also these control signals. The User's Manual of these devices describe the configuration of the memory controller in detail. E.g. following series: V850E/MAx, V850E/MSx, V850E/MEx

The external memory could be transfered between the internal RAM or a peripheral using the DMA controller of the device. Using this feature, e.g. large data from a serial interface could be automatically transfered to an external memory without consuming CPU power.

2.2 Bus signals

An external parallel bus interface usually need following signals

Address bus

Minimum count of addres lines for external device. A memory device usually need a lot of addres lines. E.g. a 128 KByte SRAM by 16-Bit data bus width need 16 address lines. A SRAM with the same size, but using a 8-Bit data bus need 17 address lines.

Data bus

8 / 16 / 32 data signals

Control signals

- Chip select

  More than one signal to select one of the external devices in the same external address range

- Read

  Signal to force the external device to put data on the data bus

- Write

  Signal to force the external device to read data from the data bus

- Byte select signals

  Signal to force the external device to write only defined bytes of a 16/32-Bit data bus. For reading this is not needed, because the V850 always read the full data bus width and select the needed byte by the internal bus control unit.

- Wait

  Signal to force the V850 microcontroller to wait until the wait signal is released.

- Bus hold

  Signals to allow a multimaster bus usage.

All these signals are needed at the same time to access an external device attached to the bus. But this need a lot of pins on the side of the microcontroller. Pins which are sometimes shared with other functions or needed by the application. One solution could be to choose a microcontroller with more pins. Therefor, some microcontrollers offer the to switch between multiplexed and non-multiplexed mode. The non-multiplexed mode is also called separate mode.

2.3 Non-multiplexed / Separate bus

This mode offer a fast, but pin-consuming external bus interface. The address bus and the data bus is separat available at port pins. It can directly be connected to the adress and data bins of the external device. A V850 microcontroller need at minimum two system clock cycles to access an external adress in this mode.

2.4 Multiplexed bus

This mode offer an external bus interface which is slower, but need lees external pins. The address bus and the data bus is multiplexed. It need an external address latch and an additional control signal to latch the address. For each access at least three system clocks are needed. The first step is to output the address to the multiplexed bus and the dedicated control signal to latch the address externally. The latched address can be connected to the external device. The multiplexed address/data bus can direclty be connected to the data lines of the device. The control signals will be active after the address periode in the timing. For details, please refer to the chapter Bus Timing. The signal for the external address latch is usually called 'ASTB' (Adress Strobe).

2.5 Bus Timing

The following diagrams show an access to the external bus interface.

The data sheet of the device define the excat timings for each signal of the interface.

The red marked logical levels are only valid for the separate bus mode.

Figure 2-1. Bus Timing Read

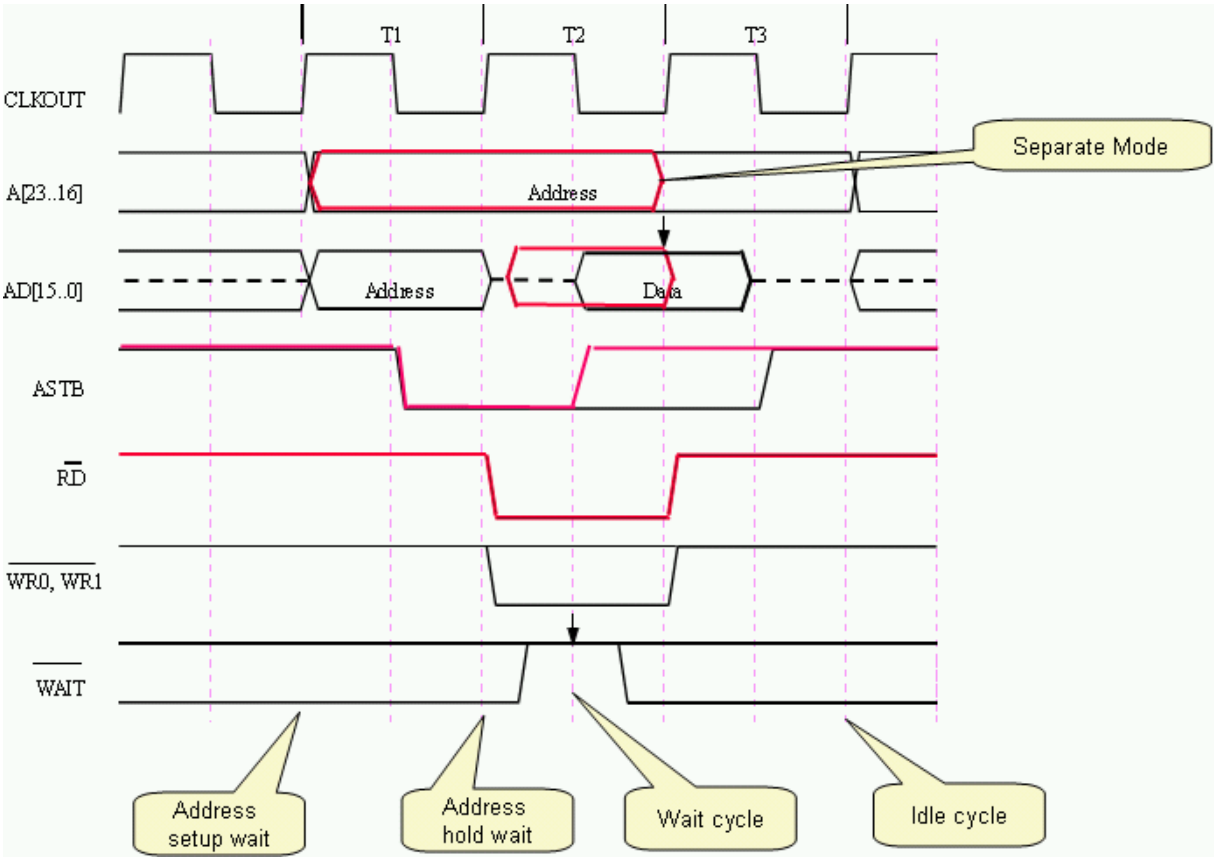
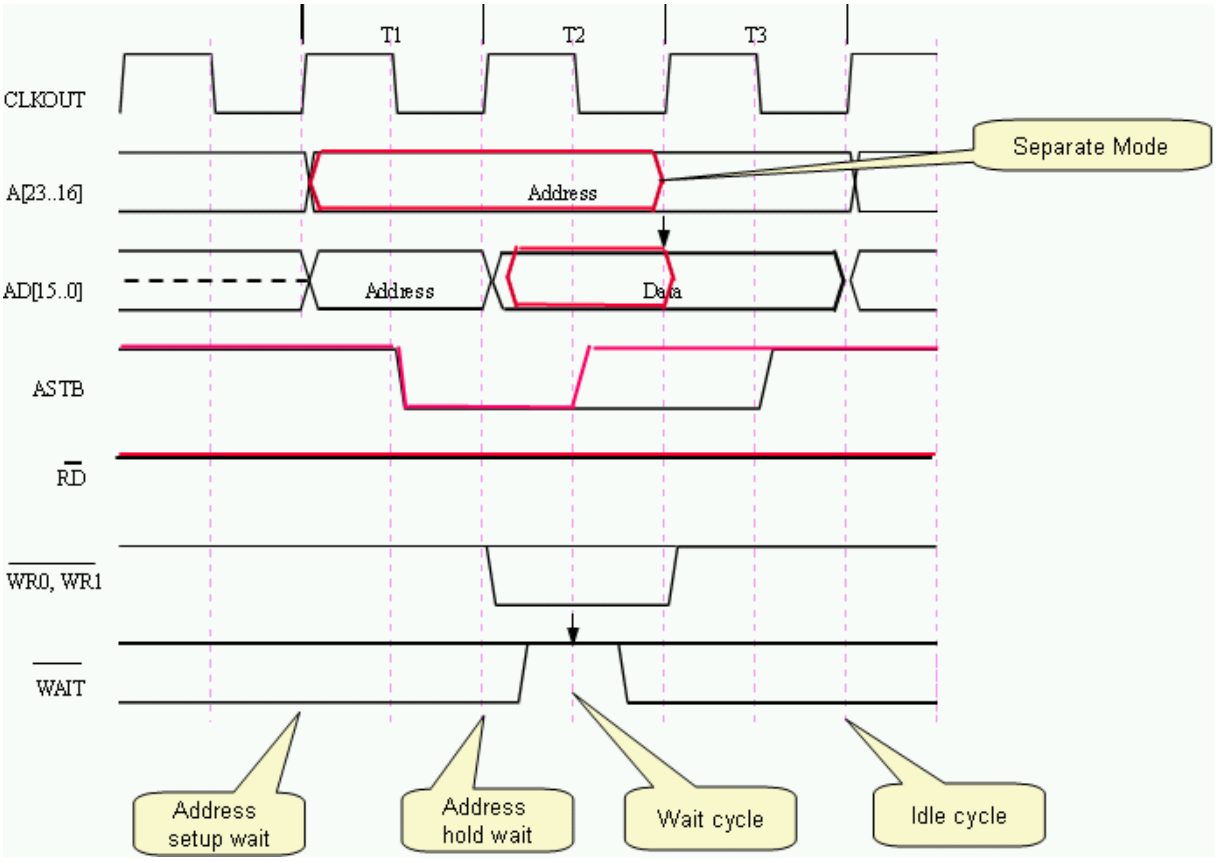


Figure 2-2. Bus Timing Write



2.6 Wait generation

The minimum access time for accessing an external device is often too fast. E.g. standard flash memories are usually not fast enough to access them with full speed. Therefore, several features are implemented to slow down the bus to meet the timing requirements.

Programmable wait cycles

- Data wait control register (DWCn)

  To realize interfacing with a low-speed memory or I/O, up to seven data wait states can be inserted in the bus cycle that is executed for each CS space. This allow slower devices to set data to the bus, or receive data after an increased time.

- Address wait control register (AWC)

  This additional wait cycle enlarge the time where the address is output to an external device.

- Bus cycle control register (BCC)

  By inserting an idle state, the data output float delay time of the external device can be secured during read access (an idle state cannot be inserted during write access).

1. The internal ROM and internal RAM areas are not subject to programmable waits, and are always accessed without a wait states. The on-chip peripheral I/O area is also not subject to programmable waits, and only wait control from each peripheral function is performed.

2. Write to the configuration register after reset and do not change them when using the bus interface. Do not access an external memory area until the initial settings of the configuration registers are complete.

External wait signal

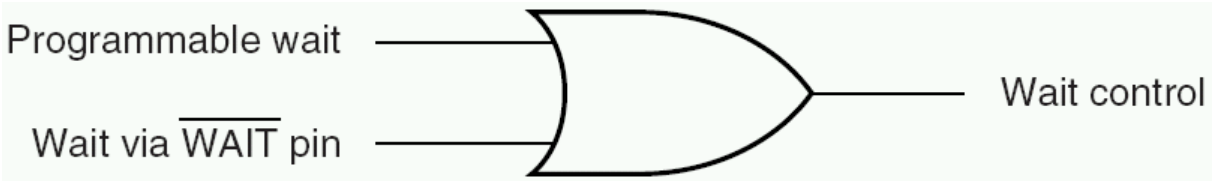
This signal is low active and will force the external bus to wait and hold all pin levels until the signal is release to high again. Using this signal, slow I/O devices can force the master device to wait until the slave device is ready and release the signal.

Access to each area of the internal ROM, internal RAM, and on-chip peripheral I/O is not subject to control by the external wait function, in the same manner as the programmable wait function.

Please consider using this signal carefully. If the CPU access an external device which force this signal to low, the CPU is not able to continue until this signal is released. No interrupt function can be serviced if the wait signal is set to low while the CPU access this external device. If this signal is set to low while no bus access is done, the CPU will incessantly continue executing code. The CPU will stop when accessing the external bus and the wait signal is set.

The programmable and external wait signal is used in parallel to force the access to wait:

Figure 2-3. Wait generation



2.7 Bus Hold Function

Two pins are available to allow a generation of a multi-master bus system.

When the HLDRQ pin is asserted (low level), indicating that another bus master has requested bus mastership, the external address/data bus goes into a high-impedance state and is released (bus hold status). If the request for the bus mastership is cleared and the HLDRQ pin is deasserted (high level), driving these pins is started again.

During the bus hold period, execution of the program in the internal ROM and internal RAM is continued until an on-chip peripheral I/O register or the external memory is accessed.

The bus hold status is indicated by assertion of the HLDAK pin (low level). The bus hold function enables the configuration of multi-processor type systems in which two or more bus masters exist.

Note that the bus hold request is not acknowledged during a multiple-access cycle initiated by the bus sizing function or a bit manipulation instruction.

2.8 Little Endian

The V850 CPU core and all successors only support the little endian access mode internally. A word (32-bit) could also accessed halfword-wise(16bit) or bytewise (bit). The little endianess determine that the byte or halfword at the lowest address (which is the same as the word address) access the lowest significant bits in the word. The higher adresses will access the more significant bits of the word.

This is the same for accessing a halfword (16bit) bytewise. The lowest byte address the lowesr significant byte, which has the same address like the half-word.

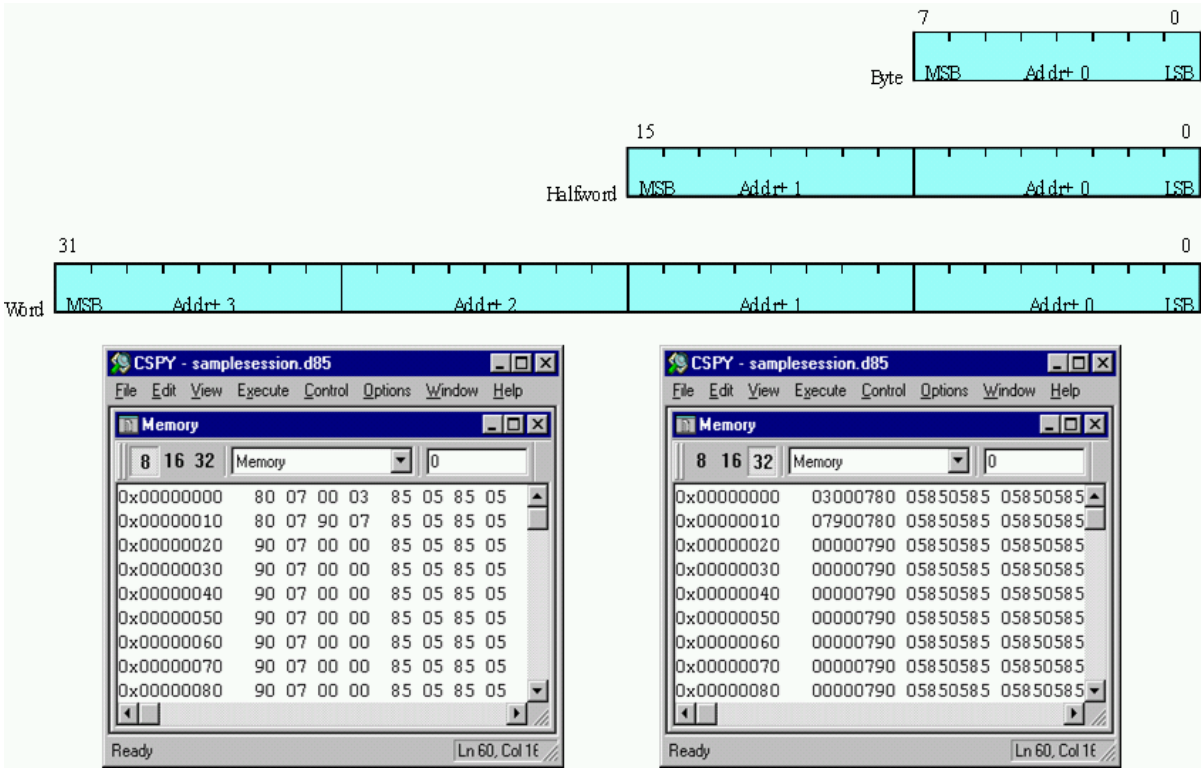
Some NEC microcontrollers allow for the external bus the switching between little endian and big endian access mode. Internally always little endianess is used to handle data. If the endianess is set to big endiann, the format will be converted to fit to the internal little endian access mode.

The endianess can be set different for any specific chip select signal. In this way, a mixed system with little and big endianess can be generated.

For microcontroller which do not have the possibility to switch between little and big endianess for external devices, special conversion instructions can be used to swap bytes or halfword with only one instruction clock to meet the correct structure. See assembly instructions.

Byte Swap Half-word	BSH
Byte Swap Word	BSW
Half-word Swap Word	HSW

Figure 2-4. Little Endian



CHAPTER 3 V850 EXTERNAL BUS INTERFACE

3.1 Fundamental description of the external bus interface in V850ES Series

Following series include the separated and multiplexed bus mode. It can be switched globally between the two modes by a SFR setting.

V850ES/Kx1 Series

- V850ES/KJ1

V850ES/Kx1+ Series

- V850ES/KJ1+

V850ES/Sx2 Series

V850ES/Jx2 Series

Following series do not include the separated bus mode. These devices only include the multiplexed bus mode with a maximum address range of 64 KByte and additional four chip select signals. This will create a maximum memory access of 256 KByte.

V850ES/Fx2 Series

- V850ES/FJ2

V850ES/Hx2 Series

- V850ES/HJ2

3.2 Chip Select area

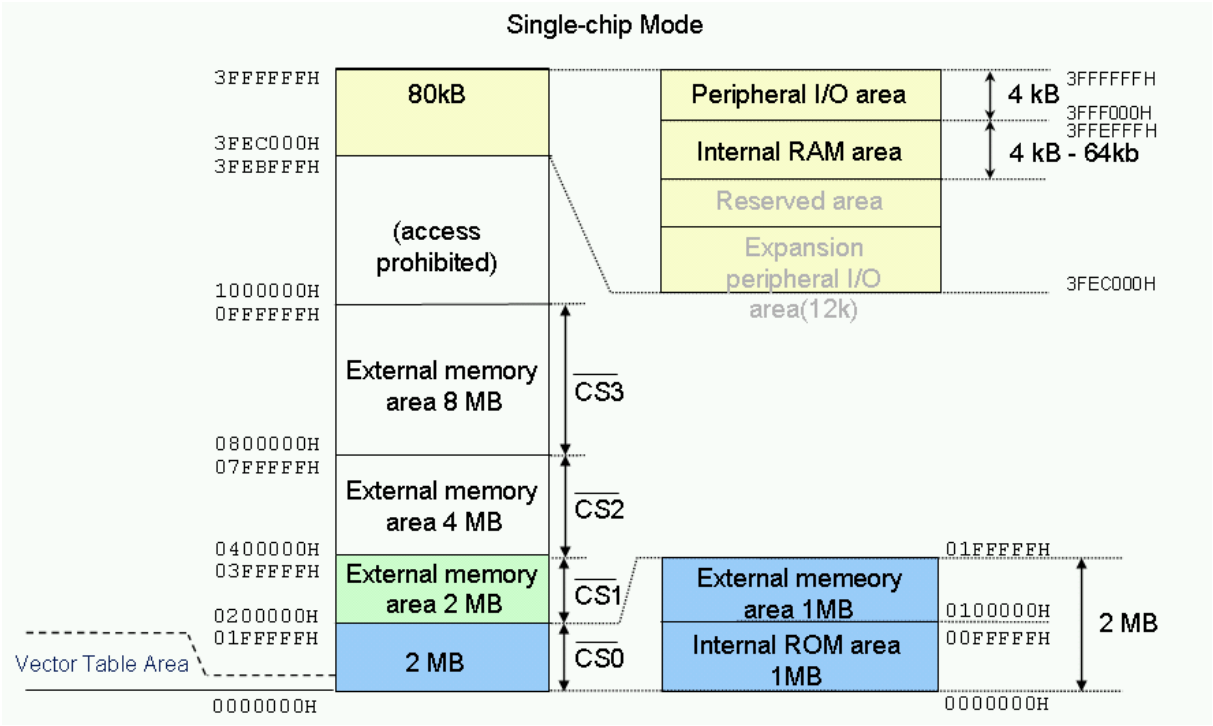
Depending on the internal accessed address, an external chp select signal can automatically set to access external devices.

The range for each chip select signal is fixed in most devices and have different sizes.

The range for the lowest chip select signal CS0\ start always at address zero. But accessing the lowest one Megabyte area will not activate the chip select signal. The lowest one Megabyte is always reseved for the internal flash memory. Even if the flash memory is smaller than one Megabyte, this area cannot be used externally. CS0\ can only access one Megybyte above the first internal Megabyte reserved for the internal flash.

The maximum external address range is defined by the range of the address bus, the number of chip selct signals and the internal range for the chip select signals.. E.g. V850ES/FJ2 have 24 address lines which allows to access 16 Mbyte memory. The four chip select signals cannot enlarge this area by four, because the internal access is limited to 16 Mbyte. Additionally, the lowest one Mbyte is reserved for the internal flash memory. V850ES/FJ2 can access up to 15 Mbyte external memory in total with different chip select signals.

Figure 3-1. Chip Select Areas



3.3 Voltage levels

Some devices allow a different operating voltage for the external bus interface. Therefore, the device have different power supply pins for the bus interface pins and other I/O pins.

E.g. V850ES/SJ2 can be controlled at a different voltage from the operating voltage. However, set BVDD = EVDD = VDD in the separate bus mode. Otherwise, the memory bus would have to work with different voltage levels.

3.4 Bus signals

The pins used to connect an external device are listed in the table below.

Table 3-1. External Bus Pins (Multiplexed Bus)

Bus Control Pin	Alternate-Function Pin I/O	I/O	Function
AD0 to AD15	PDL0 to PDL15	I/O	Address/data bus
A16 to A23	PDH0 to PDH5	Output	Address bus
WAIT	PCM0	Input	External wait control
CLKOUT	PCM1	Output	Internal system clock
WR0, WR1	PCT0, PCT1	Output	Write strobe signal
RD	PCT4	Output	Read strobe signal
ASTB	PCT6	Output	Address strobe signal
HLDRQ	PCM3	Input	Bus hold control
HLDAK	PCM2	Output	
CSn	PCSn	Output	Chip select

Table 3-2. External Bus Pins (Separate Bus)

Bus Control Pin	Alternate-Function Pin I/O	I/O	Function
AD0 to AD15	PDL0 to PDL15	I/O	Address/data bus
A0 to A15	P90 to P915	Output	Address bus
A16 to A23	PDH0 to PDH5	Output	Address bus
WAIT	PCM0	Input	External wait control
CLKOUT	PCM1	Output	Internal system clock
WR0, WR1	PCT0, PCT1	Output	Write strobe signal
RD	PCT4	Output	Read strobe signal
HLDRQ	PCM3	Input	Bus hold control
HLDAK	PCM2	Output	
CSn	PCSn	Output	Chip select

When the internal ROM, internal RAM, or on-chip peripheral I/O are accessed, the status of each pin is as follows.

Table 3-3. Pin Statuses by Internal ROM/RAM, or On-Chip Peripheral I/O Access

Separate Bus Mode		**Multiplexed Bus Mode**	
Address bus (A21 to A0)	Undefined	Address bus (A21 to A16)	Undefined
Data bus (AD15 to AD0)	Hi-Z	Address/data bus (AD15 to AD0)	Undefined
Control signal	Inactive	Control signal	Inactive

Caution When a write access is performed to the internal ROM area, address, data, and control signals are activated in the same way as access to the external memory area.

CHAPTER 4 EXTERNAL BUS INTERFACE IN THE APPLICATION

4.1 Connection

A typical connection of an external SRAM is showm in following diagrams.

Figure 4-1. External bus interface with one 8-Bit SRAM

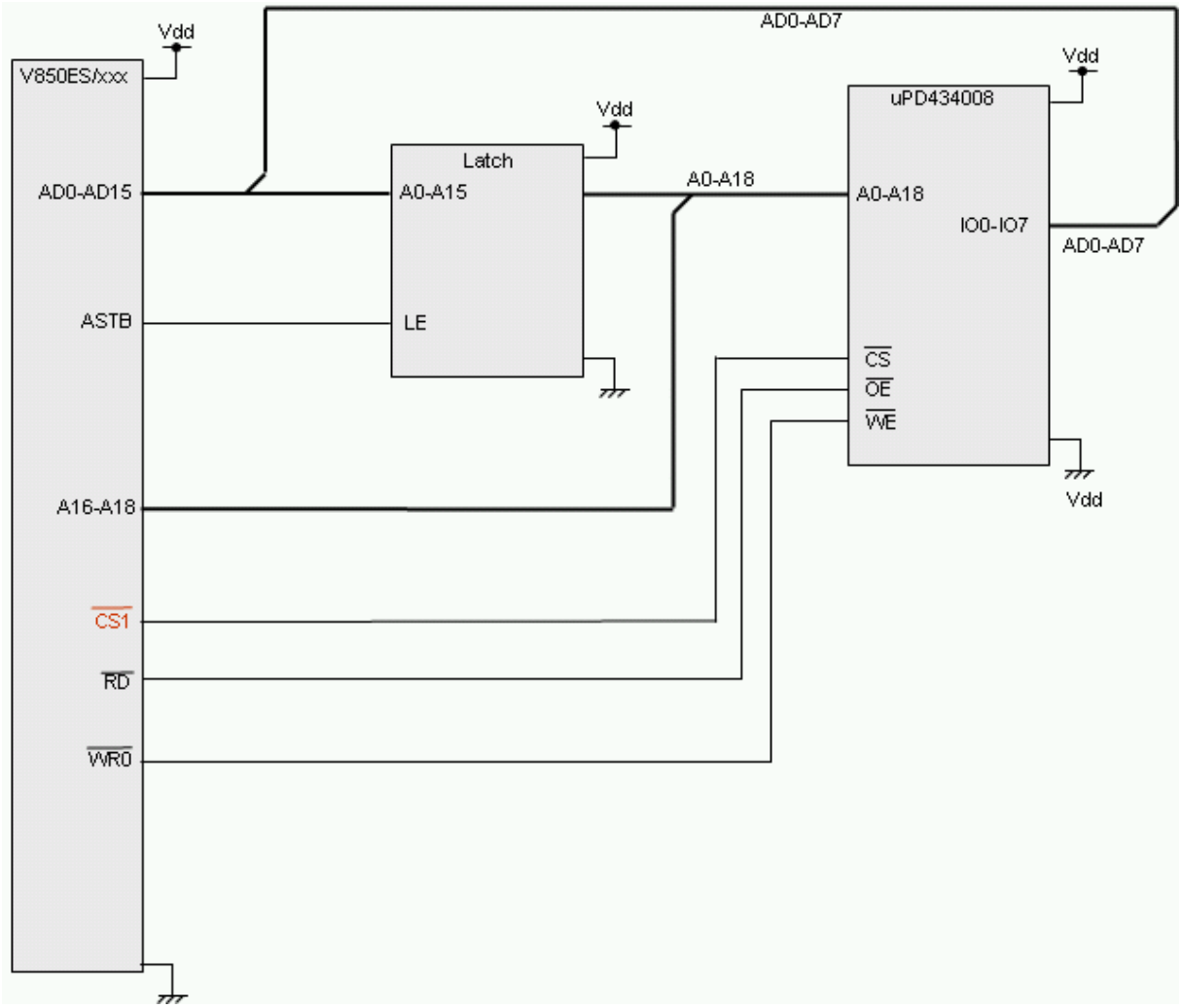


Figure 4-2. Figure 4-3. External bus interface with two 8-Bit SRAMs

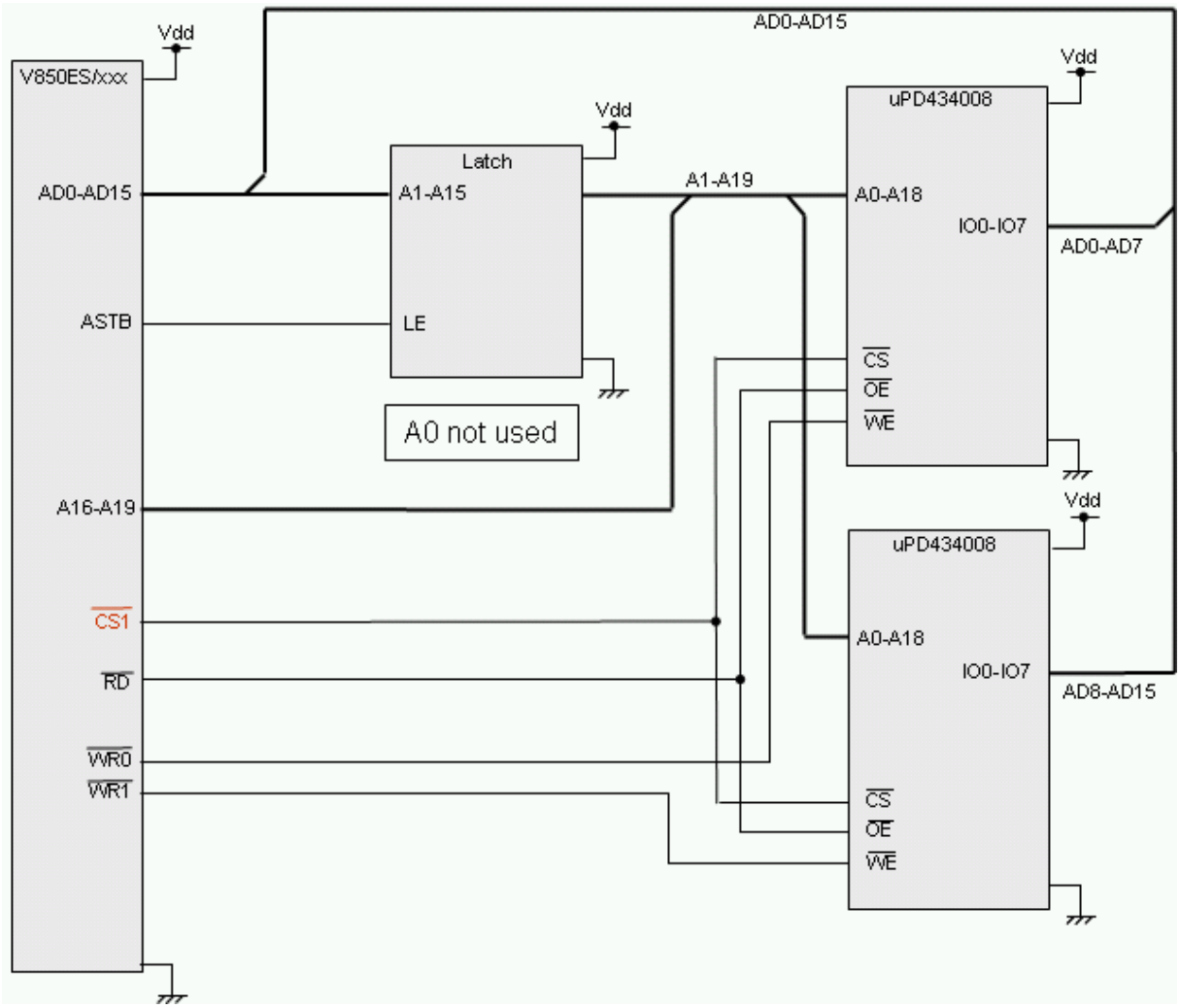
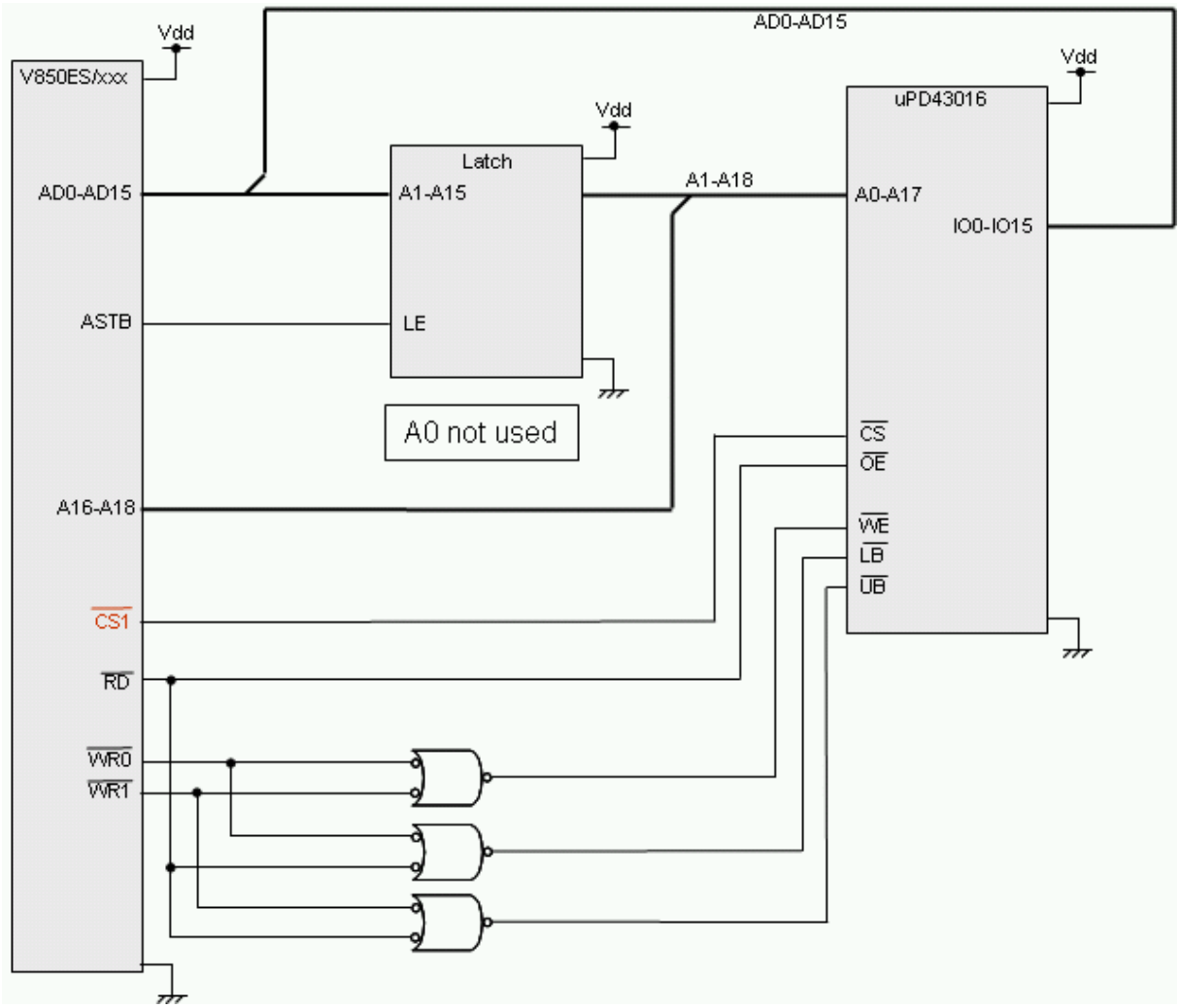


Figure 4-4. External bus interface with one 16-Bit SRAM



Note that address line A0 zero is never used in a system with a 16-Bit bus. A 32-Bit bus never use the address lines A0 and A1. These lines will ever be zero.

4.2 Initialization

All port pins which are used for the external bus interface are shared with I/O's on alphanumerical ports. Alphanumeric ports are all ports with a charachter in the name instead of a number. E.g. PDL, PCM, PCS, PCT, PDH. There is only one exception for a device which support also the separate bus mode. For this mode the separat lower address lines are shared with port P9 (numeric port).

Bus Interface Ports: PDL, PCM, PCS, PCT, PDH, (P9)

All signals lines which should be used for the external bus interface should be set to alternate function by setting the corresponding bit in the port mode control register. This automatically switch the port pin to the bus interface mode. It is not necessary to switch to input/output mode be setting the port mode register.

All pins which should not be used for external bus interface, should be set to I/O function be leaving the port mode control register at zero at the corresponding bit position.

External bus interface mode control register (EXIMC)

This register consist of only one bit which choose between Multiplexed bus mode and Separate bus mode

Bus size configuration register (BSC)

For each used chip select signal the bus size can be defined between 8-Bit and 16-Bit data bus width.

Data wait control register 0 (DWCn)

For each used chip select signal the data wait states ca be set in a range between 0-7.

Address wait control register (AWC)

For each used chip select signal the address wait states ca be set in a range between none and one.

Bus cycle control register (BCC)

For each used chip select signal the cycle wait states ca be set in a range between none and one.

After initialization of all these registers, the bus interface can be used to access external devices.