Introduction

The main purpose of this project is to design a circuit that can increase the frequency of a reference signal by two, while attempting to keep a 50% duty cycle on the doubled frequency. This is an interesting challenge, because while it is fairly simple to divide a clock frequency by two, it is more challenging to increase the frequency of a clock signal. The goal in this app note is to accomplish this task with components inside a GreenPAK™ SLG46621V device, without needing many external components like voltage-controlled oscillators.

Initial Solution

A simple way to double a frequency is to create a short one-shot pulse on the rising and falling edges of your initial clock signal. In GreenPAK Designer, that would look something like this:

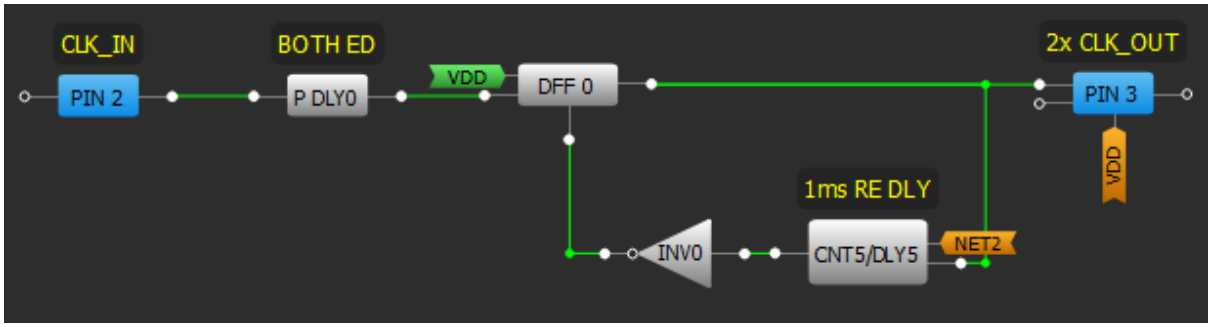

Figure 1. Initial solution

The both edge detector creates a short pulse every time CLK_IN transitions from HIGH to LOW or from LOW to HIGH. Those edge detector pulses clock VDD through DFF0, which is passed through a 1ms rising edge delay. Once it propagates through the delay, it is used to reset the DFF. This means that every time CLK_IN has an edge, it will create a 1ms pulse on the output.

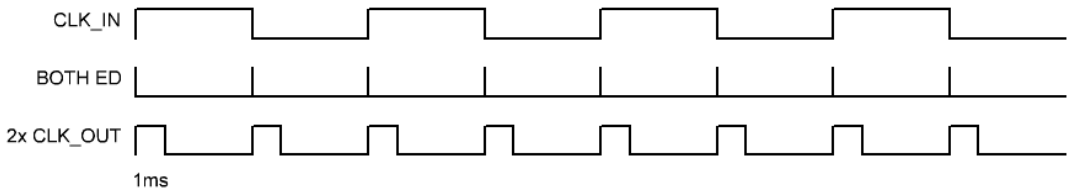

Figure 2. Timing diagram of initial solution

This technique has the downside of not guaranteeing a 50% duty cycle on the output. If you know what your input frequency is, you can adjust the amount of time in the delay block to create a 50% duty cycle. However, if you have a variable input frequency, this technique won't cut it.

Recovering the duty cycle

In order to recover the duty cycle, we need to create a different circuit that follows the steps shown in the figure below.

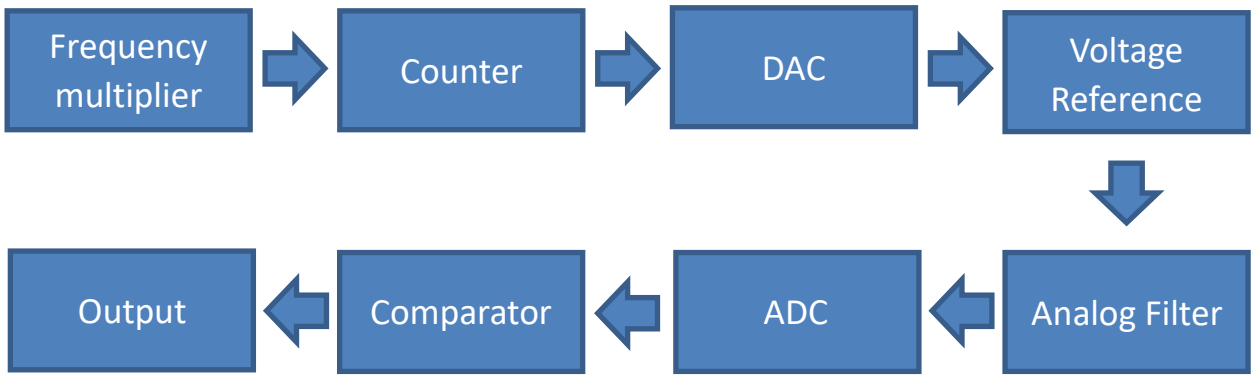

Figure 3. Block flowchart

The overall GreenPAK design is shown in the figure below:

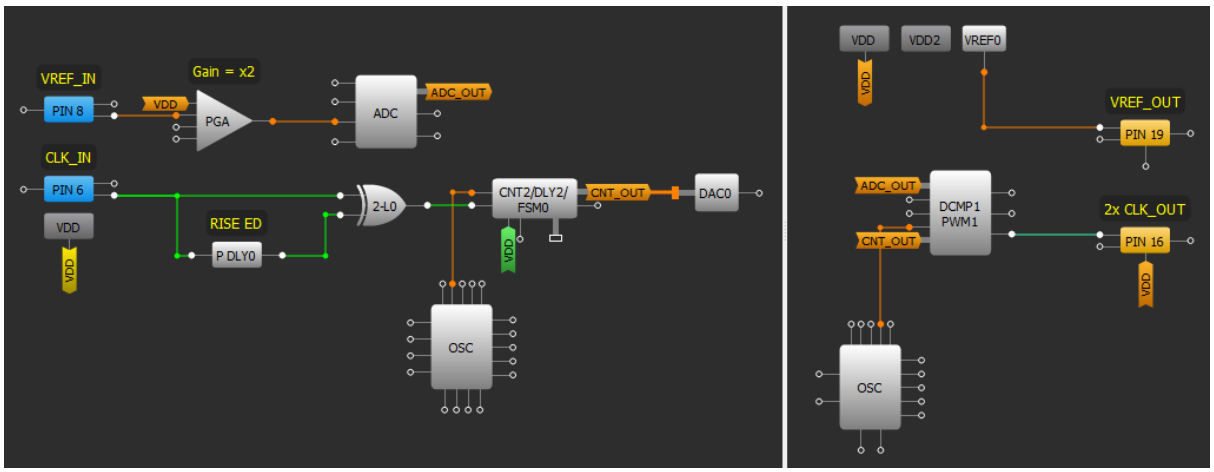

Figure 4. Overall GreenPAK design

The sections of the design can be broken into the following areas:

- Edge Detector
- Counter
- DAC (Digital to Analog Converter) and VREF (Voltage Reference)
- ADC (Analog to Digital Converter) and DCMP (Digital Comparator)

We will discuss each section one at a time.

The Edge Detector

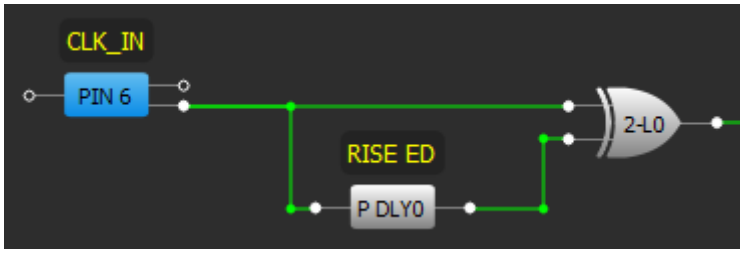

Figure 5. Edge detector

As seen in Figure 4, we use a rising edge detector and an XOR gate to double the frequency of the input signal. Now, other blocks are needed to generate the 50% duty cycle.

The Counter

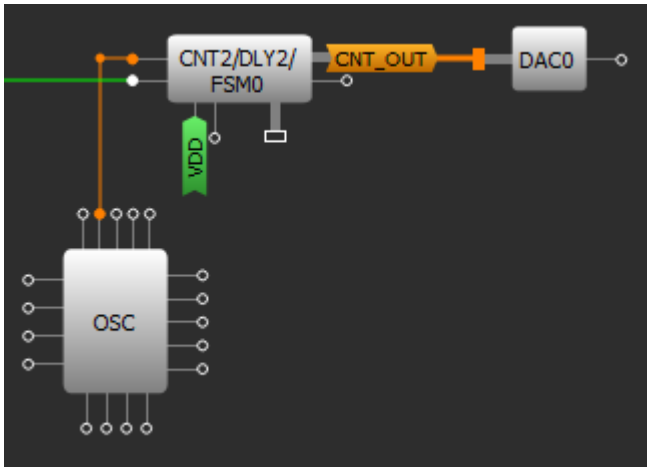

Figure 6. Counter to DAC

This counter block will count from 0 to 255. Every time a rising edge occurs on the RESET_IN pin of the counter, the counter value will reset to 0 and begin counting back up to 255. The output of the counter is connected to the DAC, which means that the value received by the DAC will be a ramp signal with positive slope.

The DAC and Voltage Reference

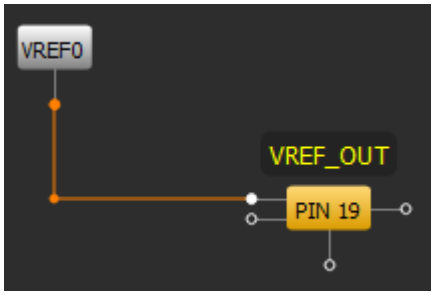

Figure 7. VREF connection

The VREF0's source selector is set to "DAC0 out" in the properties panel of the VREF0 block. This means that the analog voltage output at PIN 19 via the VREF block will be proportional to the value of the counter's value.

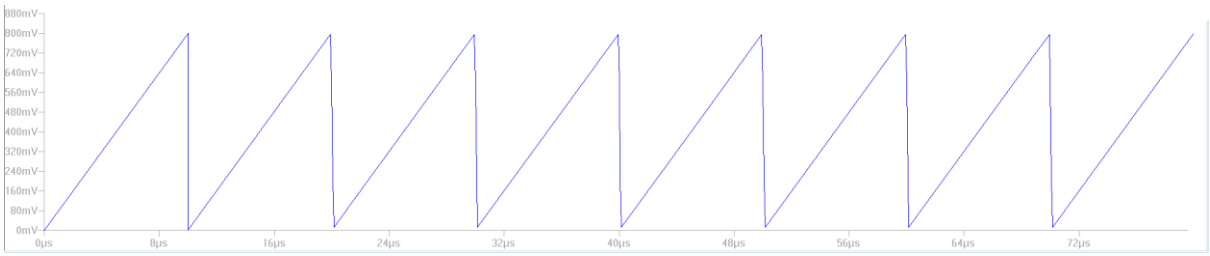

Figure 8. VREF output

Figure 8 presents the output voltage generated by the DAC and voltage reference. The counter counts up at a rate of 27MHz, which is the frequency of the GreenPAK's Ring oscillator. The output is periodically reset by CLK_IN. In other words, the maximum value of the counter tells us how many high frequency clock cycles can fit in a period of the CLK_IN signal. This value is proportional with the reference signal frequency, because the clock frequency is always the same and the frequency of the ramp is equal to the frequency of the reference signal.

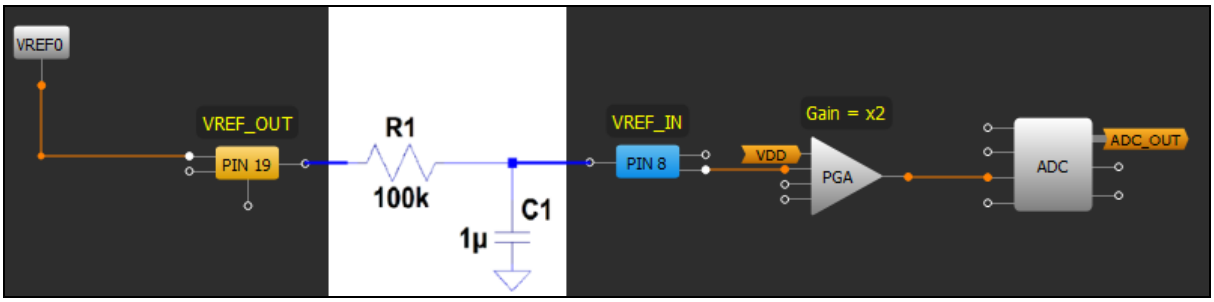

Figure 9. Feedback mechanism

The ramp signal is then powerfully filtered using a RC filter with 1.6 Hz cutoff frequency, and the output of the filter is connected to PIN 8. In other words, the output of this filter will generate the mean value of the ramp signal, which is:

$$V_{mean} = \frac{1}{T}\int_0^T f(t)dt = \frac{1}{2} * V_{peak}$$

The ADC and the Comparator

Figure 10. PGA and ADC

After the signal is filtered it is sampled by the ADC and sent to one of the GreenPAK's DCMPs (Digital Comparators). The other input of the comparator is connected the output of the counter, which creates the ramp signal as shown in Figure 7. So, the comparator inputs are a ramp signal with amplitude V_{peak} and a continuous signal equal to $\frac{1}{2}V_{peak}$. This means that the output of the comparator will be low when the ramp is under the threshold and high when the ramp's instantaneous value exceeds half of its amplitude. The PGA gain is set to 1.

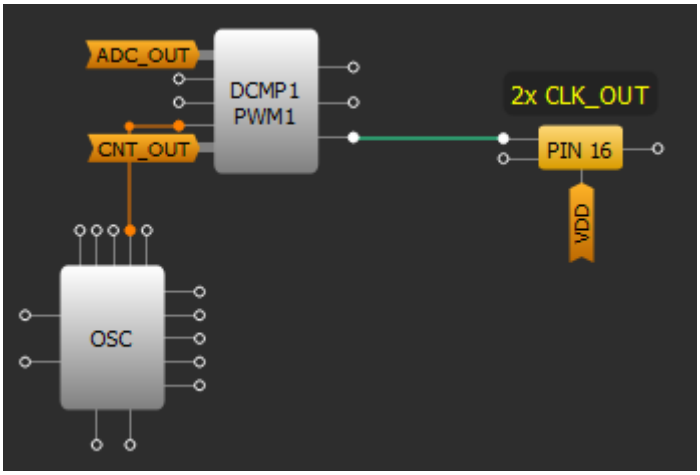

Figure 11. DCMP and output

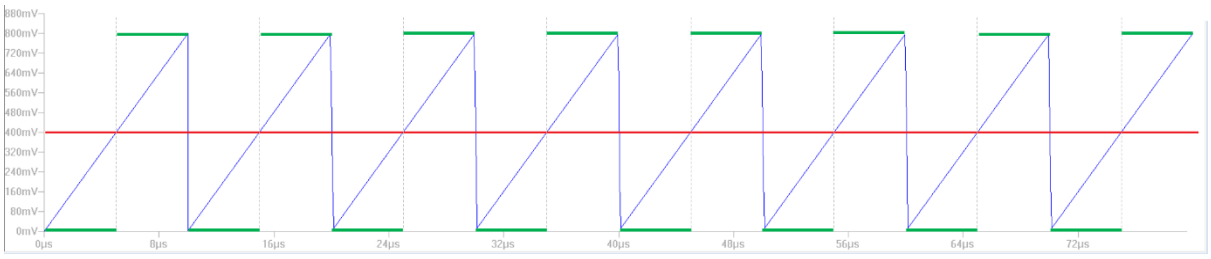

Figure 12. Input and output waveforms

The waveforms related to the input and output signals are displayed in Figure 12. The red signal represents the continuous signal provided by the filter, while the green signal is the comparator output. Thanks to the feedback mechanism, the red signal continuously shifts its level according to the amplitude of the ramp (or the frequency of the input signal) in order to ensure a 50% duty cycle.

Adjustments

The DAC and the ADC have slightly different reference voltages. For instance, if the input of the DAC is 122, the output of the ADC may be different. To solve this problem, we scaled the filtered signal to fit in the ADC range with a simple voltage divider.

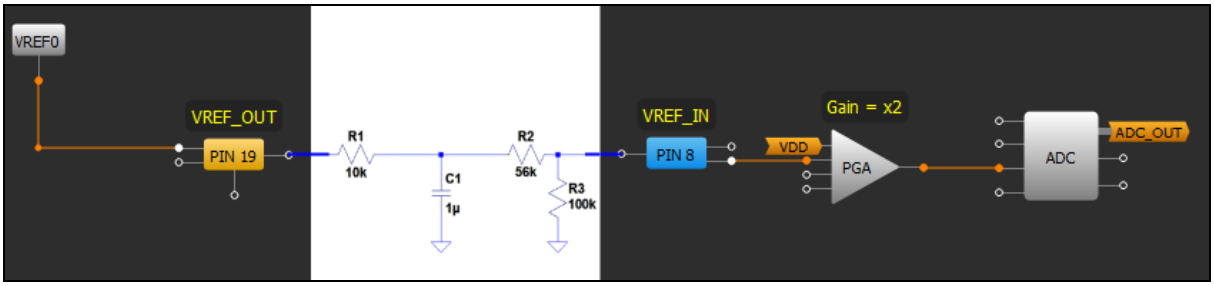

Figure 13. Voltage divider

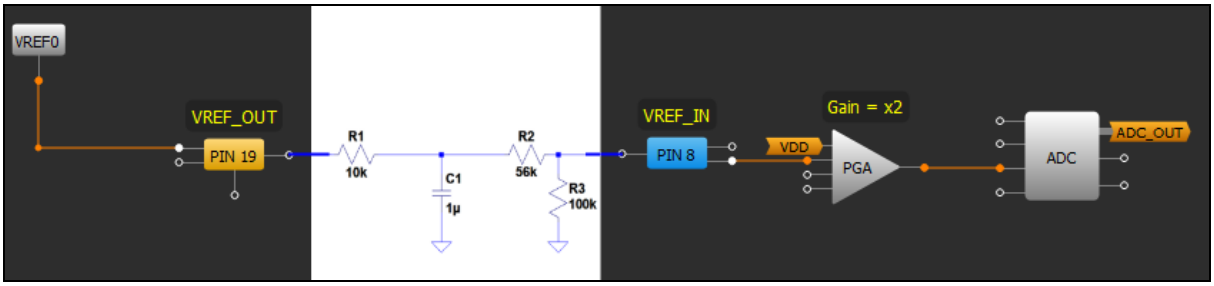

Figure 13 shows how a voltage divider connected to the filter in Figure 8 compensates for this difference. In this case, the PGA gain was set to x2. For simplicity, the resistor voltage divider could be replaced with a potentiometer for small adjustments.

Experimental results

Figure 14, shows proof of functionality for a 1Mhz input signal. The yellow signal is the input, and the blue signal is the output. Notice that the duty cycle of the output signal is 50%. Furthermore, by using a potentiometer instead of the voltage divider in

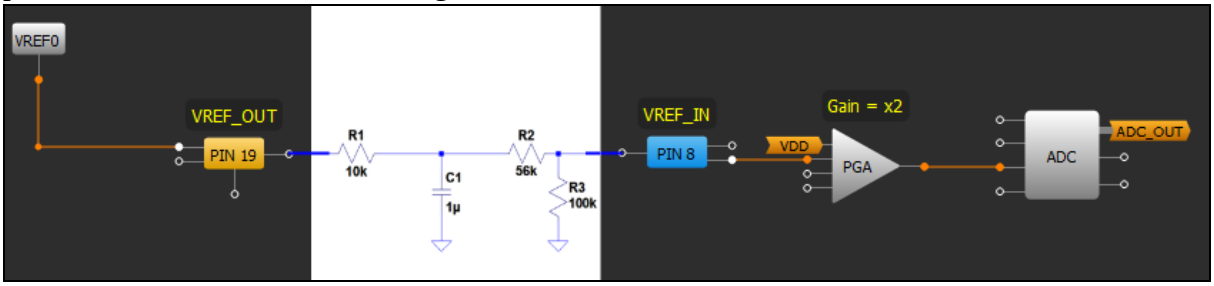

Figure 13, any duty cycle can be obtained.

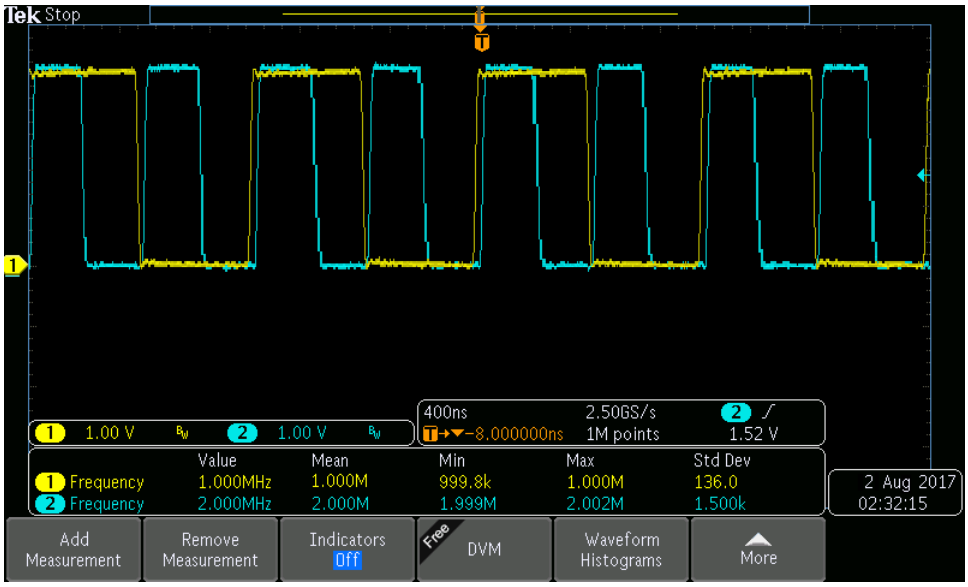

Figure 14. Results waveform

Note: The measurements were done with a Tektronix MDO 3034 oscilloscope.

How to test the circuit

Pin 6	The input frequency
Pin 19	The DAC's output – filter input
Pin 8	The ADC input
Pin 16	The output

In order to test the circuit, apply a square wave to Pin 6. The analog filter and the potentiometer should be connected between PIN 8 and PIN 19. The output on Pin 16 should be twice the frequency of the input signal, and should have a 50% duty cycle.

Conclusions

In this app note, we discussed a practical method to double the frequency of a clock signal while ensuring a 50% duty cycle. This technique only requires a few passive external components. Thanks to the low-cost of the GreenPAK SLG46621, this design would be cheaper than other solutions, like using voltage controlled oscillators. Moreover, this design doesn't introduce a lot of noise like a classic PLL that uses a very high frequency synthesis. To obtain higher frequencies, several of these circuits could be stacked in series. The output frequency will always be a power of two multiplied y the reference signal, but it cannot exceed 3MHz. For a low frequency signal, a larger number of multiplications would be possible.

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