Introduction

This application note describes how to design a circuit to control autoranging of a volt/current meter. Using the GreenPAK4 SLG46621V's onboard ADC, counters, comparators, and logic blocks, automatic adjustment of the measurement range ("autoranging") is possible without MCU intervention, allowing for faster and more reliable signal scaling while freeing up MCU resources. This article focuses on two autoranging examples: low-side current sensing using an array of shunt resistors, and dynamically attenuating a voltage input to a simple voltmeter. However, other configurations are possible, such as varying the gain of a digitally-controlled instrumentation amplifier such as the AD8250.

Autoranging is used when an application requires the accurate measurement of a voltage signal whose range spans several orders of magnitude, so the measurement process is more involved than simply routing the signal to an ADC.

Using a high-resolution ADC (16 bits or more) may be prohibitively expensive or impractical for the application, and even then it may still be insufficient to span the breadth of the measurement range. And in a system where the microprocessor must attend to many tasks, it may be impractical to burden it with monitoring the signal, adjust the gain/attenuation to scale the signal, and dedicating more I/O pins. Timers and digital filtering may also be required to prevent overly frequent toggling between ranges. For these reasons, using a GreenPAK in the design becomes prudent.

Autoranging Load Monitor

Consider a variable DC load drawing current I_{Load}, as shown in Figure 1, where I_{Load} is measured by passing it through a shunt resistor and measuring the voltage drop. The shunt resistor is placed between the load and ground. Consider a scenario in which the load current can span four or more orders of magnitude.

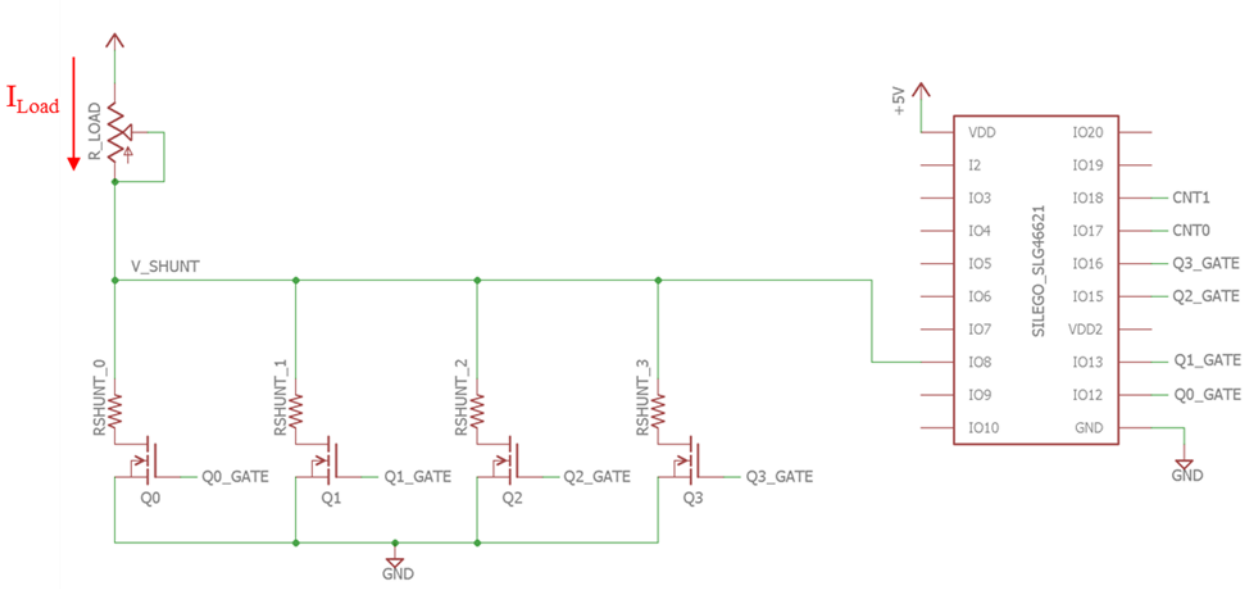

Figure 1. Autoranging ammeter test circuit

Consequently, there are four shunt resistors in parallel, each with its own low-side nMOSFET switch. Only one of the shunt resistors is "on" at any given time. The gates of the nMOS switches are connected to I/O pins of the GreenPAK SLG46621V. Note that Figure 1 does not show the SPI connections from the microcontroller to the SLG46621V, which are used to read the ADC output.

Current is monitored by measuring the voltage on the high side of the shunt resistor, VShunt. This voltage is connected to the analog input channel (pin 8) of the SLG46621V. As shown in Figure 2, the GreenPAK's internal PGA multiplies VShunt and feeds it to the single-ended input of the internal ADC. The objective is to control the nMOS switches based on the output value of the ADC.

This is accomplished in two stages. First, as shown in Figure 3, section A, the ADC output is routed to digital comparators DCMP0 and DCMP1. These compare the ADC output to predefined values stored in non-volatile memory.

These values define a window in which VShunt may reside without triggering a change of range. Once VShunt has crossed the upper or lower bound of this window, the shunt resistor must be switched out for another of lesser or greater value.

When the ADC output exceeds the upper bound in COMP0, COMP0's output ("Count up") goes high. When the ADC value is less than the lower bound in COMP1, COMP1's output ("Count down") goes low. If either "Count up" goes high or "Count down" goes low, this triggers DLY1 (see section B in Figure 3). Appendix A shows the values for LUT4. After DLY1 has counted up to its internal limit, its output goes high. Its output is fed back to LUT11 (contents shown in Appendix A), which resets DLY1's input to zero. This resets DLY1's output to zero. The result is a single low-high-low pulse that occurs after either "Count up" goes high or "Count down" goes low, plus a short delay.

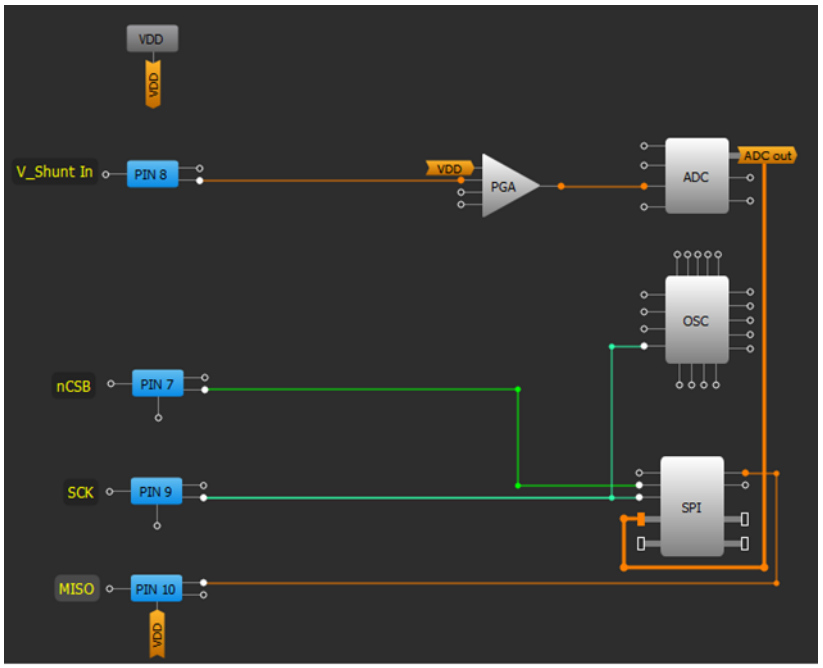

Figure 2. Part 1 of the SLG46621V's internal connection diagram

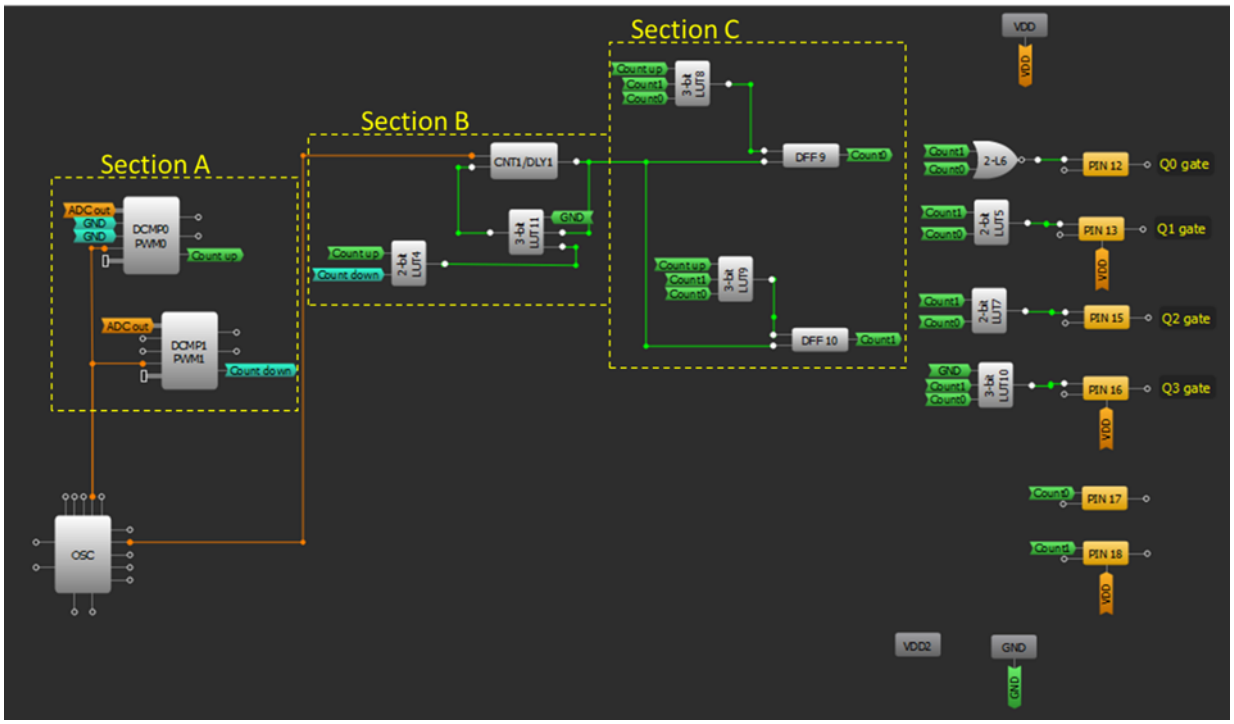

Figure 3. Part 2 of the SLG46621V's internal connection diagram

The next section consists of two DFF's and two LUT's arranged to make a two-bit up/down counter (see section C in Figure 3). DLY1's output is fed to the counter's clock input. The single-pulse output of DLY1 increments or decrements the counter by one step, depending on the state of "Count up." If "Count up" is high, the 2-bit counter will increment. If "Count down" is low, then "Count up" must be low, and so the 2-bit counter will decrement. The counter logic is configured such that it does not wrap around from b11 to b00, or vice-versa. Appendix A shows the values of LUT8 and LUT9. The counter's contents control output pins 12, 13, 15, and 16, which turn the nMOS switches on and off. A counter value of b00 turns on only switch Q0, a value of b01 turns on only switch Q1, and so forth.

Design equations

There are several parameters that must be fixed for the circuit to operate: the shunt resistor values, the reference values of DCMP0 and DCMP1, the PGA gain, and the value of DLY1. The relationship between the load current and the input to pin 8 is:

$$I_{Load} = \frac{V_{Shunt}}{R_{Shunt,i}}$$

I_{Load} = Load current

$R_{Shunt,\ i}$ = Shunt resistance of resistor *i*, where *i* is the current range, and $0 \leq i \leq 3$.

The relationship between the ADC output and the load current is:

$$ADC\ output = \frac{I_{Load} \times R_{Shunt,i} \times PGA\ gain\ \times 2^m}{V_{Ref}}$$

V_{Ref} = ADC reference voltage = 1.2V;

m = ADC resolution = 8 bits.

Therefore, the upper and lower load current boundaries for each current range are:

$$I_{Load\ Lower\ Bound,i} = \frac{V_{Ref} \times N_{COMP1}}{R_{Shunt,i} \times PGA\ gain \times 2^m}$$

$$I_{Load\ Upper\ Bound,i} = \frac{V_{Ref} \times N_{COMP0}}{R_{Shunt,i} PGA\ gain \times 2^m}$$

$I_{Load\ Lower\ Bound,\ i}$ = Load current that triggers the circuit to switch from range *i* to range *i – 1*;

$I_{Load\ Upper\ Bound,\ i}$ = Load current that triggers the circuit to switch from range *i* to range *i + 1;*

N_{COMP0} = Comparator 0 reference value;

N_{COMP1} = Comparator 1 reference value.

Table 1 shows the upper and lower current load current boundaries for each current range.

Notice that the upper and lower bounds in DCMP0 and DCMP1 were chosen such that the current ranges for each of the shunt resistors overlap. These overlapping areas form hysteresis bands, so that a load current at the edge of a range boundary does not cause the current range to toggle rapidly between the two adjacent ranges. DLY1 works in conjunction with the hysteresis bands to prevent rapid range toggling. It acts as a filter to block out currents that cross the range boundaries only momentarily. The value of the delay counter maximum and the delay's clock source can be adjusted to match the needs of the application.

DCMP0 reference (N_{COMP0}) = 15 DCMP1 reference (N_{COMP1}) = 240 PGA gain = 8			
Current range	**Shunt resistance**	**Lower boundary**	**Upper boundary**
0 (b00)	1kΩ	8.8µA	140µA
1 (b01)	100Ω	88µA	1.4mA
2 (b10)	10Ω	880µA	14mA
3 (b11)	1Ω	8.8mA	140mA

Table 1. Upper and lower load current boundaries for each current range

Figure 4 shows the relationship between I_{Load}, V_{Shunt}, and current range. The blue curves in Figure 4 correspond to an upward sweep of I_{Load}, and the red curves correspond to a downward sweep of I_{Load}. As I_{Load} increases, V_{Shunt} increases proportionally until it crosses the upper threshold of 0.14V at 140µA, at which point the range increments from 0 (b00) to 1 (b01), and the shunt resistor changes from 1kΩ to 100Ω. Similar transitions occur at 1.4mA and 14mA. During the downward sweep, the transition between range 3 (b11) and 2 (b10) occurs at V_{Shunt} = 0.0088V and I_{Load} = 8.8mA. Similar transitions occur at 880µA and 88µA. The hysteresis bands are the shaded regions bounded by the upward and downward sweeps.

Note in Figure 2 that the ADC output is also routed to the SPI shift register, so that a master SPI device can read the ADC value at any given time. Similarly, the contents of the two-bit up/down counter (Count0 and Count1) can be read on pins 17 and 18. All the microcontroller needs to measure the load current is to fetch the ADC value via SPI, read the digital values on pins 17 and 18, and multiply the ADC output by the calibration constant corresponding to the current range.

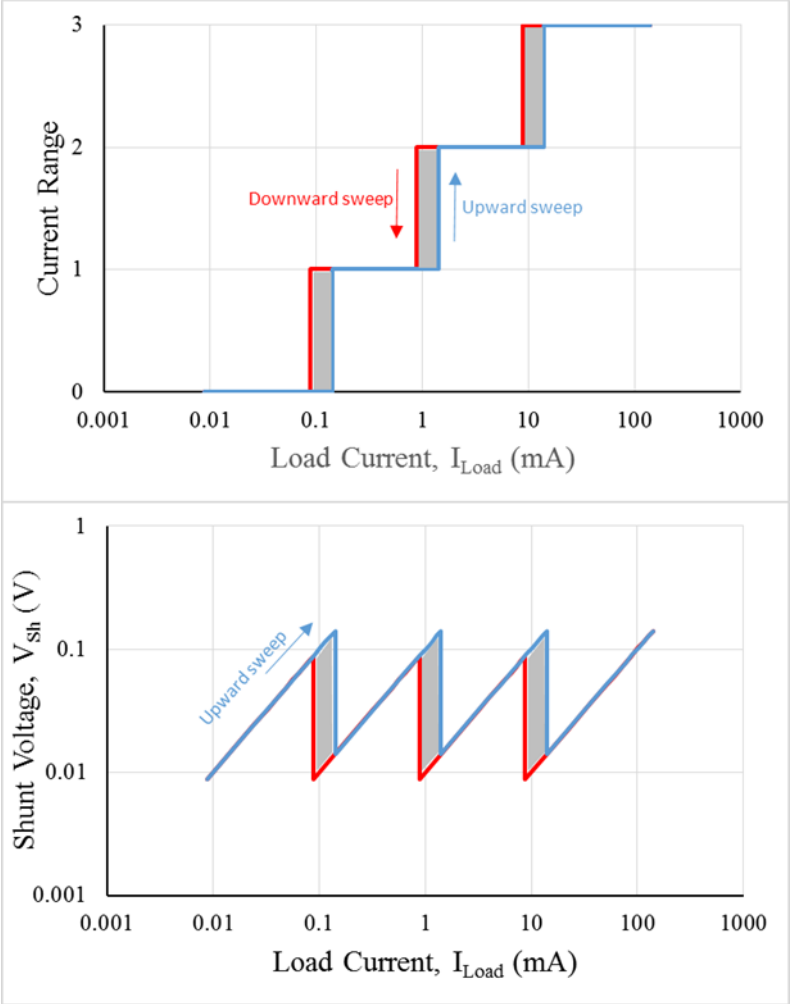

Figure 4. Shunt voltage (V_{Shunt}) and current range as functions of load current (I_{Load})

Autoranging Voltmeter

Implementing an autoranging voltmeter is possible using the same SLG46621V configuration, with some minor changes to the external components. Figure 5 shows the autoranging voltmeter test circuit, where the measured voltage V_{meas} passes through a voltage divider consisting of a 10MΩ upper resistor and one of three lower resistors, labeled V_{Div1} through V_{Div3}. A fourth resistor V_{Div0} with infinite resistance can be imagined to be in parallel with the other three lower resistors. The attenuation values for each of the resistors is shown in Table 2.

Resistor	Resistor value	Attenuation through voltage divider
R_{Div0} (virtual)	Infinite resistance	1
R_{Div1}	1000kΩ	0.091
R_{Div2}	100kΩ	0.0099
R_{Div3}	10kΩ	0.001

Table 2. Resistance and divider attenuation values for RDiv0 – RDiv4

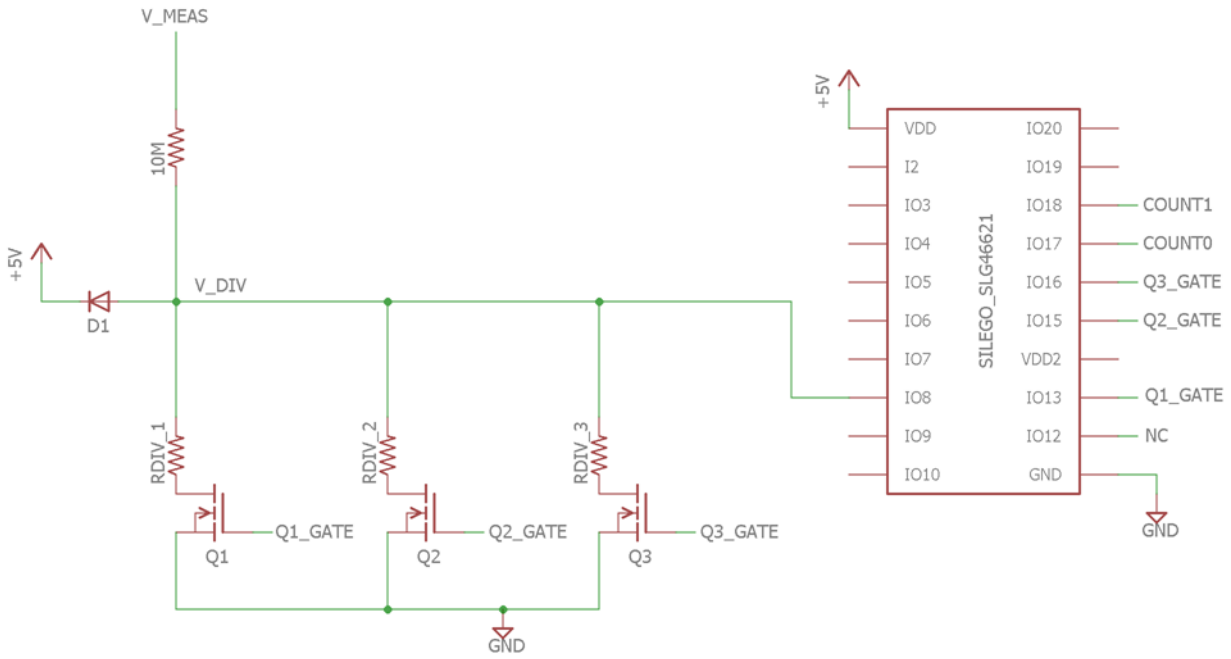

Figure 5. Autoranging voltmeter test circuit

The internal connections of the SLG46621V are the same as with the autoranging ammeter. The analog input is routed through the PGA to the ADC. The ADC output is compared to upper and lower reference boundaries in DCMP0 and DCMP1, which trigger a pulse into an up/down counter. The up/down counter controls which nMOS switch is on and which attenuation value is selected.

The design equations are similar to those corresponding to the autoranging ammeter circuit:

$$ADC\ output = \frac{V_{Meas} \times R_{Div,i} \times PGA\ gain\ \times 2^m}{(R_{Div,i} + 10M\Omega)V_{Ref}}$$

V_{Meas} = Voltage input to the voltage meter

$R_{Div,i}$ = Resistance of the lower arm of the voltage divider for attenuation range *i*, where 0 ≤ i ≤ 3

$$V_{Meas\ Lower\ Bound,i} = \frac{V_{Ref} \times N_{COMP1} \times (R_{div,i} + 10M\Omega)}{PGA\ gain \times 2^m \times R_{div,i}}$$

$$V_{Meas\ Upper\ Bound,i} = \frac{V_{Ref} \times N_{COMP0} \times (R_{div,i} + 10M\Omega)}{PGA\ gain \times 2^m \times R_{div,i}}$$

Table 3 shows the upper and lower voltage limits for each attenuation range.

Figure 6 shows the relationships between V_{Meas}, the attenuation range, and V_{Div}. The graphs look very similar to those shown in Figure 4, and hysteresis bands can be seen between the curves corresponding to the upward and downward sweeps.

DCMP0 reference (N_{COMP0}) = 15 DCMP1 reference (N_{COMP1}) = 240 PGA gain = 8			
Attenuation range	**$R_{Div,i}$**	**V_{Meas} lower boundary**	**V_{Meas} Upper boundary**
0 (b00)	Infinite resistance	8.8mV	140mV
1 (b01)	1000kΩ	97mV	1.5V
2 (b10)	100kΩ	890mV	14V
3 (b11)	10Ω	8.8V	140V

Table 3. Upper and lower boundaries of V_{Meas} for each attenuation range

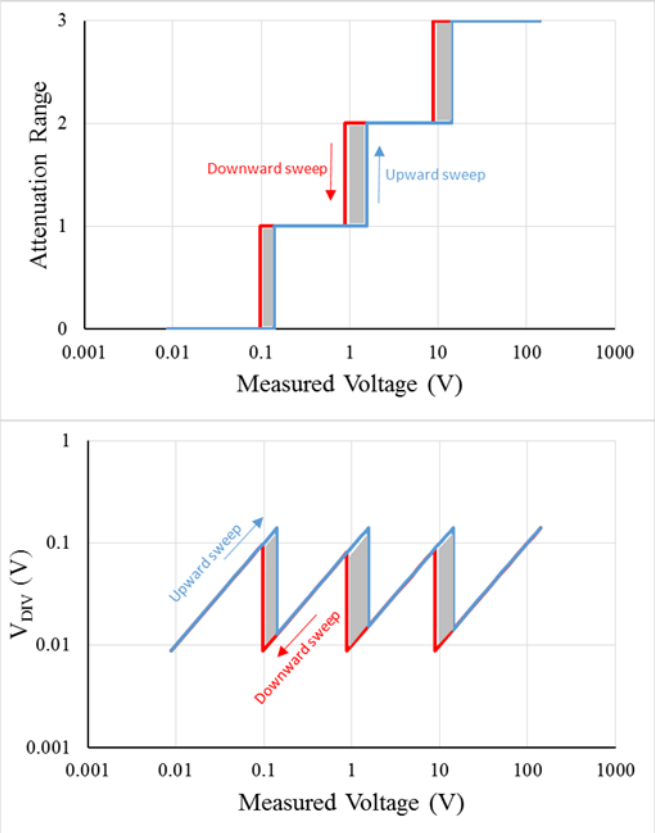

Figure 6. Attenuation range and V_{Div} as functions of V_{Meas}

Conclusion

A GreenPAK mixed-signal IC with an onboard ADC can be made to automate the ranging of voltage signals, freeing the microcontroller to attend to other tasks. Autoranging is important in many applications where a voltage that spans several orders of magnitude must be accurately measured. This application note shows how circuitry for autoranging ammeter and voltmeter may be constructed.

Appendix

2-bit LUT4

IN3	IN2	IN1	IN0	OUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1

2-bit LUT4 properties

3-bit LUT8

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1

3-bit LUT8 properties

3-bit LUT9

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1

3-bit LUT9 properties

3-bit LUT11

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0

3-bit LUT11 properties

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