

During negative gain calibration, the “negative full scale” voltage is supplied to the input of the converter. After completing a conversion, the Negative Gain Coefficient Register is updated with offset corrected data for this voltage. This data is a negative two’s complement number which is used to calculate a gain correction factor for all negative input voltages.

The order of the gain coefficient generation is not important but the offset coefficient must be generated before either of the gain coefficients. For proper calibration, the gain coefficients must have offset error removed before storage in memory. The flow chart below describes a proper method for generating the converter calibration coefficients using the system inputs.

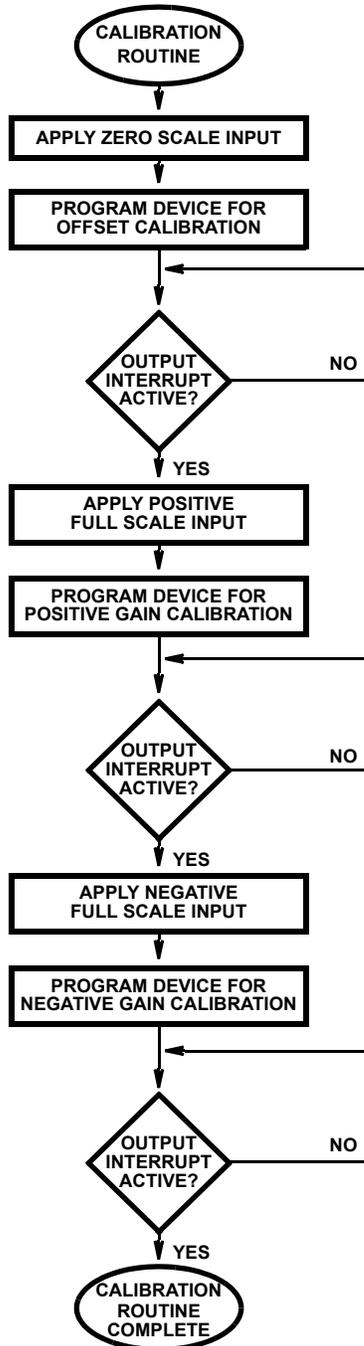


FIGURE 2.

Calibrating Conversion Results

In normal operating mode, every conversion is followed by a data calibration phase. Data calibration is as follows:

1. Offset is subtracted.
2. The polarity of the offset corrected data is determined and the proper gain correction factor is generated.
3. The offset calibrated data is multiplied by the gain correction factor generated in step two. This completes gain calibration.
4. The offset corrected data is checked for over or under range error before final coding (two’s complement, offset binary or, in unipolar mode, binary).

The calibrated, coded data is stored in memory and the user is notified of a completed conversion via an output interrupt signal.

Offset Calibration

Offset Calibration is a simple two’s complement subtraction. Each conversion has offset error removed by subtracting the contents of the Offset Correction Register from the digital filter output.

Gain Calibration

Gain calibration is a two step process. First, the proper gain correction factor is generated. Then this factor is multiplied by the offset corrected data, completing gain calibration.

The gain correction factor is generated via the divider (N/D) shown in Figure 1. After offset calibration has been completed, the converter determines which gain coefficient to use for generation of the gain correction factor. If the offset corrected data is positive, the positive gain coefficient is the denominator when determining the gain correction factor. If the offset corrected data is negative, the two’s complement of the negative gain coefficient is the denominator when determining the gain correction factor.

The input span (numerator), used to generate the gain correction factor is different for bipolar versus unipolar mode. In unipolar mode the calibration logic determines the gain correction factor by dividing the total internal resolution of the converter (2^N) by the span between the zero scale and positive full scale points. In bipolar mode the gain factor is determined by dividing one half the total internal resolution (2^{N-1}) of the converter by the span between the zero scale (bipolar midscale) and \pm full scale points.

In either unipolar or bipolar mode, the division result is the gain correction factor and is multiplied by the offset corrected filter output to calculate the proper digital output of the converter. The gain correction factor is not permanently stored but is generated for each conversion. The Gain Correction Factor Register is not accessible via the serial interface.

Range Detection

In addition to the calibration process, the converter detects over range above positive full scale and under range below minus full scale conditions. Over or under range detection affects the output data coding as described in the Data Coding section.

Over range detection is identical for both bipolar and unipolar operation. Over range is detected by comparing the offset corrected filter output to the positive gain coefficient. If the current offset corrected filter value is greater than the positive gain coefficient, an over range condition is detected.

In unipolar mode, under range is detected by sampling the sign bit of the offset calibrated data. If the sign bit is logic 1, signifying a negative voltage, an under range condition exists.

In bipolar mode, under range is detected by comparing the offset corrected filter output to the negative gain coefficient. If the current offset corrected filter value is less than the negative gain coefficient, an under range condition is detected.

Data Coding

The calibrated data can be obtained in one of various numerical codes depending on the bipolar/unipolar mode bit and the two's complement coding bit. In bipolar mode, if the two's complement bit is true, the output is two's complement. In bipolar mode, offset binary coding is used when the two's complement coding bit is not true. In unipolar mode, only binary coding is available and the two's complement coding bit is a don't care.

The output coding tables for the HI719X 24-bit family of products is shown below. V_{ZS} represents the applied zero scale input during system calibration or is AGND if internal calibration was performed. V_{PFS} represents the applied positive full scale input during system calibration or is V_{REF} if internal calibration was performed. V_{NFS} represents the applied negative full scale input during system calibration or is $-V_{REF}$ if internal calibration was performed.

TABLE 1. BIPOLAR MODE OUTPUT CODES 24-BIT

INPUT VOLTAGE	TWO'S COMPLEMENT CODE	OFFSET BINARY CODE
$>(V_{PFS} - 1.5 \text{ LSB})$	7FFFFFFF	FFFFFFF
$V_{PFS} - 1.5 \text{ LSB}$	7FFFFFFF/7FFFFFFE	FFFFFFF/FFFFFFE
$V_{ZS} - 0.5 \text{ LSB}$	000000/FFFFFFF	800000/7FFFFFFF
$V_{NFS} + 0.5 \text{ LSB}$	800001/800000	000001/000000
$<(V_{NFS} + 0.5 \text{ LSB})$	800000	000000

TABLE 2. UNIPOLAR MODE DATA OUTPUT CODES 24-BIT

INPUT VOLTAGE	BINARY CODE
$>(V_{PFS} - 1.5 \text{ LSB})$	FFFFFFF
$V_{PFS} - 1.5 \text{ LSB}$	FFFFFFF/FFFFFFE
$V_{PFS}/2 - 0.5 \text{ LSB}$	800000/7FFFFFFF
$V_{ZS} + .5 \text{ LSB}$	000001/000000
$<(V_{ZS} + 0.5 \text{ LSB})$	000000

When the range detection logic determines an over range, the converter output will clamp at the $>(V_{PFS} - 1.5 \text{ LSB})$ output as described in Table 1 or 2. When the range detection logic determines an under range, the converter output will clamp at the $<(V_{NFS} + 0.5 \text{ LSB})$ output described in Table 1 or the $<(V_{ZS} + 0.5 \text{ LSB})$ output described in Table 2.

Additional Notes

The calibration logic can be effectively bypassed by writing the Offset Correction Register to 000000 (hex) and the Gain Coefficient registers to 800000 (hex). This forces zero offset correction and a gain correction factor of 1.

The Offset Correction Register and the two Gain Coefficient registers are read/write accessible via the device serial interface.

The HI719X and HI718X products support an ability to ignore the negative gain coefficient when generating the gain correction factor. Each product has the ability to use only the positive gain coefficient when determining the gain correction factor. This feature is not recommended, but has been included to maintain compatibility with industry standard converters. In unipolar mode the negative gain coefficient is not used and does not require generation.

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