

# How to Drive PLL from Oscillator SLG47910V

## Abstract

This application shows how to drive the PLL either from the Oscillator or from the external clk (GPIO2) using the SLG47910 ForgeFPGA and Development Board. This application note comes complete with design files which can be found in the Reference Section.

## Contents

1. Terms and Definitions .....	1
2. Reference.....	2
3. Introduction .....	2
3.1 PLL connections .....	2
3.2 Signal Description.....	2
3.2.1. Inputs - Clock & Control Inputs .....	2
3.2.2. Clock & Control Outputs.....	3
4. Ingredients.....	4
5. Verilog Code.....	4
6. Floorplan: CLB Utilization.....	6
7. Design Steps .....	6
8. Conclusion .....	8
9. Revision History .....	9

## 1. Terms and Definitions

CLB	Configuration Logic Block
HDL Editor	Workspace where Verilog code is entered
FPGA	Field Programmable Gate Array
FPGA Editor	Main FPGA design and simulation window
Go Configure Software Hub	Main window for device selection
ForgeFPGA Window	Main FPGA project window for debug and IO programming
PLL	Phase Locked Loop
OSC	Oscillator

## 2. Reference

For related documents and software, please visit:

[ForgeFPGA Low-density FPGAs | Renesas](#)

Download our free ForgeFPGA™ Designer software [1] to open the .ffpga files [2] and view the proposed circuit design.

[1] [Go Configure Software Hub, Software Download and User Guide](#)

[2] [AN-FG-006 How to drive PLL from Oscillator.ffpga](#), ForgeFPGA Design File

[3] SLG47910, Preliminary Datasheet, Renesas Semiconductor

## 3. Introduction

### 3.1 PLL connections

The SLG47910 includes a low-power, wide input, and output Phase-Locked Loop (PLL) for use in applications requiring various frequencies.

The Phase Locked Loop (PLL) can be operated via two clock sources, the internal frequency from the oscillator (50 MHz) or the external clock, routed through GPIO2 pin. The PLL\_REF\_CLK\_SEL input signal is used to select between the two clock sources for PLL.

When the PLL\_REF\_CLK\_SEL signal is LOW, then the clock input to PLL is from the 50MHz OSC via REF\_CLK\_OSC. When the PLL\_REF\_CLK\_SEL signal is HIGH, then the clock input to the PLL is from an external clock from GPIO 2 via REF\_CLK\_EXT.

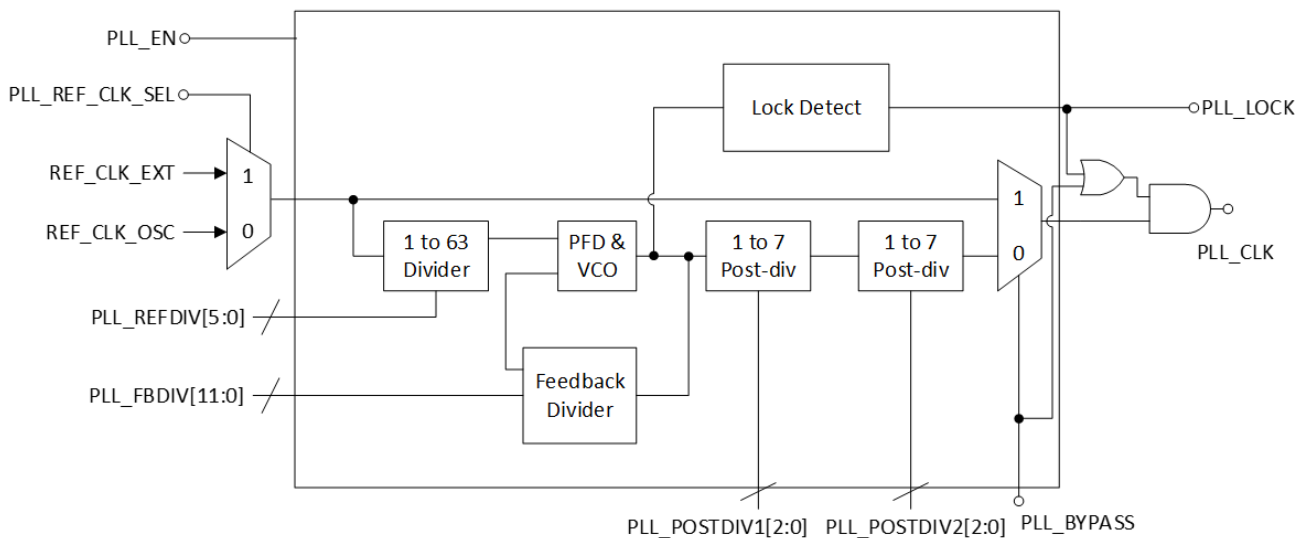


Figure 1: System Design

### 3.2 Signal Description

#### 3.2.1. Inputs - Clock & Control Inputs

Clock and control inputs determine the input clock source and intended output frequency.

**PLL\_REF\_CLK\_SEL** – Selects the PLL Input Clock source between the internal 50 MHz OSC or an external clock, originating from GPIO2. When LOW the clock input to the PLL is the OSC.

**PLL\_BYP** – BYP is an active HIGH signal that asserts a direct path between the clock input and PLL\_CLK.

**PLL\_REFDIV [5:0]** – Sets the reference divide value from 1 to 63.

**PLL\_FBDIV [11:0]** – Sets the PLL Feedback Divide value from 16 to 400.

**PLL\_POSTDIV1[2:0] & PLL\_POSTDIV2[2:0]** – The two stages of post-dividers are used to divide down the VCO Frequency before the PLL\_FOUT clock output. Each Post-divider has options for division from 1 to 7. Total post divide is POSTDIV1\*POSTDIV2.

### 3.2.2. Clock & Control Outputs

**PLL\_CLK** – PLL output clock(Depending on the Lock state of PLL)

**PLL\_LOCK** – Indicates the number of cycle slips between the feedback clock and the Phase Frequency Detector for 256 consecutive cycles.

**PLL\_EN** (Input) – Power-on for PLL. Active HIGH.

The behavior of the SLG47910's PLL is to receive a reference frequency and either divide or multiply the frequency value per the following equation, where  $f_{\text{reference\_clock}}$  is the reference frequency of the external clock source (GPIO2) or 50 MHz OSC, chosen through PLL\_REF\_CLK\_SEL:

$$FOUT = \frac{f_{\text{reference}} \times FBDIV}{REFDIV \times POSTDIV1 \times POSTDIV2}$$

Using larger values for the variables in the numerator and denominator will reduce clock jitter at the expense of increased current consumption. Below is the table specifying the different values of FBDIV, REFDIV & POSTDIV when  $f_{\text{reference}}$  is set to 50MHz

Table 1: PLL FOUT Values

FREF (MHz)	REFDIV	FBDIV	POSTDIV1	POSTDIV2	PLL_FOUT (MHz)
50	2	32	5	4	40
50	3	40	7	7	13.6
50	1	16	4	2	100

The FOUT values will be correct and achievable only for valid values of FBDIV, REFDIV and POSTDIV values.

The PLL\_BYP Signal is an active HI signal. When the PLL\_BYP signal is set as 1, then the PLL\_CLK signal runs at the frequency directly from either REF\_CLK\_EXT or REF\_CLK\_OSC. However, when the PLL\_BYP is set as 0, then the PLL\_CLK value is assigned according to the Equation above and Table 1.

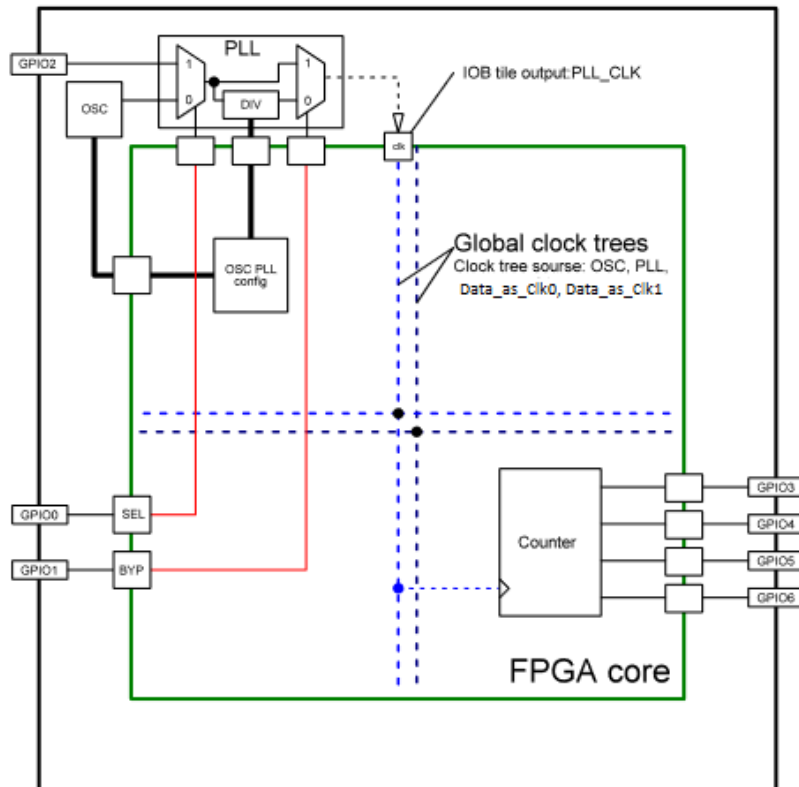


Figure 2: Block diagram of the design

## 4. Ingredients

- SLG47910 Device
- FPGADEVPAK Development Board with USB cable and power supply
- FPGAPAK Socket Adaptor Board
- Latest Revision of ForgeFPGA Workshop software

## 5. Verilog Code

Shown below is the (\*top\*) module named counter\_4bit\_pll. The Verilog code for How to drive PLL can be found in the complete design example. It is available for download ([AN-FG-006 Drive PLL from Oscillator.ffpga](#))

```
// AN-003 How to drive PLL from OSC
```

```
(* top *) module counter_4bit_pll (
  //CLK
  (* iopad_external_pin, clkbuf_inhibit *) input pll_clk,
  //POR
  (* iopad_external_pin *) input nreset,
  //OSC
  (* iopad_external_pin *) output OSC_CTRL_EN,
  //PLL
  (* iopad_external_pin *) input sel,//GPIO0
  (* iopad_external_pin *) input byp,//GPIO1
  // Selects the PLL Input Clock source between the internal 50MHz OSC and an
  external clock.
  (* iopad_external_pin *) output PLL_REF_CLK_SELECTION,
  // BYP is an active HI signal that asserts a direct path between the clock input
  and FOUT.
```

```
(* iopad_external_pin *) output PLL_CTRL_BYPASS, PLL_CTRL_EN,
// Sets the reference divide value from 1 to 63.
(* iopad_external_pin *) output [5:0] PLL_CTRL_REFDIV,
// Sets the PLL Feedback Divide value from 16 to 400.
(* iopad_external_pin *) output [11:0] PLL_CTRL_FBDIV,
// Sets the PLL Output Dividers values from 1 to 7.
(* iopad_external_pin *) output [2:0] PLL_CTRL_POSTDIV1, PLL_CTRL_POSTDIV2,
(* iopad_external_pin *) output reg [3:0] counter ,
(* iopad_external_pin *) output counter_oe0,
(* iopad_external_pin *) output counter_oe1,
(* iopad_external_pin *) output counter_oe2,
(* iopad_external_pin *) output counter_oe3
);

//OE's settings
assign counter_oe0 = 1'b1;
assign counter_oe1 = 1'b1;
assign counter_oe2 = 1'b1;
assign counter_oe3 = 1'b1;

//OSC settings
assign OSC_CTRL_EN = 1'b1; // Oscillator operates at 50MHz

//PLL settings
assign PLL_CTRL_EN = 1;
assign PLL_CTRL_BYPASS = byp;
assign PLL_REF_CLK_SELECTION = sel;
assign PLL_CTRL_REFDIV = 1;
assign PLL_CTRL_FBDIV = 20;
assign PLL_CTRL_POSTDIV1 = 5;
assign PLL_CTRL_POSTDIV2 = 2;

reg nrst;

always @(posedge pll_clk) begin
    nrst <= nreset;
end

//Counter
always @(posedge pll_clk) begin
    if (!nrst)
        counter <= 4'h0;
    else
        counter <= counter + 4'h1;
    end
endmodule
```

## 6. Floorplan: CLB Utilization

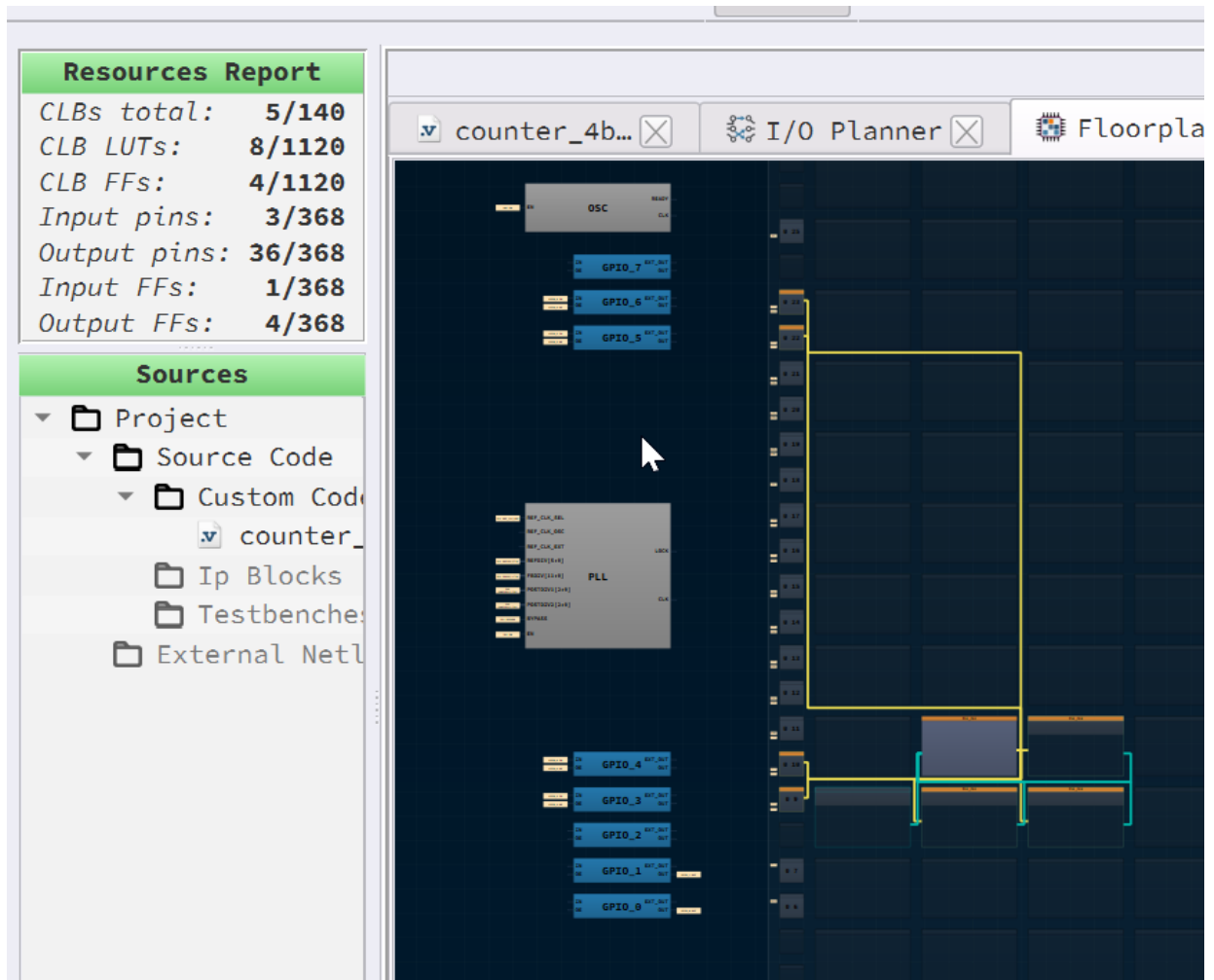


Figure 3: Floorplan

The Floorplan tab in the FPGA Editor shows the placement of the CLBs, FFs and their connections to IOB blocks.

## 7. Design Steps

1. Launch the latest version of the Go Configure Software Hub. Select the SLG47910V device and the ForgeFPGA Workshop software will load.
2. Download the design example [AN-FG-006 Drive PLL from Oscillator.ffpga](#). If you are not familiar with the ForgeFPGA Workshop software, review the Four-Bit Counter application notes that covers the basic design steps.
3. Open the [AN-FG-006 Drive PLL from Oscillator.ffpga](#) file after downloading.
4. Open the FPGA editor and review the Verilog code. There is a main code with the module name counter\_4bit\_pll which is the top module defining the whole design.
5. Open the IO planner tab on the FPGA editor and review the pin assignment.
6. Next select the Synthesize button on the lower left side of the FPGA editor.
7. Select the Generate Bitstream button on the lower left side of the FPGA editor. Check the Logger and Issues tabs to make sure that the bit stream was generated correctly.
8. Now click on the Floorplan tab and see the CLB utilization (Figure 3). Press the Ctrl and the mouse wheel to zoom-in. Confirm that the IOs selected in the IO Planner are shown in the floorplan

9. Connect the Development Board and attach it to Adaptor Board with the SLG47910 part in the socket on it. Click on the Debug button on the ForgeFPGA Workshop studio (Figure 5) and select Emulation.

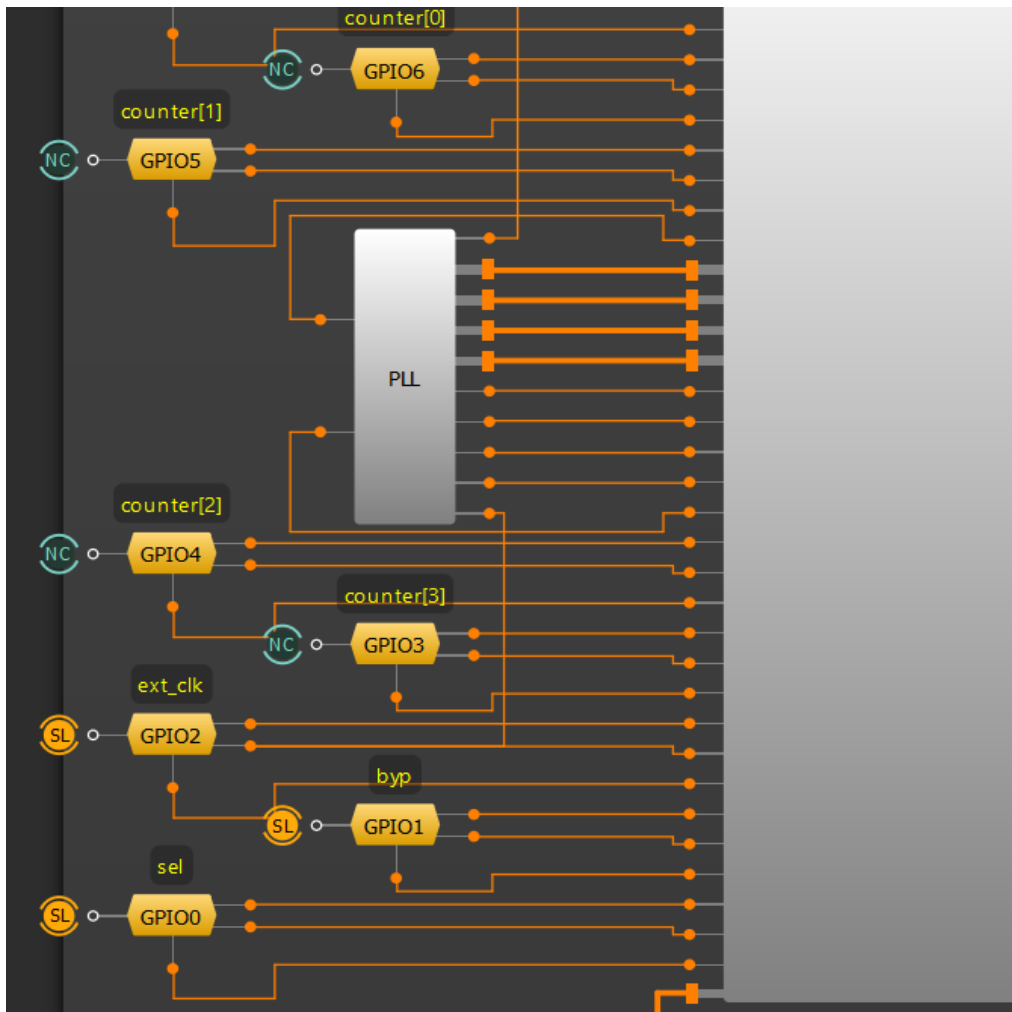


Figure 5: GPIO Connections to generate waveform during Emulation

10. Connect the GPIO2 to the Synchronous Logic Generator, Configure GPIO0 and GPIO1 as buttons or synchronous Logic Generators to function as sel and byp signals for PLL\_REF\_CTRL\_SEL and BYP\_SEL and then observe the output from GPIO3, GPIO4, GPIO5 and GPIO6 on logic analyzer. In Figure 6 it can be observed that when there is a change in the sel and byp signals, then there is a corresponding change in the frequency of the switching of the counter depicting that the PLL is being driven by 2 different clock sources.

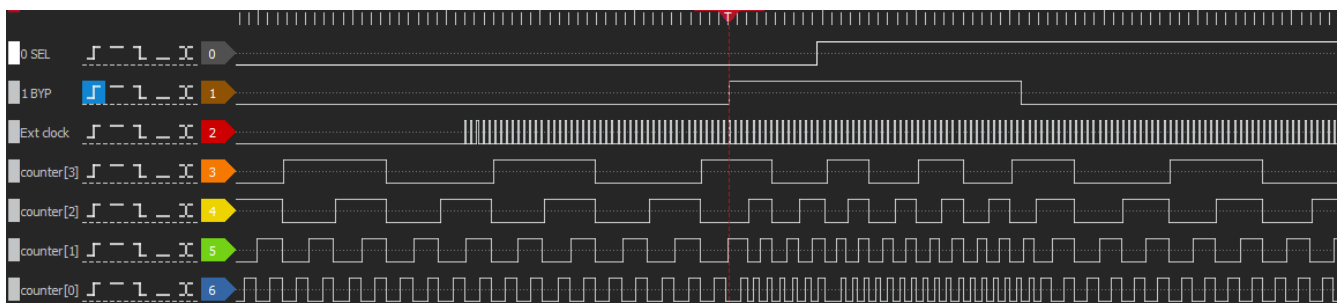


Figure 6: Change in sel and byp line to produce PLL\_CLK of different frequencies

### 8. Conclusion

This application note shows how to drive the PLL using an External Clock (GPIO2) via REF\_CLK\_EXT or using the internal Oscillator on board via REF\_CLK\_OSC. This application note also focuses on how to set the values of different PLL parameters to achieve the desirable frequency when BYP is set to 0. This procedure can be utilized for any design. This testcase is available for download ([AN-FG-006 Drive PLL from Oscillator.fpga](#)). If interested, please contact the ForgeFPGA Business Support Team.



## 9. Revision History

Revision	Date	Description
1.00	Mar 3, 2022	Initial release.
2.0	Feb 22, 2024	Updated changes according to BB revision

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.