Boost Converter Generates +5V at 375mA from Wide Range Negative Input Supply

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Author: Mike Wong

Sometimes only a negative power source is available but a positive voltage is desired. Using a standard boost converter IC, a positive voltage can be generated from the negative source. The boost converter is designed to generate an output voltage higher than the input voltage. Since the positive output voltage, 5V in this example, is higher than the negative input voltage ground level, the boost converter principle is not violated. Figure 1 shows the circuit implementation using the EL7515, a standard boost converter IC. The ground pins of the boost converter connect to the negative input source; ground becomes the "positive" input source. V_{OUT} is determined by:

$$V_{OUT} = -VFB \times \left(\frac{R_2}{R_1}\right) = -1.33V \times \left(\frac{37.5k}{10k}\right) = -5V$$

The Q_1 and Q_2 PNP transistor forms a translator that scales the +5V output voltage referenced to ground to a feedback voltage referenced to negative input. The transistor pair also eliminates temperature change and voltage drop effects. As the negative input voltage decreases, Q_2 runs at a higher current than Q_1 causing additional transistor offset mismatch. For optimal line regulation, one should set Q_1 and Q_2 to operate at the same current as the nominal input voltage. Figure 2 shows line regulation results. The maximum output to input voltage difference must be within the boost converter internal power FET drain to source breakdown voltage (Vds). The EL7515 maximum Vds is 18V. For +5V output, the minimum input voltage is -12V. 1V safety margin compensates for the D1 diode drop and any voltage spikes on the drain of the power FET. Figure 3 shows the load regulation test results. The maximum output current is determined by the input to output voltage ratio and the current limit setting of the boost converter. As shown in Figure 4, this circuit yields over 80% efficiency at 200mA output.

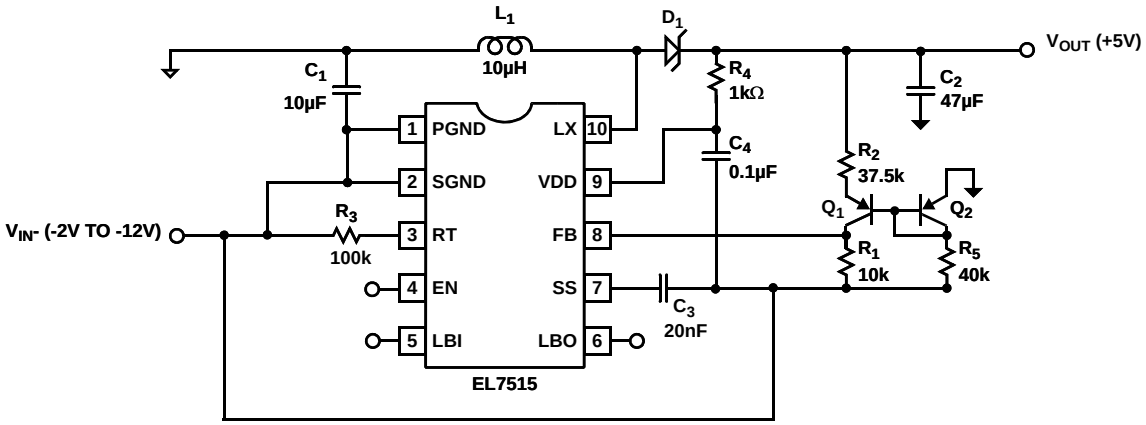

FIGURE 1. CIRCUIT SCHEMATIC

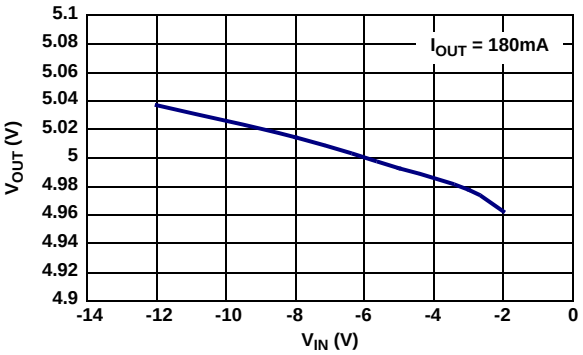

FIGURE 2. LINE REGULATION

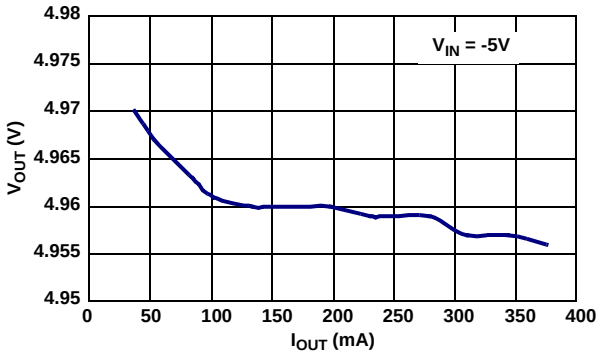

FIGURE 3. LOAD REGULATION

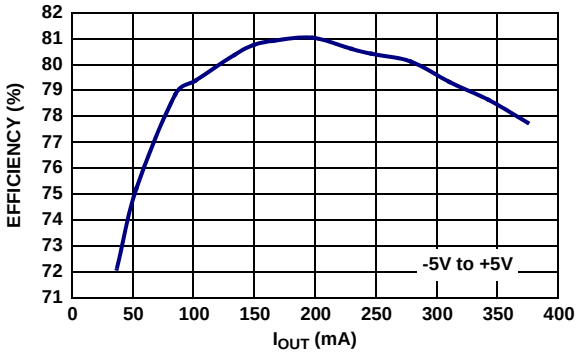

FIGURE 4. EFFICIENCY vs I_{OUT}