RENESAS Tool News

RENESAS TOOL NEWS on September 16, 2007: 070916/tn3

A Note on Using the Simulator Debugger V.9.07.00 for the SuperH RISC engine MCU Family

Please take note of the following problem in using the simulator debugger V.9.07.00 for the SuperH RISC engine MCU family:

- With using the SH2A-FPU simulator

1. Description

In the SH2A-FPU simulator for pipeline simulation, the number of execute cycles becomes incorrect as follows:

(1) The number of execute cycles up to the third instruction after reset is counted less.
(2) When memory space whose type of memory in the memory map* is "EXT" or "I/O" is accessed, 1 is added to the number of execute cycles every time of memory access.

*To reference the memory map, open the Simulator System dialog box and click the Memory tab.

2. Workarounds

2.1 Case (1) in Section 1

Add the following value to the cycle count provided in the Status or Trace window:

Value to be added
= (number of read states in type of memory where 1st instruction resides)
+ (number of states** for memory access made by 1st instruction)
+ (number of states** for memory access made by 2nd instruction)

+ (number of states** for memory access made by 3rd instruction)

**In the instructions that access memory, the number of states is that of read or write states to or from the type of memory concerned. If no memory access is made, the number of states is 0.

2.2 Case (2) in Section 1

When the type of memory is "EXT" or "I/O", set the number of read or write states in the Set Memory Map dialog box to the user calculated cycle value minus 1.

3. Schedule of Fixing the Problem

We plan to fix this problem in the next release of the product.
