

RENESAS TOOL NEWS on November 16, 2011: 111116/tn4

Corrections to HI7300/PX V.1.01 User's Manual (Real-Time OS for SuperH Family)

We inform you about corrections to the User's Manuals of HI7300/PX V.1.01, a real-time OS for the SuperH family of MCUs.

1. Manual Concerned

Title: HI7300/PX V.1.01 User's Manual (Rev.2.00)

Document No.: REJ10J1198-0200

2. Corrections

1. In page 408, delete the last 2 items of the TCAC list. To be deleted are as follows:
 - TCAC_L2_ENABLE (H'00010000)
Setting this value enables the level-2 cache (RAMCR.L2E = 1); otherwise, the level-2 cache is disabled (RAMCR.L2E = 0).
 - TCAC_L2_FC (H'00020000)
Setting this value selects the level-2 cache forcible coherency mode (RAMCR.L2FC = 1); otherwise, the level-2 cache forcible coherency mode is not selected (RAMCR.L2FC = 0).
2. In page 408, delete the first sentence of the paragraph that follows the above list. To be deleted is as follows:
Do not specify TCAC_L2_ENABLE or TCAC_L2_FC if the microcomputer being used does not support the level-2 cache.

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