Customer Notification

V850E/PHO3

32-Bit Single-Chip Microcontrollers

Operating Precautions

μPD70F3441
μPD70F3483

Renesas Electronics
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Table of Contents

(A) Table of Operating Precautions

No.	Outline		μPD70F3441		μPD70F3483
		Rev.	ES 1.0	ES 2.0	
		Rank[Note]			
1	INTDEDF interrupt is misleadingly generated (Technical limitation)		✘	✔	✔
2	CSIB master mode stop condition (Technical limitation)		✘	✔	✔
3	Unintended protection of flash blocks when applying the permanent boot block cluster protection (Specification change notice)		✘	✘	✘
4	FlexRay: Register RCV displays wrong value. (Specification change notice)		✘	✘	✘
5	FlexRay: After reception of a valid sync frame followed by a valid non-sync frame in the same static slot the received sync frame may be ignored. (Specification change notice)		✘	✘	✘
6	FlexRay: Sync frame overflow flag EIR.SFO may be set if slot counter is greater than 1024. (Specification change notice)		✘	✘	✘
7	FlexRay: Acceptance of startup frames received after reception of more than gSyncNodeMax sync frames. (Specification change notice)		✘	✘	✘
8	FlexRay: Initial rate correction value of an integrating node is zero if pMicroInitialOffsetA,B = 0x00. (Specification change notice)		✘	✘	✘
9	FlexRay: Incorrect rate and/or offset correction value if second Secondary Time Reference Point (STRP) coincides with the action point after detection of a valid frame. (Specification change notice)		✘	✘	✘
10	FlexRay: Flag SFS.MRCS is set erroneously although at least one valid sync frame pair is received. (Specification change notice)		✘	✘	✘
11	FlexRay: Rate correction set to zero in case of SyncCalcResult=MISSING_TERM. (Specification change notice)		✘	✘	✘
12	FlexRay: A sequence of received WUS may generate redundant SIR.WUPA/B events. (Specification change notice)		✘	✘	✘
13	Input voltage level of MODE1 (FLMD0) pin restricted. (Specification change notice)		✘	✘	✘

No.	Outline		μPD70F3441		μPD70F3483
		Rev.	ES 1.0	ES 2.0	
		Rank[Note]			
14	ADC: When reading the ADCRnm registers asynchronously the conversion result from previous channel might be provided. (Specification change notice)		✘	✘	✘

✔ :Not applicable

✘ :Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

(B) Description of Operating Precautions

No. 1	INTDEDF interrupt is misleadingly generated (Technical limitation)

Detail

On execution of a special code sequence from flash memory a misleading Double Error Detection interrupt INTDEDF may be generated respectively in case interrupt sharing is enabled (INTSEL.ISR = 1_b) a NMI interrupt is generated. The INTDEDF interrupt will occur only once, as the status of INTERRF.INTERR0 must be cleared to re-enable further INTDEDF interrupts.

As a consequence the Double Error Detection mechanism of the flash can not be used.

Special code sequence which generates the INTDEDF interrupt:

- 1st instruction:
  Any load instruction (LD, SLD)

- 2nd instruction
  Any branch instruction (Bcond, JARL, JMP, JR) or
  a jump to the interrupt handler due to an interrupt request

Example:

```
ld.w   0x1004[r0], r19
jmp    r20
```

Workaround

None. Do not use the Double Error Detection mechanism of the flash.

No. 2	CSIB master mode stop condition (Technical limitation)

Detail

When any channel of CSIB is operated in master mode (CB*n*CTL1.CKS[2:0]≠111_b) with CB*n*CTL1.CB*n*DAP=0_b (*n=0,1*) the CSIB may stop operating.

In transmit mode (CB*n*CTL0.CB*n*TXE=1_b, CB*n*RXE=0_b) any write to the related CB*n*TX0 register will no longer start a transmission sequence. Furthermore the related transmission interrupt request will not be generated.

In transmit/receive mode (CB*n*CTL0.CBnTXE=1_b, CB*n*RXE=1_b) any write to the related CB*n*TX0 register will no longer start a transmission/reception sequence. Furthermore the related transmission/reception interrupt request will not be generated.

In receive mode (CB*n*CTL0.CB*n*TXE=0_b, CB*n*CTL0.CB*n*RXE=1_b) any read from the related CB*n*RX0 register will no longer start a receive sequence. Furthermore the related receive interrupt request will not be generated.

The described CSIB*n* stop condition can be escaped by initiating a system reset or by a sequential clear and set of the CB*n*CTL0.CB*n*PWR bit.

The aforementioned condition does not occur when CB*n*CTL1.CB*n*DAP=1_b.

Workaround

To overcome CSIB master mode stop condition apply either of the following workarounds:

- Do not use CSIB in master mode with CB*n*CTL1.CB*n*DAP=0_b.
- Initiate a system reset, or clear and set the CB*n*CTL0.CB*n*PWR bit in case CSIB stops operating.

No. 3	Unintended protection of flash blocks when applying the permanent boot block cluster protection (Specification change notice)

Detail

Enabling the boot block cluster protection feature to permanently lock the boot block against any kind of update or manipulation (write/erase) may result in unintended protection of additional flash blocks not being part of the boot block cluster itself.

Such unintended protection may occur under the following conditions:

- Operation Mode
  - Single chip mode (self-programming)
  - Flash programming mode
- Boot block cluster settings
  - Boot block cluster area is less than 512kB
  - Boot block cluster protection is enabled

If above conditions are met any attempt to erase a flash block outside the boot block cluster starting with or including address 80000h will fail and result in erase errors.

Workaround

Do not enable the boot block cluster protection at all.
Or: When using the boot block cluster protection feature do not apply the block erase function to blocks starting with or including address 80000h

No. 4	FlexRay: Register **RCV** displays wrong value. (Specification change notice)

Description

If the calculated rate correction value is in the range of [-pClusterDriftDamping .. +pClusterDriftDamping], vRateCorrection of the CSP process is set to *zero*. In this case register **RCV** should be updated with this value. Erroneously **RCV.RCV[11:0]** holds the calculated value in the range [-pClusterDriftDamping .. +pClusterDriftDamping] instead of *zero*.

Scope

The erratum is limited to the case where the calculated rate correction value is in the range of [-pClusterDriftDamping .. +pClusterDriftDamping].

Effects

The displayed rate correction value **RCV.RCV[11:0]** is in the range of [-pClusterDrift-Damping .. +pClusterDriftDamping] instead of *zero*. The error of the displayed value is limited to the range of [-pClusterDriftDamping .. +pClusterDriftDamping]. For rate correction in the next double cycle always the correct value of *zero* is used.

Workaround

A value of **RCV.RCV[11:0]** in the range of [-pClusterDriftDamping .. +pClusterDriftDamping] has to be interpreted as zero.

Severity: (low, medium, high)

Low, no impact on rate correction, workaround available.

Classification

Non Critical Error

No. 5	FlexRay: After reception of a valid sync frame followed by a valid non-sync frame in the same static slot the received sync frame may be ignored. (Specification change notice)

Description

If in a static slot of an even cycle a valid sync frame followed by a valid non-sync frame is received, and the frame valid detection (prt_frame_decoded_on_X) of the DEC process occurs one sclk after valid frame detection of FSP process (fsp_val_syncfr_chx), the sync frame is not taken into account by the CSP process (devte_xxs_reg).

Scope

The erratum is limited to the case where more than one valid frame is received in a static slot of an even cycle.

Effects

In the described case the sync frame is not considered by the CSP process. This may lead to a SyncCalcResult of MISSIMG_TERM (error flag **SFS.MRCS** set). As a result the POC state may switch to NORMAL_PASSIVE or HALT or the Startup procedure is aborted.

Workaround

Avoid static slot configurations long enough to receive two valid frames.

Severity: (low, medium, high)

Low, this problem does not occur with typical configurations.

Classification

Non Critical Error

No. 6	FlexRay: Sync frame overflow flag **EIR.SFO** may be set if slot counter is greater than 1024. (Specification change notice)

Description

If in the static segment the number of transmitted and received sync frames reaches gSyncNodeMax and the slot counter in the dynamic segment reaches the value cStaticSlotIDMax + gSyncNodeMax = 1023 + gSyncNodeMax, the sync frame overflow flag **EIR.SFO** is set erroneously.

Scope

The erratum is limited to configurations where the number of transmitted and received sync frames equals to gSyncNodeMax and the number of static slots plus the number of dynamic slots is greater or equal than 1023 + gSyncNodeMax.

Effects

In the described case the sync frame overflow flag **EIR.SFO** is set erroneously. This has no effect to the POC state.

Workaround

Configure gSyncNodeMax to number of transmitted and received sync frames plus one or avoid configurations where the total of static and dynamic slots is greater than cStaticSlotIDMax.

Severity: (low, medium, high)

Low, workaround available, the erroneous setting of **EIR.SFO** has no influence on the protocol

operation state.

Classification

Non Critical Error

No. 7	FlexRay: Acceptance of startup frames received after reception of more than gSyncNodeMax sync frames. (Specification change notice)

Description

If a node receives in an even cycle a startup frame after it has received more than gSyncNodeMax sync frames, this startup frame is added erroneously by process CSP to the number of valid startup frames (zStartupNodes). The faulty number of startup frames is delivered to the process POC. As a consequence this node may integrate erroneously to the running cluster because it assumes that it has received the required number of startup frames.

Scope

The erratum is limited to the case of more than gSyncNodeMax sync frames.

Effects

In the described case a node may erroneously integrate successfully into a running cluster.

Workaround

Correct configuration with all startup frames placed in the first static slots.

Severity: (low, medium, high)

Low, only appears in case of faulty configurations where the number of sync nodes configured in a cluster is greater than gSyncNodeMax (**GTUC2.SNM[3:0]**).

Classification

Non Critical Error

No. 8	FlexRay: Initial rate correction value of an integrating node is *zero* if pMicroInitialOffsetA,B = 0x00. (Specification change notice)

Description:

The initial rate correction value as calculated in figure 8-8 of protocol spec v2.1 is *zero* if parameter pMicroInitialOffsetA,B was configured to be *zero*.

Scope:

The erratum is limited to the case where pMicroInitialOffsetA,B is configured to *zero*.

Effects:

Starting with an initial rate correction value of *zero* leads to an adjustment of the rate correction earliest 3 cycles later (see figure 7-10 of protocol spec v2.1). In a worst case scenario, if the whole cluster is drifting away too fast, the integrating node would not be able to follow and therefore abort integration.

Workaround:

Don’t configure pMicroInitialOffsetA,B to *zero*. A configuration of pMicroInitialOffsetA,B = 0x01instead of the calculated value *zero* will delay the start of the node by only one microtick but leads to a correct initial rate correction value.

Severity: (low, medium, high)

Low, workaround available.

Classification:

Non Critical Error

No. 9	FlexRay: Incorrect rate and/or offset correction value if second Secondary Time Reference Point (STRP) coincides with the action point after detection of a valid frame. (Specification change notice)

Description

If a valid sync frame is received before the action point and additionally noise or a second frame leads to a STRP coinciding with the action point, an incorrect deviation value of *zero* is used for further calculations of rate and/or offset correction values.

Scope

The erratum is limited to configurations with an action point offset greater than static frame length.

Effects

In the described case a deviation value of *zero* is used for further calculations of rate and/or offset correction values. This may lead to an incorrect rate and/or offset correction of the node.

Workaround

Configure action point offset smaller than static frame length.

Severity: (low, medium, high)

Low, with typical configurations the action point offset is much smaller than the static frame length. With such configurations no valid frame can be received before action point.

Classification

Non Critical Error

No. 10	FlexRay: Flag **SFS.MRCS** is set erroneously although at least one valid sync frame pair is received. (Specification change notice)

Description

If in an odd cycle 2c+1 after reception of a sync frame in slot n the total number of different sync frames per double cycle has exceeded gSyncNodeMax and the node receives in slot n+1 a sync frame that matches with a sync frame received in the even cycle 2c, the sync frame pair is not taken into account by CSP process. This may cause the flags **SFS.MRCS** and **EIR.CCF** to be set erroneously.

Scope

The erratum is limited to the case of a faulty cluster configuration where different sets of sync frames are transmitted in even and odd cycles and the total number of different sync frames is greater than gSyncNodeMax.

Effects

In the described case the error interrupt flag **EIR.CCF** is set and the node may enter either the POC state NORMAL_PASSIVE or HALT.

Workaround

Correct configuration of gSyncNodeMax.

Severity: (low, medium, high

Low, occurs only with invalid cluster configurations.

Classification

Non Critical Error

No. 11	FlexRay: Rate correction set to zero in case of SyncCalcResult=MISSING_TERM. (Specification change notice)

Description:

In case a node receives too few sync frames for rate correction calculation and signals a SyncCalcResult of MISSING_TERM, the rate correction value is set to zero instead to the last calculated value.

Scope:

The erratum is limited to the case where a node enters NORMAL_PASSIVE state (pAllowHaltDueToclock=false) because of receiving too few sync frames for rate correction calculation (SyncCalcResult=MISSING_TERM).

Effects:

In the described case a rate correction value of zero is applied in NORMAL_PASSIVE state instead of the last rate correction value calculated in NORMAL_ACTIVE state. This decreases the probability to re-enter NORMAL_ACTIVE state.

Workaround:

If NORMAL_PASSIVE state is entered due to missing sync frames, use higher level application software to leave this state and to initiate a re-integration into the cluster.

Severity: (low, medium, high)

Low, workaround available.

Classification:

Non Critical Error

No. 12	FlexRay: A sequence of received WUS may generate redundant SIR.WUPA/B events. (Specification change notice)

Description

If a sequence of wakeup symbols (WUS) is received, all separated by appropriate idle phases, a valid wakeup pattern (WUP) should be detected after every second WUS. The E-Ray detects a valid wakeup pattern after the second WUS and then after each following WUS.

Scope

The erratum is limited to the case where the application program frequently resets the appropriate SIR.WUPA/B bits.

Effects

In the described case there are more SIR.WUPA/B events seen than expected.

Workaround

Ignore redundant SIR.WUPA/B events.

Severity: (low, medium, high)

Low, workaround available.

Classification

Non Critical Error

No. 13	Input voltage level of MODE1 (FLMD0) pin restricted. (Specification change notice)

Description

The voltage input high level V_{IH} and voltage input low level V_{IL} of the MODE1 (FLMD0) pin as described in the data sheet differ from the true voltage input levels of the input buffer.

Effects

Instead of
$V_{IH(min)} = 0.7\ V_{DD3}$ and $V_{IL(max)} = 0.3\ V_{DD3}$
the correct limitations of the voltage input level are
$V_{IH(min)} = 0.8\ V_{DD3}$ and $V_{IL(max)} = 0.2\ V_{DD3}$

Thus the MODE1 (FLMD0) pin features the same voltage input range as the MODE0, MODE2 and $\overline{\text{RESET}}$ pin.

Workaround

None. Please check the applied voltage input levels for the MODE1 (FLMD0) pin of the concerned circuit layout.
The flash programmers PG-FP4 and PG-FP5 can be used without any restriction, since these devices apply appropriated voltage levels at the FLMD0 pin.

No. 14	ADC: When reading the ADCRnm registers asynchronously the conversion result from previous channel might be provided. (Specification change notice)

Details

When the A/D converter (ADC) is operating in scan mode and is stopped asynchronously (by clearing the ADCEn bit, rewriting of ADMn0/ADMn1/ADMn2 registers, or an enabled external or timer trigger event) the internal current ADCRnm master register might be loaded with the conversion result of the previous converted channel.
After AD conversion restart (by setting the ADCEn bit, or automatically after rewriting of ADMn0/ADMn1/ADMn2 registers, or by the enabled external or timer trigger event) the ADCRnm master register still holds the conversion result of the previous converted channel.
When the concerned conversion result register (ADCRnm) is read during the conversion time, the conversion result of the previous channel may be read, if at that time the internal ADCRSEL signal is active (for an ADC clock period of 62.5 ns).

Because of the small timing window (62.5 ns), a consecutive read of same ADCRnm register will never result in two invalid values.
When all specified channels are scanned once after reconfiguration, further reading of ADCRnm register will always return a valid value of the correspoding channel.

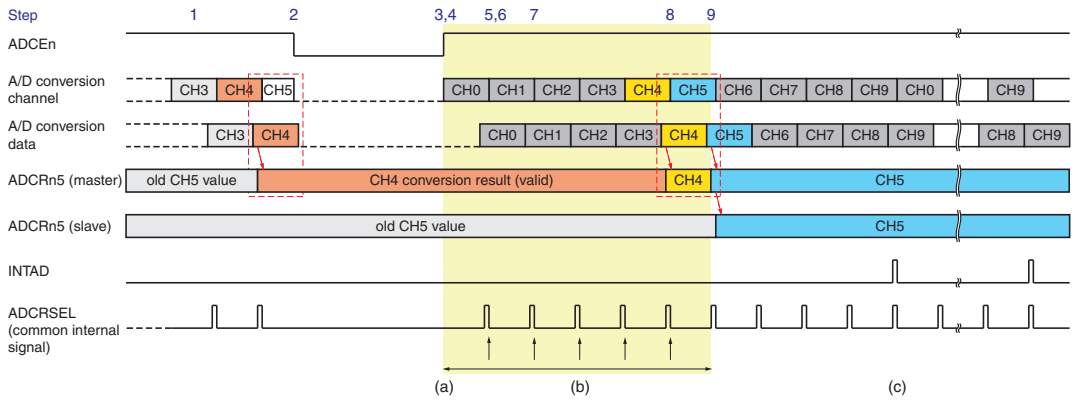
Example

1. AD conversion in SCAN mode (ADCE=1)
2. AD conversion stop (ADCE=0)
3. AD restart in SCAN mode (ADCE=1 and Trigger)
4. AD conversion of channel 0
5. AD conversion end of channel 0
6. AD conversion of channel 1
7. AD conversion end of channel 1

...

8. AD conversion of channel m
9. AD conversion end of channel m

When an ADCRnm register is read between steps 3 to 9, the result of the previous channel might be read until the conversion of the concerned channel has been finished the first time, e. g. ADCRn0 can be read properly from step 6 on.



No. 14	ADC: When reading the ADCRnm registers asynchronously the conversion result from previous channel might be provided. (Specification change notice)

(Example continued)

(a) Restart of A/D converter.
(b) For instance when ADCRn5 register is read after restart of the A/D converter during period (b) at the timing of an active ADCRSEL signal (1 x ADCLK = 62.5 ns), the conversion result may be read from ADCRn5 master register, which holds the result of the previous channel 4 at that time, rather than from the ADCRn5 slave register.
(c) After first INTADn occurrence, proper read of all ADCRnm registers is ensured.

Workaround

When the ADC is stopped asynchronously during scan mode operation apply one of the following three procedures when reading the conversion results after reconfiguration and restart of the ADC.

- Use DMA transfer to obtain AD conversion results (ADDMAn register).
- Read ADCRnm registers in a corresponding INTADn service routine.
- Synchronize the first read of ADCRnm registers with the first occurrence of the INTADn interrupt after restart of the ADC (without applying an interrupt service routine)
  - Clear ADICn.IF flag during reconfiguration and check ADICn.IF flag before reading the ADCRnm registers.
  - In case of external or timer trigger ensure that the period b/w two consecutive trigger events is greater than the scan period of all selected channels. (refer to precaution 15.8 (2) in UM)

Example

Example for synchronizing the first read of ADCRnm registers after the first occurrence of the INTADn interrupt (without applying an interrupt service routine):

```
Initialization/ Reconfiguration
...
// stop ADC
ADMn0.ADCEn = 0
// reconfigure ADC
...
// clear request flag & start ADC
ADICn.IF = 0
ADMn0.ADCEn = 1
...
```

```
Asynchronous read
...
// check request flag (or wait until it is set)
if (ADICn.IF == 1)
{
   // read ADCRnm registers
   ...
}
...
```

(C) Valid Specification

Item	Date published	Document No.	Document Title
1	February 2004	U14559EJ3V1UM00	V850E1 32-Bit Microprocessor Core Architecture (User's Manual)
2	November 2008	U16374EJ1V0UM00	V850E1 32-Bit Microprocessor Core Architecture (Floating Point Operation Unit) (User's Manual)
3	April 2010	U17754EE6V0UM00	V850E/PHO3 Hardware (User's Manual)

(D) Revision History

Item	Date published	Document No.	Comment
1	February 2007	EASE-CN-0018-0.1	First release of this document
2	July 2007	EASE-CN-0018-0.2	Adding of precautions no. 26 to 27
3	August 2007	EASE-CN-0018-0.3	Modified precaution no. 26 - CSIE 'Inconsistent read data in master mode" Corrected register setting for condition "Master mode enabled" from [CEnCTL0[2:0] <> 111b] to [CEnCTL1.CEnCKS[2:0] <> 111b]. Adding of precautions no. 28 to 37
4	April 2008	EASE-CN-0018-0.4	Adding of precautions no. 3 to 9 Transferring previous precautions no. 1to 30, 33 to 37 to user's manual U17754EE3V0UM00
5	June 2008	EASE-CN-0018-0.5	Precaution no.10 added.
6	July 2008	EASE-CN-0018-0.6	Transferring previous precautions no .3 to 9 to user's manual U17754EE4V0UM00 Adding of precautions no.4 to 12
7	December 2009	EASE-CN-0018-0.7	Adding μPD70F3483 to list of operating precautions Adding of precaution no. 13
8	Sep 14, 2010	R01TU0011ED0100	Adding of precaution no. 14

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