Date : Aug. 9, 2022

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0094A/E	Rev.	1.00
Title	User's Manual Hardware corrections for the division ratio setting of PLL1		Information Category	Technical Notification		
Applicable Product	RZ/G2L Group RZ/G2LC Group RZ/V2L Group RZ/G2UL Group RZ/A3UL Group RZ/Five Group	Lot No. All lots	Reference Document	RZ/G2L Group, RZ/G2LC Group, RZ/V2L Group User's Manual: Hardware Rev.1.10 RZ/G2UL Group, RZ/A3UL Group, RZ/Five Group User's Manual: Hardware Rev.1.00		

This technical update describes document corrections of the following User's Manual: Hardware.

RZ/G2L Group, RZ/G2LC Group User's Manual: Hardware Rev.1.10 (R01UH0914EJ0110)

RZ/V2L Group User's Manual: Hardware Rev.1.10 (R01UH0936EJ0110)

RZ/G2UL Group User's Manual: Hardware Rev.1.00 (R01UH0968EJ0100)

RZ/A3UL Group User's Manual: Hardware Rev.1.00 (R01UH0973EJ0100)

RZ/Five Group User's Manual: Hardware Rev.1.00 (R01UH0986EJ0100)

1. **Section 4. Boot Mode, 4.1 Overview**, the following description is added.

For RZ/G2L, RZ/G2LC RZ/V2L, RZ/G2UL

[From]

Once this LSI is released from the system reset state, the clock pulse generator (CPG) executes a specified sequence, and then Cortex-A55 Core 0 is started first to boot from the device selected according to the settings through the MD_BOOT2 to MD_BOOT0 pins. The values of the MD_BOOT2 to MD_BOOT0 pins are read once the LSI is released from the system reset state. After the LSI is booted up, the user program should enable or disable the operation of Cortex-A55 Core 0, Cortex-A55 Core 1, and Cortex-M33 as required.

[To]

Once this LSI is released from the system reset state, the clock pulse generator (CPG) executes a specified sequence, and then Cortex-A55 Core 0 is started first to boot from the device selected according to the settings through the MD_BOOT2 to MD_BOOT0 pins. The values of the MD_BOOT2 to MD_BOOT0 pins are read once the LSI is released from the system reset state. After the LSI is booted up, the user program should enable or disable the operation of Cortex-A55 Core 0, Cortex-A55 Core 1, and Cortex-M33 as required.
The CPG_PL1_DDIV register must be set when the user program starts.

For RZ/A3UL

[From]

Once this LSI is released from the system reset state, the clock pulse generator (CPG) executes a specified sequence, and then Cortex-A55 Core 0 is started first to boot from the device selected according to the settings through the MD_BOOT2 to MD_BOOT0 pins. The values of the MD_BOOT2 to MD_BOOT0 pins are read once the LSI is released from the system reset state.

[To]

Once this LSI is released from the system reset state, the clock pulse generator (CPG) executes a specified sequence, and then Cortex-A55 Core 0 is started first to boot from the device selected according to the settings through the MD_BOOT2 to MD_BOOT0 pins. The values of the MD_BOOT2 to MD_BOOT0 pins are read once the LSI is released from the system reset state.
The CPG_PL1_DDIV register must be set when the user program starts.

For RZ/Five

[From]

Once this LSI is released from the system reset state, the clock pulse generator (CPG) executes a specified sequence, and then AX45MP is started first to boot from the device selected according to the settings through the MD_BOOT2 to MD_BOOT0 pins. The values of the MD_BOOT2 to MD_BOOT0 pins are read once the LSI is released from the system reset state.

[To]

Once this LSI is released from the system reset state, the clock pulse generator (CPG) executes a specified sequence, and then AX45MP is started first to boot from the device selected according to the settings through the MD_BOOT2 to MD_BOOT0 pins. The values of the MD_BOOT2 to MD_BOOT0 pins are read once the LSI is released from the system reset state.

The CPG_PL1_DDIV register must be set when the user program starts.

2. **Section 7. Clock Pulse Generator (CPG), 7.4.6 Procedure for Switching the Division Ratio of the Dynamic Switching Frequency Dividers**, the following description is added.

For RZ/G2L, RZ/G2LC, RZ/V2L

[From]

7.4.6 Procedure for Switching the Division Ratio of the Dynamic Switching Frequency Dividers

Use the following procedure to set the division ratio of the dynamic switching frequency dividers.

* A sample procedure for DIV_PLL2_A is described here.

1) Confirming the DIV_PLL2_A state (checking that it is not busy)

- Check the following bit in the clock status monitor register (CPG_CLKSTATUS).
- DIV_PLL2_A state: Confirm that bit 0 (DIVPL2A_STS) = 0 (switching is completed).

Wait until the above condition is satisfied.

2) Setting the DIV_PLL2_A division ratio

- Set up the following bits in the division ratio setting (PLL2) register (CPG_PL2_DDIV).
- Setting of division ratio: Bits 1 and 0 (DIVPL2A_SET) = desired value and bit 16 (DIV_PLL2_A_WEN) = 1

3) Confirming the DIV_PLL2_A state (checking that it is not busy)

- Check the following bit in the clock status monitor register (CPG_CLKSTATUS).
- DIV_PLL2_A state: Confirm that bit 0 (DIVPL2A_STS) = 0 (switching is completed).

Wait until the above condition is satisfied.

The following registers are used in the above procedure.

— Division ratio setting (PLL2) register (CPG_PL2_DDIV)

— Division ratio setting (PLL3) register (CPG_PL3A_DDIV)

— Division ratio setting (PLL3) register (CPG_PL3B_DDIV)

— Division ratio setting (PLL6) register (CPG_PL6_DDIV)

The following status monitor register is used.

— Clock status monitor register (CPG_CLKSTATUS)

When 1 is written to a xx_WEN bit placed in the upper 16 bits of a division ratio setting register, the clock switching control begins even if the settings in the lower bits are not changed. Check the status monitor register (CPG_CLKSTATUS) and wait until the switching is completed. The clock will temporarily stop at the timing of switching.

[To]

7.4.6 Procedure for Switching the Division Ratio of the Dynamic Switching Frequency Dividers

Use the following procedure to set the division ratio of the dynamic switching frequency dividers.

* A sample procedure for DIV_PLL2_A is described here.

1) Confirming the DIV_PLL2_A state (checking that it is not busy)

- Check the following bit in the clock status monitor register (CPG_CLKSTATUS).
- DIV_PLL2_A state: Confirm that bit 0 (DIVPL2A_STS) = 0 (switching is completed).

Wait until the above condition is satisfied.

2) Setting the DIV_PLL2_A division ratio

- Set up the following bits in the division ratio setting (PLL2) register (CPG_PL2_DDIV).
- Setting of division ratio: Bits 1 and 0 (DIVPL2A_SET) = desired value and bit 16 (DIV_PLL2_A_WEN) = 1

3) Confirming the DIV_PLL2_A state (checking that it is not busy)

- Check the following bit in the clock status monitor register (CPG_CLKSTATUS).
- DIV_PLL2_A state: Confirm that bit 0 (DIVPL2A_STS) = 0 (switching is completed).

Wait until the above condition is satisfied.

The following registers are used in the above procedure.

— Division ratio setting (PLL1) register (CPG_PL1_DDIV)

— Division ratio setting (PLL2) register (CPG_PL2_DDIV)

— Division ratio setting (PLL3) register (CPG_PL3A_DDIV)

— Division ratio setting (PLL3) register (CPG_PL3B_DDIV)

— Division ratio setting (PLL6) register (CPG_PL6_DDIV)

The following status monitor register is used.

— Clock status monitor register (CPG_CLKSTATUS)

When 1 is written to a xx_WEN bit placed in the upper 16 bits of a division ratio setting register, the clock switching control begins even if the settings in the lower bits are not changed. Check the status monitor register (CPG_CLKSTATUS) and wait until the switching is completed. The clock will temporarily stop at the timing of switching.

For RZ/G2UL, RZ/A3UL, RZ/Five

[From]

7.4.6 Procedure for Switching the Division Ratio of the Dynamic Switching Frequency Dividers

Use the following procedure to set the division ratio of the dynamic switching frequency dividers.

* A sample procedure for DIV_PLL2_A is described here.

1) Confirming the DIV_PLL2_A state (checking that it is not busy)

- Check the following bit in the clock status monitor register (CPG_CLKSTATUS).
- DIV_PLL2_A state: Confirm that bit 0 (DIVPL2A_STS) = 0 (switching is completed).

Wait until the above condition is satisfied.

2) Setting the DIV_PLL2_A division ratio

- Set up the following bits in the division ratio setting (PLL2) register (CPG_PL2_DDIV).
- Setting of division ratio: Bits 1 and 0 (DIVPL2A_SET) = desired value and bit 16 (DIV_PLL2_A_WEN) = 1

3) Confirming the DIV_PLL2_A state (checking that it is not busy)

- Check the following bit in the clock status monitor register (CPG_CLKSTATUS).
- DIV_PLL2_A state: Confirm that bit 0 (DIVPL2A_STS) = 0 (switching is completed).

Wait until the above condition is satisfied.

The following registers are used in the above procedure.

— Division ratio setting (PLL2) register (CPG_PL2_DDIV)

— Division ratio setting (PLL3) register (CPG_PL3A_DDIV)

— Division ratio setting (PLL3) register (CPG_PL3B_DDIV)

The following status monitor register is used.

— Clock status monitor register (CPG_CLKSTATUS)

When 1 is written to a xx_WEN bit placed in the upper 16 bits of a division ratio setting register, the clock switching control begins even if the settings in the lower bits are not changed. Check the status monitor register (CPG_CLKSTATUS) and wait until the switching is completed. The clock will temporarily stop at the timing of switching.

[To]

7.4.6 Procedure for Switching the Division Ratio of the Dynamic Switching Frequency Dividers

Use the following procedure to set the division ratio of the dynamic switching frequency dividers.

* A sample procedure for DIV_PLL2_A is described here.

1) Confirming the DIV_PLL2_A state (checking that it is not busy)

- Check the following bit in the clock status monitor register (CPG_CLKSTATUS).
- DIV_PLL2_A state: Confirm that bit 0 (DIVPL2A_STS) = 0 (switching is completed).

Wait until the above condition is satisfied.

2) Setting the DIV_PLL2_A division ratio

- Set up the following bits in the division ratio setting (PLL2) register (CPG_PL2_DDIV).
- Setting of division ratio: Bits 1 and 0 (DIVPL2A_SET) = desired value and bit 16 (DIV_PLL2_A_WEN) = 1

3) Confirming the DIV_PLL2_A state (checking that it is not busy)

- Check the following bit in the clock status monitor register (CPG_CLKSTATUS).
- DIV_PLL2_A state: Confirm that bit 0 (DIVPL2A_STS) = 0 (switching is completed).

Wait until the above condition is satisfied.

The following registers are used in the above procedure.

— Division ratio setting (PLL1) register (CPG_PL1_DDIV)

— Division ratio setting (PLL2) register (CPG_PL2_DDIV)

— Division ratio setting (PLL3) register (CPG_PL3A_DDIV)

— Division ratio setting (PLL3) register (CPG_PL3B_DDIV)

The following status monitor register is used.

— Clock status monitor register (CPG_CLKSTATUS)

When 1 is written to a xx_WEN bit placed in the upper 16 bits of a division ratio setting register, the clock switching control begins even if the settings in the lower bits are not changed. Check the status monitor register (CPG_CLKSTATUS) and wait until the switching is completed. The clock will temporarily stop at the timing of switching.