To our customers,

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On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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GRADE A

RENESAS TECHNICAL NEWS

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Precautions Regarding the PWM Output Disable Function in the 32180 Group

Classification	Concerned Products
Corrections and supplementary explanation of document √ Notes Knowhow Others	32180 group

Content

If all of the conditions described below are met when the TOU output pin is set as a general-purpose port, one of the following register bits may inadvertently be cleared to 0:

- PO0DIS (P160/TO21–P165/TO26 output disable select) bit in the PWM Output 0 Disable Control Register (PO0DISCR)
- PO1DIS (P180/TO29–P185/TO34 output disable select) bit in the PWM Output 1 Disable Control Register (PO1DISCR)
- PO2DIS (P210/TO37–P215/TO42 output disable select) bit in the PWM Output 2 Disable Control Register (PO2DISCR)

(These bits basically are designed to be cleared by only writing a 0 in software.)

Occurrence conditions

The above problem occurs when all of the following conditions are met:

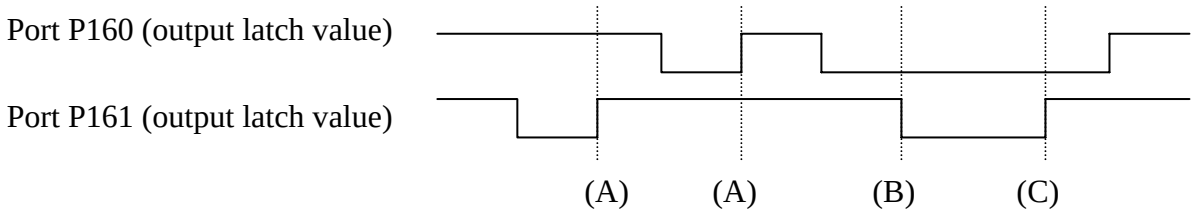
- The TOU output pin is set as a general-purpose port.[Note 1]
- The POxLVEN (output disable level enable/disable select) bits in the respective control registers are set to 1 (output disable level enabled):
  - PO0LVEN bit in the PWM Output 0 Disable Level Control Register (PO0LVCR)
  - PO1LVEN bit in the PWM Output 1 Disable Level Control Register (PO1LVCR)
  - PO2LVEN bit in the PWM Output 2 Disable Level Control Register (PO2LVCR)
- The output latch levels on ports P160–P165, P180–P185, and P210–P215 change in state simultaneously from where the PWM output disable condition is met to where it is not or vice versa.[Note 2]

Note 1: This also applies when either one of the control pins that disable PWM output is set for use as a general-purpose port. (For example, port P160 is used as timer output TO21 and port P161 as a general-purpose port.)

Note 2: For example, this applies to the case where the output latch level on port P160 and that on port P161 simultaneously change from high to low and low to high respectively.

Note: The pin level-triggered PWM output disable function is controlled by the output latch level on each port. Therefore, even while the port is being used in input mode, the above phenomenon may occur depending on the value written to the port data register.

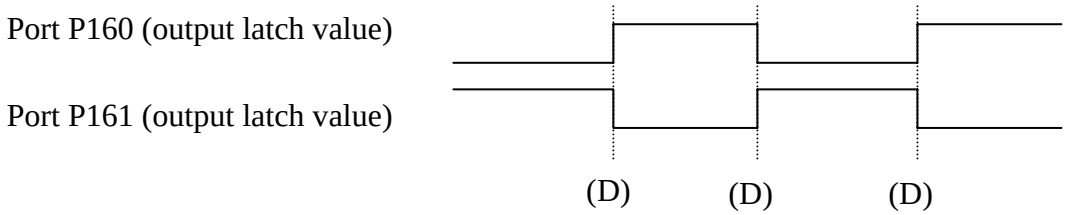
Example: When PWM output is disabled on condition that ports P160 and P161 are detected low at the same time.



(A): The anticipated phenomenon does not occur because the PWM output disable condition is not met.

(B): The PO0DIS (P160/TO21–P165/TO26 output disable select) bit is set to 1 because the PWM output disable condition is met.

(C): The PO0DIS (P160/TO21–P165/TO26 output disable select) bit may inadvertently be cleared to 0 by a change of states from where the PWM output disable condition is met to where it is not.



(D): The PWM output disable condition happens to be met due to a difference in output timing delays, causing the anticipated phenomenon to occur.

Countermeasures

- When using the pin level-triggered PWM output disable function, be sure to use the TOU output for control.
- When the TOU output pin is used as a general-purpose port and the POxLVEN (output disable level enable/disable select)bit has output disable level enabled, make sure to forbid the output latch levels on ports P160–P165, P180–P185, or P210–P215 to change in state from where the PWM output disable condition is met to where it is not. Or, if allowing such a change, check the status of the POxDIS (P160/TO21–P165/TO26, P180/TO29–P185/TO34, or P210/TO37–P215/TO42 output disable select) bit in software.