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On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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GRADE A

MESC TECHNICAL NEWS No.M16C-13-9802

Supplemental Description of DMAC for the M16C/60, M16C/61 and M16C/62 Group MCUs

1. Related devices

M16C/60, M16C/61 and M16C/62 groups

2. DMA enable bit

The DMA enable bit is bit 3 of both DMA0 and DMA1 control registers.
When the DMA enable bit is set to "1" the DMAC is in an active state and the following occurs:

a. The value of whichever of the source or destination pointer that is set up as the forward pointer is reloaded into the forward address pointer.
b. The value in the transfer counter reload register is reloaded into the transfer counter.

Therefore, the DMAC will start from the initial conditions once again if the DMA enable bit is set to "1" while in the active state.

3. DMA request bit

The DMA request bit is bit 2 of both DMA0 and DMA1 control registers.
Regardless of the DMAC status (enable bit set or clear), the request bit is set to "1" when a request signal for a DMA transfer occurs, based on the DMA request factor. The bit is cleared to "0" when data transfer begins. Further, the user can clear ("0") the DMA request bit but not set it.

It is possible that the DMA request bit may become "1" due to the DMA request cause select bits being changed. Therefore the DMA request bit should be cleared ("0") after changing the DMA request cause select bits.

If DMAC is in the active state (enable bit set) when the request bit becomes "1", the data transfer begins immediately. That in turn immediately causes the DMA request bit to be cleared ("0"). Therefore, to best judge the state of the DMAC, the DMA enable bit should be read instead of the request bit.

4. Initialization of DMA-related registers