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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A802A/E	Rev.	1.00
Title	SH7760 I2C Bus Interface Single Buffer Mode Master Transmitter Additional Restriction		Information Category	Technical Notification		
Applicable Product	SH7760 Group	Lot No. All lots	Reference Document	SH7760 Group Hardware Manual Rev.2.00 Feb. 12, 2010 (REJ09B0554-0200)		

There is an additional restriction of the SH7760 I2C single buffer mode master transmitter.

Note that this information is same as the previous manual of the SH7760 (ADE-602-291) section 19.7.1 Restriction 1 and 19.6.1 Master Transmitter (Single Buffer Mode) (4).

[Restriction]

For a master transmitter in single buffer mode, the following restriction should be taken into account. There is a restriction on a write of the second and following bytes to ICTXD register and a set of FSB to 1. Details are discussed it in the following paragraphs.

For details of master transmitter operation in single buffer mode, see 19.4.8, Master Transmitter Operation (Single Buffer Mode). This section mainly describes flag manipulation in relation to the restriction. Below shown are operational examples for transmission of one-byte, two-byte, and three-byte data. When two or more bytes are transmitted, writing of the second and third bytes is subject to the timing restriction. Meanwhile, single-byte data transmission has no timing restriction.

When transmitting three or more bytes, delay manipulation of the third byte transmission will remove the timing restriction on writing of the succeeding transmit bytes. (Transmission is stopped with the MDE flag being set to 1.)

(1) One-byte data transmission

Figure 1.1 shows an operational example of one-byte data transmission.

Write data 1 before clearing the MAT and MDE flags to 0 in (2) (for example, in initial setting preceding the issue of start conditions.). Once the MDE flag is cleared, data transmission starts. Set the FSB flag to 1 at the timing between (1) and (3) (for example, before the MAT and MDE flags are cleared in (2)).

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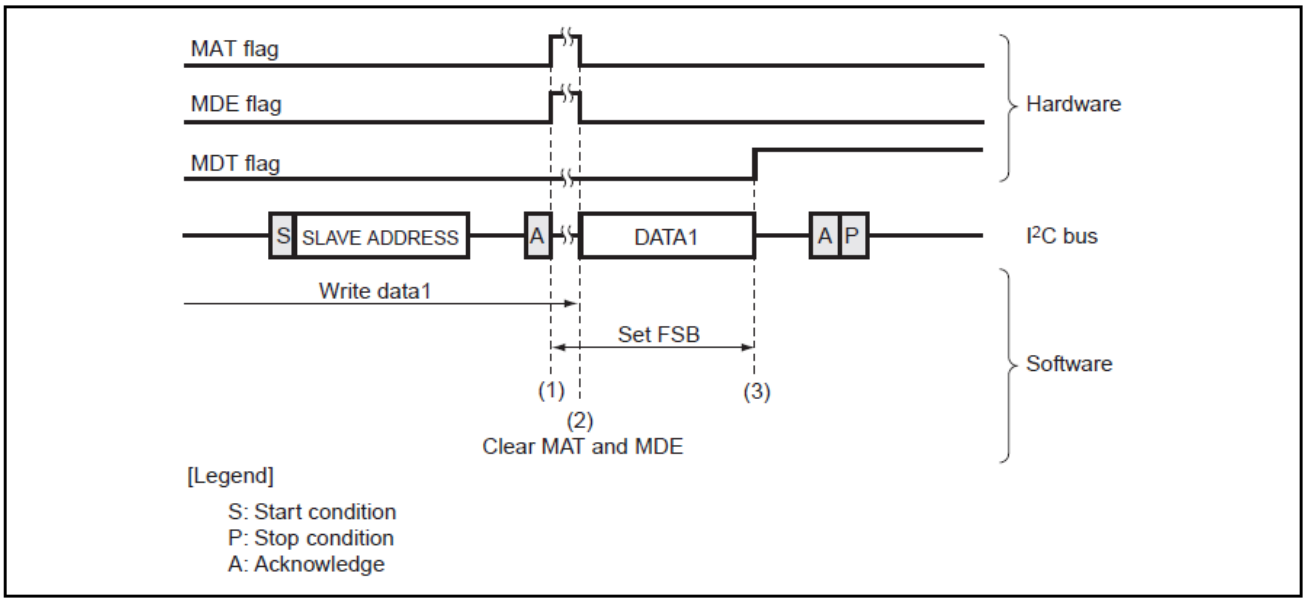

Figure 1.1 Operational Example of One-byte Data Transmission

(2) Two-byte data transmission

Figure 1.2 shows an operational example of two-byte data transmission.

Write data 1 before clearing the MAT and MDE flags to 0 in (2) (for example, in initial setting preceding the issue of start conditions.). Once the MDE flag is cleared, data transmission starts.

[Restriction] Write data 2 within eight SCL clock cycles after clearing the MAT and MDE flags in (2).

Otherwise, data 1 is transmitted twice. If it is impossible to write data 2 within eight SCL clock cycles due to long interrupt processing time, use FIFO buffer mode. Set the FSB flag to 1 at the timing between (4) and (5) (for example, when the MDE flag is set to 1).

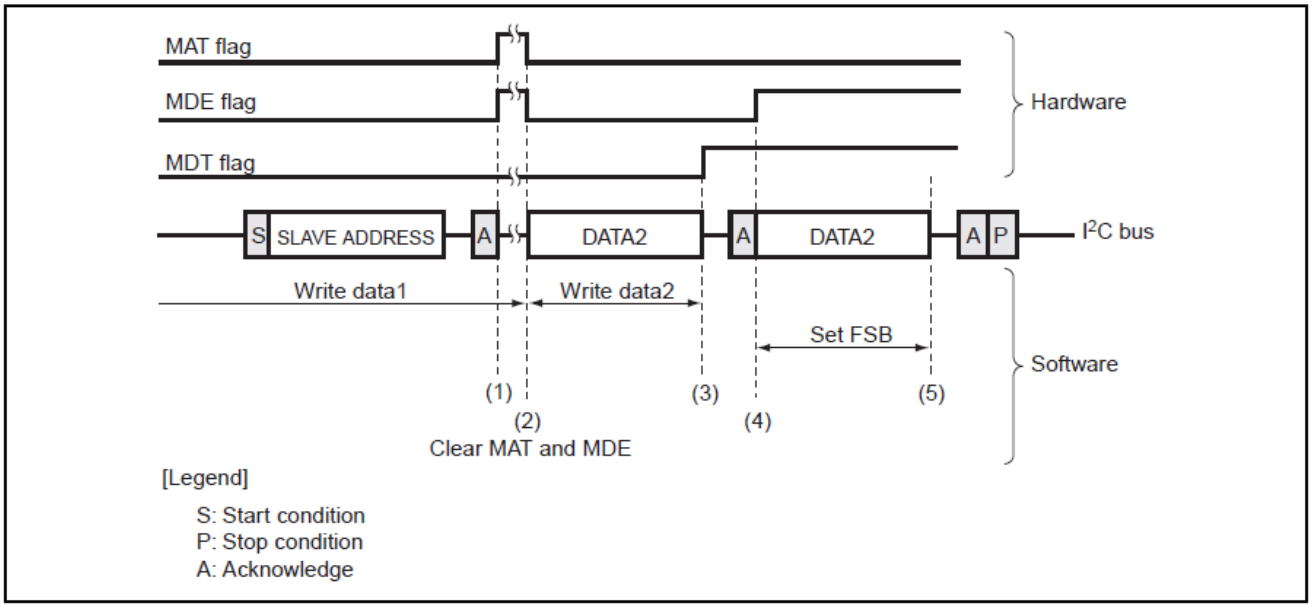

Figure 1.2 Operational Example of Two-byte Data Transmission

(3) Transmission of three or more bytes

Figure 1.3 shows an operational example of three-byte data transmission.

Write data 1 before clearing the MAT and MDE flags in (2) (for example, in initial setting preceding the issue of start conditions). Once the MDE flag is cleared, data transmission starts.

[Restriction] Write data 2 within eight SCL clock cycles after clearing the MAT and MDE flags in (2).

Otherwise, data 1 is transmitted twice. If interrupt processing time is too long to write data 2 within eight SCL clock cycles, use FIFO buffer mode.

Write data 3 only after the timing of (8), and hold the MDE flag as 1 until the timing of (8). (If MDE is set to 1 in (4), refrain from writing data 3 and hold MDE as 1 until (8)). After delaying a write of data 3, write the succeeding transmit data and set FSB to 1 at the moment of a transmission stop with MDE =1. Then the fourth and succeeding bytes can be transmitted without time restriction. To get the timing of (8) ((5) + extra time (1 SCL): it may be longer depending on the system), use the MDT flag. To get the timing at which the MDT flag is set in (5), clear the MDT flag to 0 beforehand within eight SCL clock cycles after the MDT flag is first set to 1 (between (6) and (7)). If it is difficult to make the timing of (8), use FIFO buffer mode.

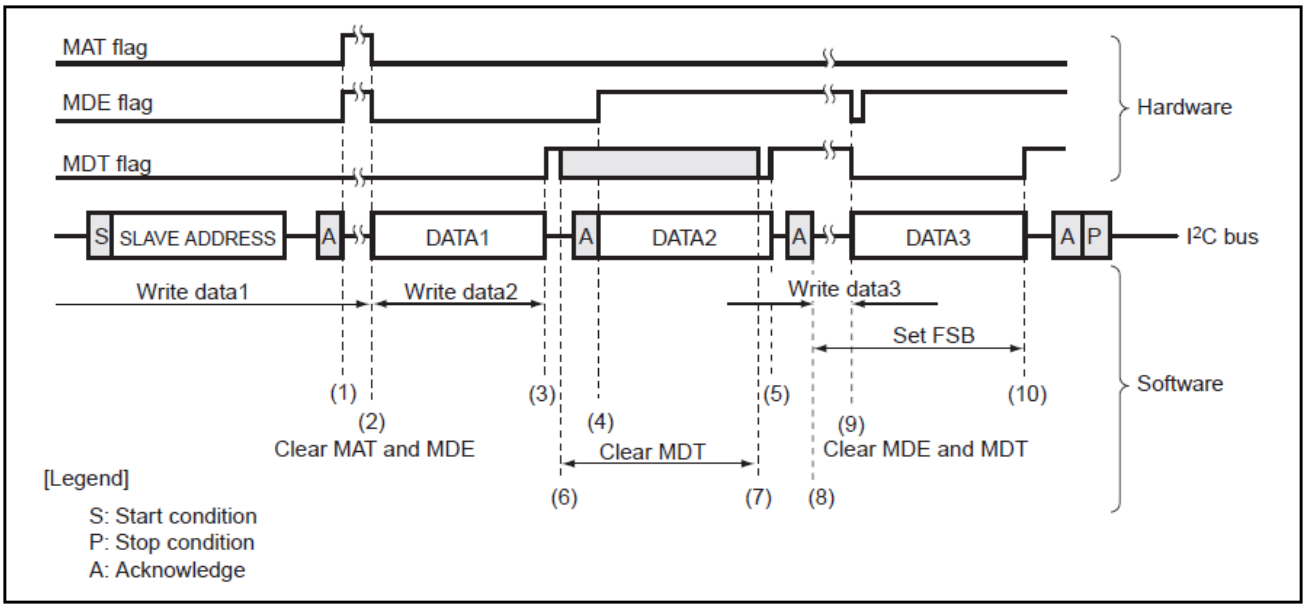

Figure 1.3 Operational Example of Three-byte Data Transmission

An example of transmission of data exceeding three bytes is as follows:

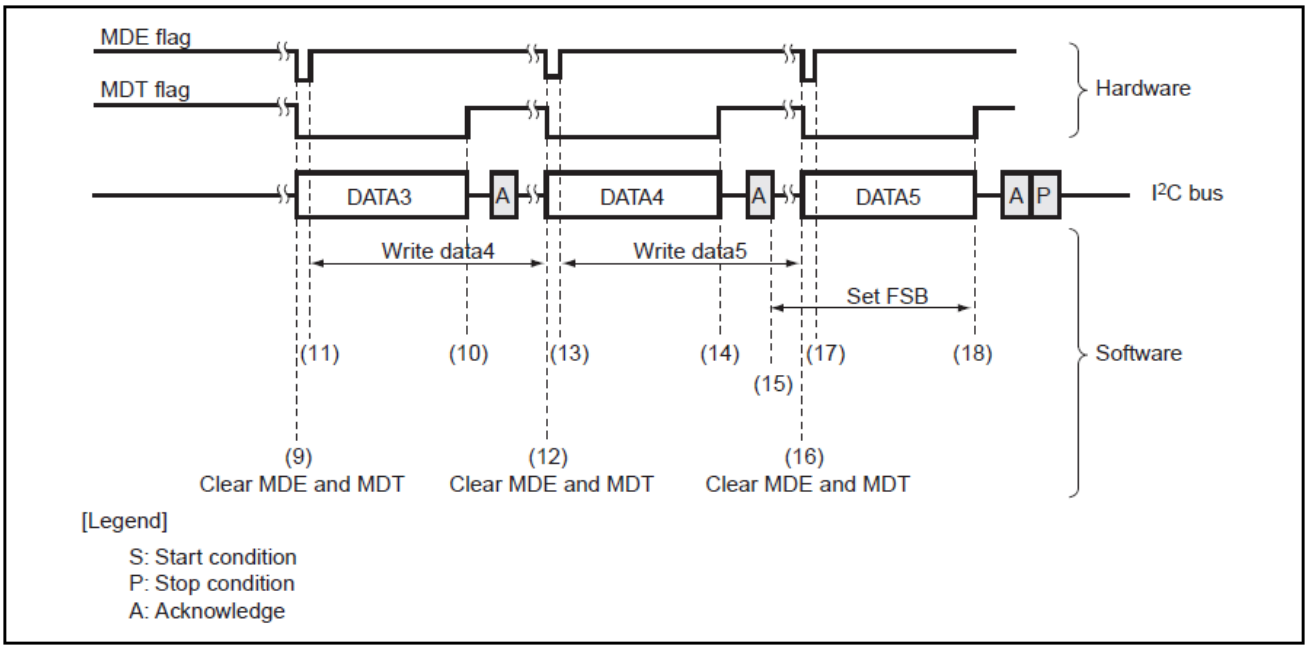

Figure 1.4 Operation Example of Four or More Byte Data Transmission

[Manual correction]

(4) Monitor the progress of data byte transmission (page 699) is corrected as follows. The cancelation line parts are removed and gray parts are modified or added.

(a) ~~Wait for a master event (the MDE bit in the master status register).~~

Set the next byte to the transmit data register. (This must be done before the first byte is completely output.)

(b) ~~Load the next data byte into the transmit data register.*~~

Wait for a master event (the MDE bit in the master status register).

~~Note: * There is no need to observe the limitation that "execution must continue until the first data byte has been output" in this case.~~

Note that there is no correction for procedure (c).

- End of Correction -