To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Date: Apr.28.2008

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-A641A/E	Rev.	1.00
Title	SH7720 hardware manual revised to Rev.3.00		Information Category	Technical Notification		
Applicable Product	SH3-DSP SH7700 Series SH7720 Group	Lot No. All	Reference Document	SH7720 Hardware Manual (REJ09B0033-0200 Rev.2.00) SH7720 Group, SH7721 Group Hardware Manual (REJ09B0033-0300 Rev.3.00)		

SH7720 Hardware Manual is revised from Rev.2.00 to Rev.3.00. SH7720 and SH7320 Group Hardware Manuals are merged into manual Rev.3.00, to which the SH7721 Group is newly added. All the pins in the SD host interface (SDHI) are added. Please refer to main revisions and additions in Rev.3.00 as shown in the following.

Item	Page	Revision (See Manual for Details)
All		SH7720 and SH7320 Group Hardware Manuals are merged into this manual, to which the SH7721 Group is newly added.
All		The pins in the SD host interface (SDHI) are added.
Introduction Abbreviations	viii	Added DES Data Encryption Standard RSA Rivest Shamir Adleman SSL Secure Socket Layer SDHI SD Host Interface
Section 1 Overview Table 1.1 SH7720/SH7721 Features	5	Deleted **Item** / **Features** Serial I/O with FIFO (SIOF0, SIOF1) • Internal 64-byte transmit/receive FIFO • Supports 8-/16-/16-bit stereo sound input/output • Sampling rate clock input selectable from Pϕ and external pin • Internal prescaler for Pϕ • ~~SPI mode~~ ~~- Provides continuous full-duplex communication with SPI slave device in fixed master mode.~~ ~~Transmit/receive data length of fixed 8-bits~~ • With interrupt request and DMAC request

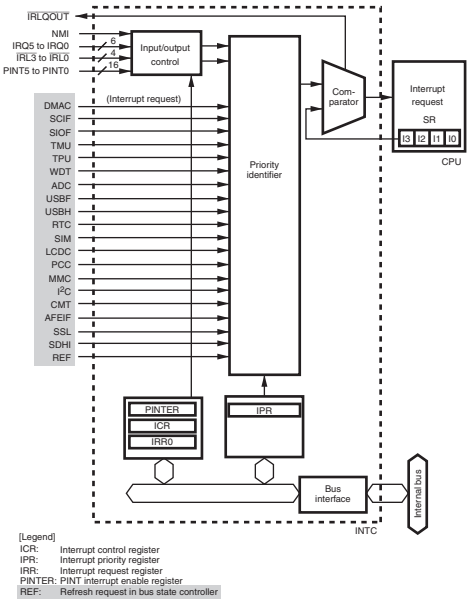
<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Table 1.1 SH7720/SH7721 Features</td><td>6, 7</td><td>Amended
<table>
<tr><th>Item</th><th>Features</th></tr>
<tr><td>PC card controller (PCC)</td><td>• Complies with the PCMCIA Rev.2.1/JEIDA Version 4.2
Supports the IC memory card interface and I/O card interface</td></tr>
<tr><td>A/D converter (ADC)</td><td>• 10 bits ± 4 LSB, four channels
• Conversion time: 15 µs
Input range: 0 to AV_{CC} (max. 3.6 V)</td></tr>
<tr><td>SD host interface (SDHI)
Note: Only for models with the SDHI</td><td>Added</td></tr>
<tr><td>SSL accelerator (SSL)
Note: SH7720 group only</td><td>• RSA encryption
• Supported operations: addition, subtraction, multiplication, power operation
DES and Triple-DES encryption/decryption</td></tr>
</table></td></tr>
<tr><td>Table 1.2 Product Lineup (SH7720 Group)
Table 1.3 Product Lineup (SH7721 Group)</td><td>8, 9</td><td>Replaced and table numbers assigned</td></tr>
<tr><td>1.2 Block Diagram
Figure 1.1 Block Diagram</td><td>10</td><td>SDHI and its related pins added; bridges and clocks deleted.</td></tr>
</table>

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>1.3 Pin Assignments
1.3.1 Pin Assignments
Figure 1.2 Pin Assignments (PLBG0256GA-A (BP-256H/HV))</td><td>11</td><td>Amended
K17 → SCIF0_TxD/IrTX/PTT2
L17 → SCIF0_RxD/IrRX/PTT1</td></tr>
<tr><td>Figure 1.3 Pin Assignments (PLBG0256KA-A (BP-256C/CV))</td><td>12</td><td>Amended
L20→SCIF0_TxD/IrTX/PTT2
L21→SCIF0_RxD/IrRX/PTT1
K1→VssQ1
L1→VccQ1
U5→D5</td></tr>
<tr><td>Table 1.4 List of Pin Assignments</td><td>24</td><td>Amended
<table>
<tr><th>Pin No. (PLBG0256 GA-A)</th><th>Pin No. (PLBG0256 KA-A)</th><th>Pin Name</th><th>Function</th></tr>
<tr><td>U16</td><td>V15</td><td>$\overline{\text{DACK0}}$/ PINT1/ PTM4</td><td>DMA transfer request reception/ port interrupt/ general-purpose port</td></tr>
<tr><td>Y12</td><td>Y11</td><td>$\overline{\text{CS0}}$</td><td>Chip select</td></tr>
<tr><td>Y13</td><td>Y12</td><td>$\overline{\text{RD}}$</td><td>Read strobe</td></tr>
<tr><td>Y14</td><td>Y13</td><td>VssQ1</td><td>I/O power supply (0 V)</td></tr>
<tr><td>Y18</td><td>AA17</td><td>$\overline{\text{DACK1}}$/ PTM5</td><td>DMA transfer request reception/ general-purpose port</td></tr>
</table></td></tr>
</table>

Item	Page	Revision (See Manual for Details)
1.3.2 Pin Functions Table 1.5 SH7720/SH7721 Pin Functions	26, 29, 32	Amended

Classification	Symbol	Name	Function
Clock	XTAL	Crystal	For connection to a crystal resonator.
	CKIO	System clock	Used as a pin to input external clock or output clock.
Direct memory access controller (DMAC)	$\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$	DMA-transfer request	Input pins for external requests for DMA transfer
	$\overline{\text{DACK0}}$, $\overline{\text{DACK1}}$	DMA transfer request reception	Indicates the acceptance of DMA transfer requests to external devices.
Serial I/O with FIFO (SIOF)	SIOF0_SYNC, SIOF1_SYNC	SIOF frame sync	SIOF frame synchronization signals
	SIOF0_TxD, SIOF1_TxD	SIOF transmit data	SIOF transmit data pin
	SIOF0_RxD, SIOF1_RxD	SIOF receive data	SIOF receive data pin
A/D converter (ADC)	AN3 to AN0		Analog input pin
	AVcc		Power supply pin for the A/D or D/A converter. When the A/D or D/A converter is not in use, connect this pin to input/output power supply (VccQ).
	AVss		Ground pin for the A/D or D/A converter. Connect this pin to input/output power supply (VssQ).

1.3.2 Pin Functions	35	Notes added …. 6. SDHI associated pins support only for the models including the SDHI.
Section 2 CPU 2.1 Processing States and Processing Modes 2.1.1 Processing States (1) Reset State	37	Deleted In manual reset, the register contents of a part of the LSI on-chip modules, ~~such as the bus state controller (BSC),~~ are retained.

Item	Page	Revision (See Manual for Details)
Section 8 Interrupt Controller (INTC) Figure 8.1 Block Diagram of INTC	244	Changed 
8.2 Input/Output Pins Table 8.1 Pin Configuration	245	Amended **Name** / **Abbreviation** / **I/O** / **Description** Bus request signal pin / $\overline{\text{IRQOUT}}$ / Out-put / Bus request signal for an interrupt
Section 8 Interrupt Controller (INTC) 8.3 Register Descriptions	246	Deleted ~~Interrupt request register 10 (IRR10)~~

Item | **Page** | **Revision (See Manual for Details)**

8.3.1 Interrupt Priority Registers A to J (IPRA to IPRJ)

Table 8.2 Interrupt Sources and IPRA to IPRJ

248

Amended

Register	Bits 15 to 12	Bits 7 to 4	Bits 3 to 0
IPRD	Reserved*	IRQ5	IRQ4
IPRG	SCIF0	Reserved*	Reserved*
IPRJ	Reserved*	SDHI	AFEIF

Note: * Reserved. Always read as 0. The write value should always be 0. The SSL and SDHI -related bits are effective only for the models that include them. Reserved bits apply if they are not included.

8.3.4 Interrupt Request Register 0 (IRR0)

252

Changed

IRR0 is an 8-bit register that indicates interrupt requests from the TMU and IRQ0 to IRQ5.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

8.3.5 Interrupt Request Register 1 (IRR1)

253

Deleted

IRR1 is an 8-bit register that indicates whether interrupt requests from the DMAC ~~and LCDC~~ are generated.

8.3.6 Interrupt Request Register 2 (IRR2)

254

Changed

IRR2 is an 8-bit register that indicates whether interrupt requests from the SSL and LCDC are generated. This register is initialized to H'00 by a power-on reset or manual reset, but is not initialized in standby mode.

Note: On the models not having the SSL, the SSL-related bits are reserved. The write value should always be 0.

Added

Bit	Bit Name	Description
4	SSLIR	SSLI Interrupt Request … Note: On the models not having the SSL, this bit is reserved and always read as 0. The write value should always be 0.

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>8.3.12 Interrupt Request Register 8 (IRR8)</td><td>261</td><td>Changed

IRR8 is an 8-bit register that indicates whether interrupt requests from the SDHI, MMC, and AFEIF are generated. This register is initialized to H'00 by a power-on reset or manual reset, but is not initialized in standby mode.

Note: On the models not having the SDHI, the SDHI-related bits are reserved. The write value should always be 0.

Changed and a note added.

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>0</td><td>SDIR</td><td>SDI Interrupt Request

Indicates whether the SDI (SDHI) interrupt request is generated.

0: SDI interrupt request is not generated

1: SDI interrupt request is generated

Note: On the models not having the SDHI, this bit is reserved and always read as 0. The write value should always be 0.</td></tr>
</table>
</td></tr>
<tr><td>8.3.13 Interrupt Request Register 9 (IRR9)</td><td>262</td><td>Amended

IRR9 is an 8-bit register that indicates whether interrupt requests from the PCC, USBH, USBF, and CMT are generated. This register is initialized to H'00 by a power-on reset or manual reset, but is not initialized in standby mode.</td></tr>
<tr><td>8.4.3 IRL interrupts</td><td>267</td><td>Deleted

IRL interrupts are included with noise canceller function and detected when the sampled levels of each peripheral module clock keep same value for 2 cycles. This prevents sampling error level in $\overline{\text{IRL}}$ pin changing. ~~In standby mode, noise canceller is handled by the RTC clock because the peripheral module clocks are halted. Therefore, when RTC is not used, recovering to standby by IRL interrupts cannot be executed in standby mode.~~</td></tr>
</table>

Item	Page	Revision (See Manual for Details)
8.4.4 PINT Interrupts	268	Added While an RTC clock is supplied, recovery from a standby state on a PINT interrupt is possible if the interrupt level is higher than that set in the I3 to I0 bits of the SR register.
8.4.6 Interrupt Exception Handling and Priority Table 8.3 Interrupt Exception Handling Sources and Priority (IRQ Mode)	270	Ammended

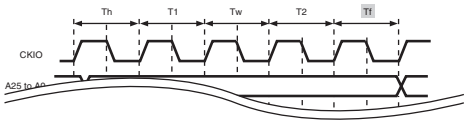
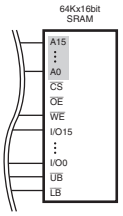
Interrupt Source		Interrupt Code	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Unit	Default Priority
USBH	USBHI	H'A60*3	0 to 15 (0)	IPRJ (11 to 8)	—	
DMAC (2)	DEI4	H'B80*3	0 to 15 (0)	IPRF (11 to 8)	High	
	DEI5	H'BA0*3			Low	
TMU	TMU_SUNI	H'6C0	0 to 15 (0)	IPRD (11 to 8)	—	
—	—	—	—	—	—	

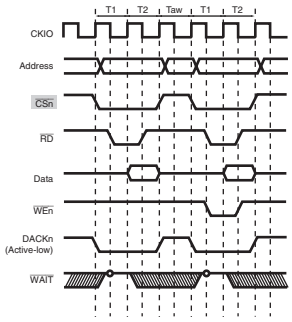
Item	Page	Revision (See Manual for Details)
Table 8.4 Interrupt Exception Handling Sources and Priority (IRL Mode)	272	Changed

Interrupt Source		Interrupt Code	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Unit	Default Priority
NMI						
H-UDI						
IRL	IRL3 to IRL0=B'0000	H'200*3	15	—	—	
	IRL3 to IRL0=B'0001	H'220*3	14	—	—	
	IRL3 to IRL0=B'0010	H'240*3	13	—	—	
	IRL3 to IRL0=B'0011	H'260*3	12	—	—	
	IRL3 to IRL0=B'0100	H'280*3	11	—	—	
	IRL3 to IRL0=B'0101	H'2A0*3	10	—	—	
	IRL3 to IRL0=B'0110	H'2C0*3	9	—	—	
	IRL3 to IRL0=B'0111	H'2E0*3	8	—	—	
	IRL3 to IRL0=B'1000	H'300*3	7	—	—	
	IRL3 to IRL0=B'1001	H'320*3	6	—	—	
	IRL3 to IRL0=B'1010	H'340*3	5	—	—	
	IRL3 to IRL0=B'1011	H'360*3	4	—	—	
	IRL3 to IRL0=B'1100	H'380*3	3	—	—	
	IRL3 to IRL0=B'1101	H'3A0*3	2	—	—	
	IRL3 to IRL0=B'1110	H'3C0*3	1	—	—	
TMU	TMU_SUNI	H'6C0	0 to 15 (0)	IPRD (11 to 8)	—	
—	—	—	—	—	—	

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Section 9 Bus State Controller (BSC)
9.2 Input/Output Pins
Table 9.1 Pin Configuration</td><td>283, 284</td><td>Amended
<table>
<tr><th>Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>RD/$\overline{WR}$</td><td>O</td><td>Read/write signal
Connects to $\overline{WE}$ pins when SDRAM or byte-selection SRAM is connected.</td></tr>
<tr><td>$\overline{RD}$</td><td>O</td><td>Read strobe (read data output enable signal)
A strobe signal to indicate the memory read cycle when the PCMCIA is used.</td></tr>
<tr><td>$\overline{WAIT}$</td><td>I</td><td>External wait input (sampled at the falling edge of CKIO)</td></tr>
<tr><td>$\overline{REFOUT}$</td><td>O</td><td>Bus mastership request signal for refreshing</td></tr>
</table></td></tr>
<tr><td>9.3.2 Shadow Area</td><td>285</td><td>Changed
The BSC decodes A28 to A25 of the physical address and generates chip select signals that correspond to areas 0, 2 to 4, 5A, 5B, 6A, and 6B.</td></tr>
<tr><td>9.4.1 Common Control Register (CMNCR)</td><td>291</td><td>Amended
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>31 to 16</td><td>—</td><td>All 0</td><td>R</td><td>Reserved
These bits are always read as 0. The write value should always be 0.</td></tr>
<tr><td>15</td><td>—</td><td>0</td><td>R</td><td>Reserved
This bit is always read as 0. The write value should always be 0.</td></tr>
</table></td></tr>
</table>

Item	Page	Revision (See Manual for Details)
9.4.2 CSn Space Bus Control Register (CSnBCR)	294	Changed **Bit** / **Bit Name** / **Description** 30 IWW2 / 29 IWW1 / 28 IWW0: Idle Cycles between Write-Read Cycles and Write-Write Cycles … 000: No idle cycle …
9.4.3 CSn Space Wait Control Register (CSnWCR) (1) Normal Space, Byte-Selection SRAM CS0WCR, CS6BWCR CS2WCR, CS3WCR CS4WCR CS5AWCR CS5BWCR CS6AWCR		Added **Bit** / **R/W** / **Description** 10 R/W: … 9 R/W / 8 R/W: Specify the number of wait cycles that are necessary for read or write access. 7 R/W: …
CS4WCR CS5AWCR CS5BWCR		Added **Bit** / **Bit Name** / **Description** 18 R/W: … 17 R/W / 16 R/W: Specify the number of cycles that are necessary for write access. 000: The same cycles as WR3 to WR0 setting (read or write access wait)

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>9.4.4 SDRAM Control Register (SDCR)</td><td>326</td><td>Amended
<table>
<tr><th>Bit</th><th>Bit Name</th><th>R/W</th><th>Description</th></tr>
<tr><td>12</td><td>—</td><td>R</td><td>Reserved
This bit is always read as 0. The write value should always be 0.</td></tr>
<tr><td>11</td><td>RFSH</td><td>R/W</td><td>Refresh Control
Specifies whether or not the refresh operation of the SDRAM is performed.
0: No refresh
1: Refresh</td></tr>
</table></td></tr>
<tr><td>9.5.5 SDRAM Interface
(10) Low-Frequency Mode</td><td></td><td>Deleted</td></tr>
<tr><td>9.5.7 Byte-Selection SRAM Interface
Figure 9.34 Wait Timing for Byte-Selection SRAM (BAS = 1) (Software Wait Only)</td><td>390</td><td>Changed
 
</td></tr>
<tr><td>Figure 9.36 Example of Connection with 16-Bit Data-Width Byte-Selection SRAM</td><td>391</td><td>Changed
 
</td></tr>
<tr><td>9.5.8 PCMCIA Interface
(1) Basic Timing for Memory Card Interface</td><td>395</td><td>Changed
If all 32 Mbytes of the memory space are used as an IC memory card interface, the REG signal that switches between the common memory and attribute memory can be generated by an I/O port.</td></tr>
</table>

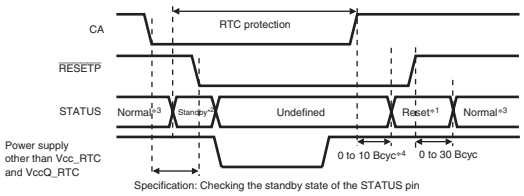
<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Section 10 Direct Memory Access Controller (DMAC)
10.2 Input/Output Pins
Table 10.1 Pin Configuration</td><td>409</td><td>Changed
<table>
<tr><th>Channel</th><th>Name</th><th>Pin Name</th><th>I/O</th></tr>
<tr><td>0</td><td>DMA transfer request</td><td>$\overline{\text{DREQ0}}$</td><td>Input</td></tr>
<tr><td></td><td>DMA transfer request reception</td><td>$\overline{\text{DACK0}}$</td><td>Output</td></tr>
<tr><td></td><td>DMA transfer end</td><td>$\overline{\text{TEND0}}$</td><td>Output</td></tr>
<tr><td>1</td><td>DMA transfer request</td><td>$\overline{\text{DREQ1}}$</td><td>Input</td></tr>
<tr><td></td><td>DMA transfer request reception</td><td>$\overline{\text{DACK1}}$</td><td>Output</td></tr>
<tr><td></td><td>DMA transfer end</td><td>$\overline{\text{TEND1}}$</td><td>Output</td></tr>
</table></td></tr>
<tr><td>Section 10 Direct Memory Access Controller (DMAC)
10.4.2 DMA Transfer Requests
(3)</td><td>428</td><td>Added
….Transfer request signals comprise the transmit data empty transfer request and receive data full transfer request from the ADC set by CHCR0 to CHCR5 and the SCIF0, SCIF1, MMC, USBF, SIM, SIOF0, SIOF1, and SDHI set by DMARS0/1/2,…. These conditions also apply to the SIOF1, MMC, USBF, SIM, SIOF0, SIOF1, and SDHI…..</td></tr>
<tr><td>Table 10.18 Example of BSC Ordinary Memory Access (No Wait, Idle Cycle 1, Longword Access to 16-Bit Device)</td><td>447</td><td>Amended
 

Note: The DACK is asserted for the last transfer unit of the DMA transfer. When the transfer unit is divided into several bus cycles and the CSn is negated between bus cycles, the DACK is also divided.</td></tr>
<tr><td>10.5 Usage Notes
10.5.2 Notes on the Cases When DACK is Divided</td><td>448</td><td>Section 10.5.2 added</td></tr>
</table>

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Section 11 Clock Pulse Generator (CPG)
11.1 Features</td><td>453</td><td>Deleted
~~• Clocks for specific modules generated: In addition to Iϕ, Pϕ, and Bϕ, two other clocks, USBH/USBF clock (Uϕ), can be generated for specific modules. Uϕ is a clock input from an external pin.~~</td></tr>
<tr><td>Table 11.1 Pin Configuration</td><td>457</td><td>Amended
Note: To prevent device malfunction, the value of the mode control pin is sampled only upon a power-on reset.</td></tr>
<tr><td>11.3 Clock Operating Modes</td><td>458</td><td>Changed
Mode 0: …… The frequency of CKIO ranges from 24.00 to 66.67 MHz, because the input clock frequency ranges from 24.00 to 66.67 MHz.</td></tr>
<tr><td rowspan="2">Section 11 Clock Pulse Generator (CPG)
11.4.1 Frequency Control Register (FRQCR)</td><td>461</td><td>Changed
…FRQCR is initialized by a power-on reset, but not initialized by a power-on reset at the WDT overflow. FRQCR retains its value in a manual reset and in standby mode.</td></tr>
<tr><td>461</td><td>Deleted
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>15</td><td>PLL2EN</td><td>PLL2 Enable
PLL2EN specifies whether make the PLL circuit 2 ON in clock operating mode 7.
~~When the PLL circuit 2 is necessary to output the USBH/USBF clock, PLL2EN makes the circuit ON.~~ The PLL circuit 2 is ON in non-clock operating mode 7 regardless of the PLL2EN setting.
0: PLL circuit 2 is OFF
1: PLL circuit 2 is ON</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>11.4.2 USBH/USBF Clock Control Register (UCLKCR)</td><td>464</td><td>Changed
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>7</td><td>USSCS2</td><td>Source Clock Select
These bits select the source clock.
000: Clock stopped
001: Setting prohibited
010: Setting prohibited
011: Initial value
(To run the USBH/USB, however, change the setting to "110: EXTAL_USB" or "111: USB crystal resonator".)
100: Setting prohibited
101: Setting prohibited
110: EXTAL_USB
111: USB crystal resonator</td></tr>
<tr><td>6</td><td>USSCS1</td><td></td></tr>
<tr><td>5</td><td>USSCS0</td><td></td></tr>
</table></td></tr>
<tr><td>11.6 Usage Notes</td><td>466</td><td>Notes 4 and 5 added.</td></tr>
<tr><td>Section 13 Power-Down Modes
13.1 Features
Table 13.1 States of Power-Down Modes</td><td>478</td><td>Changed
<table>
<tr><th>Mode</th><th>Transition Conditions</th><th>Canceling Procedure</th></tr>
<tr><td>Software Standby mode</td><td>Execute SLEEP instruction with STBY bit in STBCR set to 1</td><td>Interrupt (NMI, IRQ (edge detection), RTC, TMU, PINT
Reset</td></tr>
</table></td></tr>
<tr><td>13.2 Input/Output Pins
Table 13.2 Pin Configuration</td><td>479</td><td>Changed
<table>
<tr><th>Pin Name</th><th>Abbreviation</th><th>I/O</th></tr>
<tr><td>Status 1 output</td><td>STATUS1</td><td>Output</td></tr>
<tr><td>Status 0 output</td><td>STATUS0</td><td></td></tr>
<tr><td>Chip active</td><td>CA</td><td>Input</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>13.3.5 Standby Control Register 5 (STBCR5)</td><td>486</td><td>Amended and notes added
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>7</td><td>—</td><td>Reserved
This bit is always read as 0. The write value should always be 0.</td></tr>
<tr><td>6</td><td>MSTP56</td><td>Module Stop Bit 56
When the MSTP56 bit is set to 1, the supply of the clock to the SDHI is halted.
0: Clock supply to SDHI halted
1: SDHI operates
Note: On the models not having the SDHI, this bit is reserved and is always read as 0. The write value should always be 0.</td></tr>
<tr><td>2</td><td>MSTP52</td><td>Module Stop Bit 52
When the MSTP52 bit is set to 1, the supply of the clock to the SSL is halted.
0: SSL operates
1: Clock supply to SSL halted
Note: On the models not having the SSL, this bit is reserved. The write value should always be 1.</td></tr>
</table></td></tr>
<tr><td>13.5 Software Standby Mode
13.5.2 Canceling Software Standby Mode</td><td>489, 490</td><td>Changed
Software standby mode is canceled by interrupts (NMI, IRQ (edge detection), RTC, TMU, and PINT) or a reset.
(1) Canceling with Interrupt
The on-chip WDT can be used for hot starts. When the chip detects an NMI, IRQ (edge detection)*1, RTC*1, TMU*1, or PINT*1 interrupt,…
Notes: 1. Only when the RTC is used, software standby mode can be canceled by IRQ (edge detection), RTC, TMU, or PINT interrupt.</td></tr>
</table>

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>13.8 Hardware Standby Mode
13.8.1 Transition to Hardware Standby Mode</td><td>496</td><td>Deleted
~~After entering software standby mode by the SLEEP instruction,~~ this LSI enters hardware standby mode by driving the CA pin low.</td></tr>
<tr><td>Section 13 Power-Down Modes
Figure 13.12 Timing When Power of Pins other than VCC_RTC and VCCQ_RTC is Off</td><td>498</td><td>Amended
 

Notes: *1 Reset: HH (STATUS1 = High, STATUS0 = High)
*2 Standby: LH (STATUS1 = Low, STATUS0 = High)
*3 Normal operation: LL (STATUS1 = Low, STATUS0 = Low)
*4 Bcyc: Bus clock cycle</td></tr>
<tr><td>Section 15 16-Bit Timer Pulse Unit (TPU)
15.2 Input/Output Pins
Table 15.2 TPU Pin Configurations</td><td>514</td><td>Changed
<table>
<tr><th>Channel</th><th>Name</th><th>Pin Name</th><th>I/O</th></tr>
<tr><td>0</td><td>TPU compare match output 0</td><td>TPU_TO0</td><td>Output</td></tr>
<tr><td>1</td><td>TPU compare match output 1</td><td>TPU_TO1</td><td>Output</td></tr>
<tr><td>2</td><td>TPU compare match output 2A</td><td>TPU_TO2</td><td>Output</td></tr>
<tr><td></td><td>TPU clock input 2A</td><td>TPU_TI2A</td><td>Input</td></tr>
<tr><td></td><td>TPU clock input 2B</td><td>TPU_TI2B</td><td>Input</td></tr>
<tr><td>3</td><td>TPU compare match output 3A</td><td>TPU_TO3</td><td>Output</td></tr>
<tr><td></td><td>TPU clock input 3A</td><td>TPU_TI3A</td><td>Input</td></tr>
<tr><td></td><td>TPU clock input 3B</td><td>TPU_TI3B</td><td>Input</td></tr>
</table></td></tr>
<tr><td>Section 15 16-Bit Timer Pulse Unit (TPU)
15.4.4 PWM Modes</td><td>536</td><td>Amended
Conditions of duty 0% and 100% are shown below.
Duty 0%: The set value of the duty register (TGRA) is TGRB + 1 for the period register(TGRB).
Duty 100%: The set value of the duty register (TGRA) is 0.</td></tr>
</table>

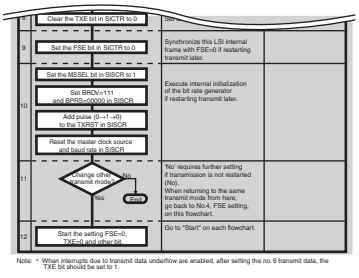
<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Section 18 Serial Communication Interface with FIFO (SCIF)
Table 18.1 Pin configuration</td><td>588</td><td>Changed
<table><tr><th>Channel</th><th>Pin Name</th><th>Abbreviation</th></tr><tr><td>0</td><td>SCIF0_SCK</td><td>SCK</td></tr><tr><td></td><td>SCIF0_RxD</td><td>RxD</td></tr><tr><td></td><td>SCIF0_TxD</td><td>TxD</td></tr><tr><td></td><td>$\overline{\text{SCIF0\_CTS}}$</td><td>$\overline{\text{CTS}}$*2</td></tr><tr><td></td><td>$\overline{\text{SCIF0\_RTS}}$</td><td>$\overline{\text{RTS}}$*2</td></tr></table></td></tr>
<tr><td>18.5 Interrupt Sources and DMAC</td><td>635</td><td>Changed
Set the interrupt enable bits (TIE, RIE) that correspond to the interrupt sources used for activation of the DMAC. Clear the other interrupt enable bits (TSIE, ERIE, BRIE, and DRIE) to 0.</td></tr>
<tr><td>Section 19 Infrared Data Association Module (IrDA)
19.2 Input/Output Pins
Table 19.1 Pin Configuration</td><td>640</td><td>Changed
<table><tr><th>Name</th><th>Pin Name</th><th>Abbreviation</th></tr><tr><td>IrDA receive data</td><td>IrRX</td><td>IrRx</td></tr><tr><td>IrDA transmit data</td><td>IrTX</td><td>IrTx</td></tr></table></td></tr>
<tr><td>Section 19.3 Infrared Data Association Module (IrDA)
19.3.1 IrDA Mode Register (SCIMR)</td><td>641</td><td>Added
Note: Recommended value of IrDA</td></tr>
<tr><td>Section 20 I^2C Bus Interface (IIC)
20.2 Input/Output Pins
Table 20.1 I^2C Bus Interface Pins</td><td>648</td><td>Changed
<table><tr><th>Name</th><th>Pin Name</th><th>Abbreviation</th></tr><tr><td>IIC clock</td><td>IIC_SCL</td><td>SCL</td></tr><tr><td>IIC data I/O</td><td>IIC_SDA</td><td>SDA</td></tr></table></td></tr>
</table>

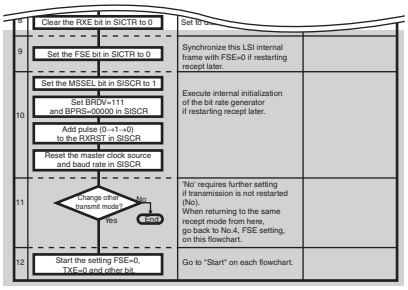
<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>20.3.5 I²C Bus Status Register (ICSR)</td><td>656</td><td>Changed
<table><tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr><tr><td>3</td><td>STOP</td><td>Stop Condition Detection Flag
[Setting conditions]
In master mode: when a stop condition is detected after frame transfer is completed
In slave mode: when a stop condition is detected after the address set in SAR matches the salve address that comes as the first byte after the detection of a start condition
[Clearing condition]
When 0 is written in STOP after reading STOP = 1</td></tr></table></td></tr>
<tr><td>20.7 Usage Notes</td><td>677</td><td>Changed
The falling edge of the ninth clock is recognized by checking the SCLO bit in the I²C bus control register 2 (ICCR2).</td></tr>
<tr><td>Section 21 Serial I/O with FIFO (SIOF)</td><td>679</td><td>Deleted
This LSI includes a clock-synchronized serial I/O module with FIFO (SIOF) that comprises two channels. ~~The SIOF can perform serial communication with a serial peripheral interface bus (SPI).~~</td></tr>
<tr><td>21.1 Features</td><td>679</td><td>SPI mode deleted.</td></tr>
<tr><td>21.2 Input/Output Pins
Table 21.1 Pin Configuration</td><td>681</td><td>All descriptions related to SPI mode deleted.</td></tr>
<tr><td>21.3 Register Descriptions</td><td>682</td><td>SPI Control Register (SPICR) deleted.</td></tr>
</table>

Item	Page	Revision (See Manual for Details)
21.3.9 FIFO Control Register (SIFCTR)	701, 702	Changed

Bit	Bit Name	Description
15	TFWM2	…
14	TFWM1	A transfer request to the transmit FIFO is issued by the TDREQ bit in SISTR. The transmit FIFO is always used as 16 stages of the FIFO regardless of these bit settings.
13	TFWM0	
7	RFWM2	…
6	RFWM1	A transfer request to the receive FIFO is issued by the RDREQ bit in SISTR. The receive FIFO is always used as 16 stages of the FIFO regardless of these bit settings.
5	RFWM0	

21.4.7 Transmit and Receive Procedures (1) Transmission in Master Mode	721	Figure 21.9 replaced.



Item	Page	Revision (See Manual for Details)
(2) Reception in Master Mode	722	Figure 21.10 replaced. 
Table 21.11 Transmit and Receive Reset	725	Added Note 1 to 4 Notes: Refer to the following procedure to operate the transmit reset/receive reset. 1. Set the master clock source in peripheral clock. (Write 1 (master clock = Pf (peripheral clock)) to MSSEL bit in the SISCR register). 2. Set prescaler count value of the baud rate generator by1/1. (Write "00000" (division ratio= 1/1) to the BRPS bits 4 to 0 in SISCR register). 3. Set division ratio in borate generator's output level by 1/1. (Write "111" (division ratio=1/1) to the BRDV bits 2 to 0 in SISCR register). 4. Reset transmit/receive operation. (Write "1", to reset, to TXRST or RXRST bit in the SICTR register).
21.4 Operation 21.4.10 SPI Mode		Deleted
21.5 Usage Notes	734	Added

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Section 23 USB Pin Multiplex Controller
23.2 Input/Output Pins
Table 23.3 Pin Configuration (Power Control Signal)</td><td>757</td><td>Changed
<table>
<tr><th>Name</th><th>Pin Name</th><th>I/O</th></tr>
<tr><td>USB1 power enable/pull-up control pin</td><td>USB1_pwr_en/ USBF_UPLUP</td><td>Output</td></tr>
<tr><td>USB2 power enable pin</td><td>USB2_pwr_en</td><td>Output</td></tr>
<tr><td>USB1 overcurrent /monitor pin</td><td>$\overline{\text{USB1\_ovr\_current}}$/ USBF_VBUS</td><td>Input</td></tr>
<tr><td>USB2 overcurrent pin</td><td>$\overline{\text{USB2\_ovr\_current}}$</td><td>Input</td></tr>
</table></td></tr>
<tr><td>23.4 Examples of External Circuit
23.4.1 Example of the Connection between USB Function Controller and Transceiver</td><td>759</td><td>Changed
The USBF_VBUS pin is multiplexed with the $\overline{\text{USB1\_ovr\_current}}$ pin, and writing 1 to bit 0 (USB_SEL) of UTRCTL selects the USBF_VBUS pin functions.</td></tr>
<tr><td>23.5 Usage Notes
23.5.3 Handling of USB Power Supply</td><td></td><td>Deleted</td></tr>
<tr><td>Section 24 USB Host Controller (USBH)
24.1 Features</td><td>765</td><td>Added
Support 127 endpoints control in maximum
Possible to use only the SDRAM area of area 3 as transmit data and discriptor.</td></tr>
</table>

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>24.2 Input/Output Pins
Table 24.1 Pin Configuration</td><td>766</td><td>Amended
<table>
<tr><th>Pin Name</th><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>USB1 power enable/pull-up control pin</td><td>USB1_pwr_en</td><td>Output</td><td>USB port 1 power enable control</td></tr>
<tr><td>USB2 power enable pin</td><td>USB2_pwr_en</td><td>Output</td><td>USB port 2 power enable control</td></tr>
<tr><td>USB1 overcurrent/monitor pin</td><td>$\overline{\text{USB1\_ovr\_current}}$/USBF_VBUS</td><td>Input</td><td>USB port 1 over-current detect/ USB cable connection monitor pin</td></tr>
<tr><td>USB2 overcurrent pin</td><td>$\overline{\text{USB2\_ovr\_current}}$</td><td>Input</td><td>USB port 2 over-current detect</td></tr>
<tr><td>USB external clock</td><td>EXTAL_USB</td><td>Input</td><td>Connect a crystal resonator for USB. Alternatively, an external clock (48 MHz) may be input for USB.</td></tr>
<tr><td>USB crystal</td><td>XTAL_USB</td><td>Output</td><td>Connect a crystal resonator for USB.</td></tr>
</table></td></tr>
<tr><td>24.7 Usage Notes</td><td>801</td><td>Note 1 changed as below, and note 2 added.
1. When using the USB host controller, the bus clock (Bϕ) must be set to 32 MHz or higher. The peripheral clock (Pϕ) must also be set to a higher frequency than 13 MHz.</td></tr>
<tr><td>2. Usage notes on Resume operation</td><td>801</td><td>Section name changed</td></tr>
</table>

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Section 25 USB Function Controller (USBF)
25.1 Features</td><td>803</td><td>Deleted
~~• Supports self-powered mode~~</td></tr>
<tr><td>Section 25 USB Function Controller (USBF)
25.2 Input/Output Pins
Table 25.1 Pin Configuration and Functions</td><td>805</td><td>Changed
<table>
<tr><th>Name</th><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>USB1 overcurrent/monitor pin</td><td>USB1_ovr_current/ USBF_VBUS</td><td>Input</td><td>USB port 1 over-current detection/ USB cable connection monitor pin</td></tr>
<tr><td>USB external clock</td><td>EXTAL_USB</td><td>Input</td><td>Connect a crystal resonator for USB. Alternatively, an external clock (48 MHz) may be input for USB.</td></tr>
<tr><td>USB crystal</td><td>XTAL_USB</td><td>Output</td><td>Connect a crystal resonator for USB.</td></tr>
<tr><td>USB1 power enable/pull-up control pin</td><td>USB1_pwr_en/USBF_UPLUP</td><td>Output</td><td>USB port 1 power enable control/ Pull-up control output pin</td></tr>
<tr><td>~~2P pin~~</td><td>~~USB2_P~~</td><td>~~I/O~~</td><td>~~D+~~</td></tr>
<tr><td>~~2M pin~~</td><td>~~USB2_M~~</td><td>~~I/O~~</td><td>~~D–~~</td></tr>
</table></td></tr>
<tr><td>25.3 Register Description
25.3.1 Interrupt Flag Register 0 (IFR0)
25.3.2 Interrupt Flag Register 1 (IFR1)
25.3.3 Interrupt Flag Register 2 (IFR2)
25.3.4 Interrupt Flag Register 3 (IFR3)
25.3.5 Interrupt Flag Register 4 (IFR4)</td><td>808, 810, 811, 813, 815</td><td>Amended
Shown below is the revised explanation in section 25.3.1. The same change has been made to sections 25.3.2 to 25.3.5
When each flag is set to 1 and the interrupt is enabled in the corresponding bit of IER0, an interrupt request is generated ~~from the INT pin~~ as specified by the corresponding bit in ISR0.</td></tr>
</table>

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>25.3.6 Interrupt Select Register 0 (ISR0)
25.3.7 Interrupt Select Register 1 (ISR1)
25.3.8 Interrupt Select Register 2 (ISR2)
25.3.9 Interrupt Select Register 3 (ISR3)
25.3.10 Interrupt Select Register 4 (ISR4)</td><td>816, 817, 818</td><td>Amended
Shown below is the revised explanation in section 25.3.6 (above the table). The same change has been made to sections 25.3.7 to 25.3.10 (only the register names differ: ISR0 → ISR1 to ISR4 and interrupt flag register 0 → interrupt flag register 1 to 4).
ISR0 selects the interrupt requests to the INTC to be indicated in interrupt flag register 0. When a bit in ISR0 is cleared to 0, the corresponding interrupt is requested as a USBFI0 interrupt. When a bit is set to 1, the corresponding interrupt is requested as a USBFI1 interrupt. With the initial value, each of the interrupt source flags in the interrupt flag register 0 is selected as a USBFI0 interrupt.</td></tr>
<tr><td>25.3.11 Interrupt Enable Register 0 (IER0)
25.3.12 Interrupt Enable Register 1 (IER1)
25.3.13 Interrupt Enable Register 2 (IER2)
25.3.14 Interrupt Enable Register 3 (IER3)
25.3.15 Interrupt Enable Register 4 (IER4)</td><td>818, 819, 820,</td><td>Changed
Shown below is the revised explanation in section 25.3.11. The same change has been made to sections 25.3.12 to 25.3.15 (only the register name differs: interrupt select register 0 → interrupt select register 1 to 4).
When an interrupt flag is set to 1 while the corresponding bit of each interrupt is set to 1, the interrupt request set in the interrupt select register 0 is issued.</td></tr>
<tr><td>25.3.31 DMA Transfer Setting Register (DMA)</td><td>826</td><td>Corrected
The USB1_pwr_en pin level can be controlled by the bit 2.</td></tr>
<tr><td>25.3.36 Control Register 0 (CTLR0)</td><td>830</td><td>Changed
<table><tr><th>Bit</th><th>Bit Name</th><th>Initial value</th><th>R/W</th><th>Description</th></tr><tr><td>2</td><td>—</td><td>0</td><td>R</td><td>Reserved
This bit is always read as 0. The write value should always be 0.</td></tr></table></td></tr>
</table>

Item	Page	Revision (See Manual for Details)
25.5 EP4 Isochronous-Out Transfer Figure 25.14 EP4 Isochronous-Out Transfer Operation (SOF is Normal) Figure 25.15 EP4 Isochronous-Out Transfer Operation (SOF is Broken)	849, 890	All “INTN” in the figures changed to “Interrupt request”.
25.6 EP5 Isochronous-In Transfer Figure 25.16 EP5 Isochronous-In Transfer Operation (SOF is Normal) Figure 25.17 EP5 Isochronous-In Transfer Operation (SOF in Broken)	852, 853	All “INTN” in the figures changed to “Interrupt request”.
25.9 Usage Notes 25.9.7 Note on Clock Frequency	861	Section 25.9.7 added.
Section 26 LCD Controller	863	Representations of the bus clock and peripheral clock are changed from Bck and Pck to Bϕ and Pϕ, respectively.
26.1 Features	863	Corrected • Supports the selection of data formats (the endian setting for bytes, packed pixel method) by register settings.
26.3 Register Description 26.3.1 LCDC Input Clock Register (LDICKR)	867	Added This LCDC can select the bus clock (Bϕ), the peripheral clock (Pϕ), or the external clock (LCD_CLK) as its operation clock source.
26.3.10 LCDC Horizontal Character Number Register (LDHCNR)	880	Deleted Notes: 1. The values set in HDCN and HTCN must satisfy the relationship of HTCN ≥ HDCN. ~~Also, the total number of characters of HTCN must be an even number. (The set value will be an odd number, as it is one less than the actual number.)~~

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Table 26.3 Limits on the Resolution of Rotated Displays, Burst Length, and Connected Memory (32-bit SDRAM)</td><td>901</td><td>Changed
Note: Set the data of the number of line specified as burst length that can be stored in address of SDRAM same as that of ROW.</td></tr>
<tr><td>26.5 Clock and LCD Data Signal Examples</td><td></td><td>Figure 26.21 Clock and LCD Data Signal Example (TFT Color 12-Bit Data Bus Module) deleted.</td></tr>
<tr><td>Section 27 A/D Converter
27.1 Features</td><td>929</td><td>Amended
• High-speed conversion
— Minimum conversion time: 15 µs per channel
~~(Pϕ = 33 MHz operation)~~</td></tr>
<tr><td>27.2 Input Pins
Table 27.1 Pin Configuration</td><td>931</td><td>Changed
<table>
<tr><th>Pin Name</th><th>Abbreviation</th><th>I/O</th><th>Function</th></tr>
<tr><td>Analog power supply pin</td><td>AVcc</td><td>Input</td><td>Analog power supply and reference voltage for A/D conversion</td></tr>
<tr><td>Analog ground pin</td><td>AVss</td><td>Input</td><td>Analog ground</td></tr>
<tr><td>ADC analog input pin 0</td><td>AN0</td><td>Input</td><td>Analog inputs</td></tr>
<tr><td>ADC analog input pin 1</td><td>AN1</td><td>Input</td><td></td></tr>
<tr><td>ADC analog input pin 2</td><td>AN2</td><td>Input</td><td></td></tr>
<tr><td>ADC analog input pin 3</td><td>AN3</td><td>Input</td><td></td></tr>
<tr><td>ADC external trigger pin</td><td>$\overline{\text{ADTRG}}$</td><td>Input</td><td>External trigger input for starting A/D conversion</td></tr>
</table></td></tr>
<tr><td>27.3 Register Description
27.3.1 A/D Data Registers A to D (ADDRA to ADDRD)</td><td>932</td><td>Added
Each ADDR is initialized to H'0000 by a reset and the module standby function and in standby mode.</td></tr>
<tr><td>27.3.2 A/D Control/Status Registers (ADCSR)</td><td>933</td><td>Added
ADCSR is initialized to H'0000 by a reset and the module standby function and in standby mode.</td></tr>
</table>

Item	Page	Revision (See Manual for Details)
27.4 Operation 27.4.1 Single Mode	936	Steps 1 and 9 added; step 8 partially deleted. 1. Start the clock supply to the ADC module (clear the MSTP33 bit in STBCR3 to 0) to run the ADC module. … 8. Execution of the A/D interrupt handling routine ends. ~~Then, when the ADST bit is set to 1, A/D conversion starts and steps 2 to 7 are executed.~~ 9. Stop the clock supply to the ADC module (set the MSTP33 bit in STBCR3 to 1) to place the ADC in the module standby state.
27.4.2 Multi Mode	938	Steps 1 and 7 added (same as steps 1 and 9 above).
27.4.3 Scan Mode	940	Steps 1 and 8 added (same as steps 1 and 9 above); step 7 partially deleted and changed. … 7. Steps 3 to 5 are repeated as long as the ADST bit remains set to 1. When the ADST bit is cleared to 0, A/D conversion stops. ~~After that, if the ADST bit is set to 1, A/D conversion starts again from the first channel (AN0).~~ …
Table 27.3 A/D Conversion Time (Single Mode)	943	Added Note: Values in the table are numbers of states (tcyc) for Pϕ.
27.7 Usage Notes 27.7.1 Notes on A/D Conversion 27.7.2 Notes on A/D Conversion-End Interrupt and DMA Transfer	946 to 948	Added

Item	Page	Revision (See Manual for Details)
27.7.5 Setting Analog Input Voltage	949	Deleted Operating the chip in excess of the following voltage range may result in damage to chip reliability. ~~Analog Input Voltage Range:~~ During A/D conversion, the voltages (VANn) input to the analog input pins ANn should be in the range $AV_{SS} \leq VANn \leq AV_{CC}$ (n = 0 to 3). ~~The relationship between AV_{CC}, AV_{SS} and $V_{CC}Q$, $V_{SS}Q$ should satisfy $V_{CC}Q - 0.3\ V \leq AV_{CC} \leq V_{CC}Q + 0.3\ V$ and $AV_{SS} = V_{SS}Q$. Even when the A/D converter is not used, make sure that AV_{CC} is connected to VccQ and AV_{SS} is connected to VssQ~~.
Section 28 D/A Converter (DAC) 28.5 Usage Note 28.5.1 Handling of the Analog Power Supply Pins		Deleted
Section 29 PC card controller (PCC) 29.1.1 PCMCIA Support (1) Continuous 32-Mbyte Area Mode	959	Changed ….When an address of 32 Mbytes or less is accessed, set 0 in POPA25. This bit does not affect access to attribute memory space or I/O memory space.
(2) Continuous 16-Mbyte Area Mode	961	Changed and deleted ….In the common memory space, set the PC card address in bit 2 (P0PA25) and bit 1 (P0PA24) of the general control register to access each address space of 16 Mbytes unit. By this operation, values are output to A25 and A24 pins, enabling an address space of more than 16 Mbytes specified by P0PA24 to be accessed ~~(initial value: 0 for P0PA25)~~.

Item	Page	Revision (See Manual for Details)
29.2 Input/Output Pins Table 29.2 PCC Pin Configuration	962	Changed

Pin Name	Abbreviation	I/O
PCC wait request	$\overline{\text{PCC\_WAIT}}$	Input
PCC 16-bit input/output	$\overline{\text{PCC\_IOIS16}}$	Input
PCC ready	PCC_RDY	Input
PCC battery detection 1	PCC_BVD1	Input
PCC battery detection 2	PCC_BVD2	Input
PCC card detection 1	$\overline{\text{PCC\_CD1}}$	Input
PCC card detection 2	$\overline{\text{PCC\_CD2}}$	Input
PCC voltage detection 1	$\overline{\text{PCC\_VS1}}$	Input
PCC voltage detection 2	$\overline{\text{PCC\_VS2}}$	Input
PCC space indication	$\overline{\text{PCC\_REG}}$	Output
PCC buffer control	$\overline{\text{PCC\_DRV}}$	Output
PCC reset	PCC_RESET	Output

29.3 Register Description	963	Pin description changed [Before change] → [After change] PCC_RDY ($\overline{\text{IREQ}}$) → RDY/$\overline{\text{BSY}}$ $\overline{\text{PCC\_IOIS16}}$ (WP) → WP $\overline{\text{PCC\_VS2}}$ → $\overline{\text{VS2}}$ $\overline{\text{PCC\_VS1}}$ → VS1 $\overline{\text{PCC\_CD2}}$ → CD2 $\overline{\text{PCC\_CD1}}$ → CD1

Item	Page	Revision (See Manual for Details)
29.3.1 Area 6 Interface Status Register (PCC0ISR)	964	Amended

Bit	Bit Name	Description
7	P0RDY/IREQ	PCC0 Ready The value on the RDY/$\overline{\text{BSY}}$ pin of the PC card connected to area 6 is read when the IC memory card interface is connected. The value of $\overline{\text{IREQ}}$ pin of the PC card connected to area 6 is read when the I/O card interface is connected. This bit cannot be written to. 0: Indicates that the value of RDY/$\overline{\text{BSY}}$ is 0 when the PC card connected to area 6 is an IC memory card interface type. The value of RDY/$\overline{\text{BSY}}$ is 0 when the PC card connected to area 6 is the I/O card interface type. 1: Indicates that the value of PCC_RDY ($\overline{\text{IREQ}}$) is 1 when the PC card connected to area 6 is the IC memory card interface type. The value of PCC_RDY ($\overline{\text{IREQ}}$) is 1 when the PC card connected to area 6 is the I/O card interface type.
6	P0MWP	PCC0 Write Protect The value of WP of the PC card connected to area 6 is read when the IC memory card interface is connected. 0 is read when the I/O card interface is connected. This bit cannot be written to. 0: Indicates that the value of WP is 0 when the PC card connected to area 6 uses the IC memory card interface type. The value of bit 6 is always 0 when the PC card connected to area 6 is the I/O card interface type. 1: Indicates that the value of WP is 1 when the PC card connected to area 6 is the IC memory card interface type.

Item	Page	Revision (See Manual for Details)
29.3.1 Area 6 Interface Status Register (PCC0ISR)	965	Changed

Bit	Bit Name	Description
1	P0BVD2/P0SPKR	PCC0 Battery Voltage Detect 2 and 1 The values of BVD1 and BVD2 pin of the PC card connected to area 6 are read when the IC memory card interface is connected. The values of $\overline{\text{STSCHG}}$ and $\overline{\text{SPKR}}$ pin of the PC card connected to area 6 are read when the I/O card interface is connected. These bits cannot be written to. (1) and (2) added
0	P0BVD1/P0STSCHG	

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>29.5 Usage Notes
(2) Pin Function Control and Card Type Switching</td><td>985</td><td>Changed
….Also, the card status change register (PCC0CSCR) must be cleared after the setting has been made. However, this restriction does not apply to the card detection pins (CD1 and CD2).</td></tr>
<tr><td>Section 30 SIM Card Module (SIM)
30.2 Input/Output Pins
Table 30.1 Pin Configuration</td><td>989</td><td>Changed
<table><tr><th>Name</th><th>Abbreviation</th><th>I/O</th></tr><tr><td>SIM data</td><td>SIM_D*</td><td>I/O</td></tr><tr><td>SIM clock</td><td>SIM_CLK</td><td>Output</td></tr><tr><td>SIM reset</td><td>SIM_RST</td><td>Output</td></tr></table></td></tr>
<tr><td rowspan="3">31.3.3 Response Type Register (RSPTYR)</td><td>1033</td><td>Changed
RSPTYR specifies command format in conjunction with CMDTYR. Bits RTY2 to RTY0 are used to specify the number of response bytes, and bits RTY5 and RTY4 are used to make additional settings.</td></tr>
<tr><td>1033</td><td>Bit 6 changed to a reserved bit.</td></tr>
<tr><td>1033</td><td>Note: Checking of CRC by RTY4 ~~and RTY6~~ is not checking the command response CRC error bit but checking the command response CRC. This checking is not performed for the CRC of the R2 command response in MMC mode.</td></tr>
</table>

Item	Page	Revision (See Manual for Details)
Table 31.2 Correspondence between Commands and Settings of CMDTYR and RSPTYR	1034, 1035	* deleted and note changed.

CMD INDEX	RSPTYR 6	5	4	2 to 0
CMD2	~~*~~			101
CMD3			*	100
CMD4				000
CMD7		1	*	100
CMD9	~~*~~			101
CMD10	~~*~~			101

Notes:

…

* of RTY4 and RTY6 : Set 1 after checking CRC in command response.

…

31.3.4 Transfer Byte Number Count Register (TBCR)	1036	Deleted

… This setting is ignored by the stream transfer command in MMC mode stream.

~~Before executing a command with data read in the multiblock transfer, 16 or more bytes should be set.~~

Bit	Bit Name	Description
3	C3	Transfer data block size
2	C2	~~Before executing a command with data transfer, 4 or more bytes should be set before. Note that the C3 to C0 bits should be set to 0000 when forcible erase is performed by the CMD42 command.~~
1	C1	
0	C0	
		0000: 1 byte
		....

Item: 31.3.7 Response Registers 0 to 16 and D (RSPR0 to RSPR16 and RSPRD)
Page: 1040
Revision (See Manual for Details): Changed

Bit	Bit Name	Initial Value	R/W
7 to 5	—	All 0	—
4 to 0	RSPRD	All 0	R/W

Item: 31.3.14 Interrupt Status Registers 0 and 1 (INTSTR0 and INTSTR1)
Page: 1051
Revision (See Manual for Details): Amended

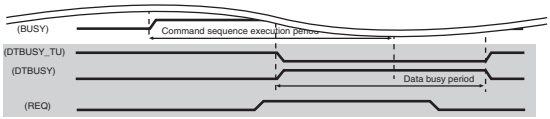
Bit	Bit Name	Description
2	CRCERI	CRC Error Flag [Setting condition] When a CRC error for command response or receive data, and CRC status error for transmission data response are detected while CRCERIE = 1. For any non-R2 command response, CRC is checked when the RTY4 in RSPTYR is set for enabling. For the R2 command response, CRC is not checked; therefore, this flag is not set. [Clearing condition] Write 0 after reading CRCERI = 1. Note: When the CRC error occurs, halt the command sequence by setting the CMDOFF bit to 1.

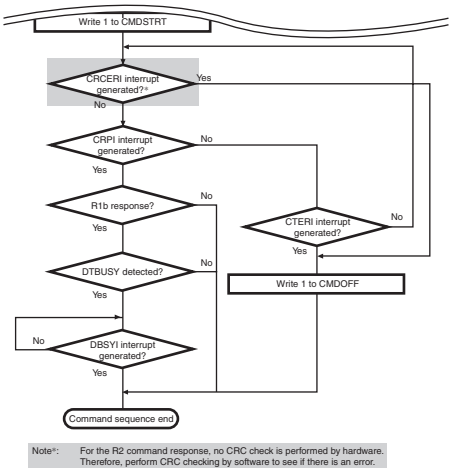
Item: 31.3.15 Transfer Clock Control Register (CLKON)
Page: 1053
Revision (See Manual for Details): Changed

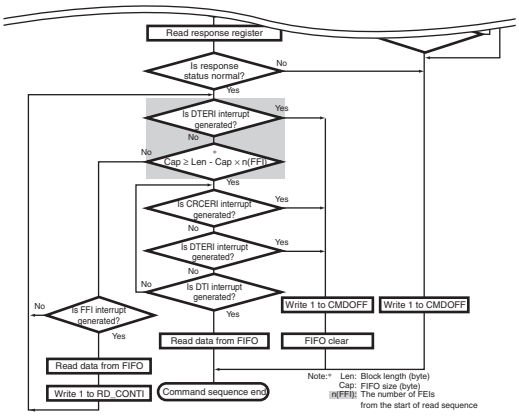
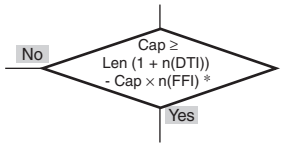
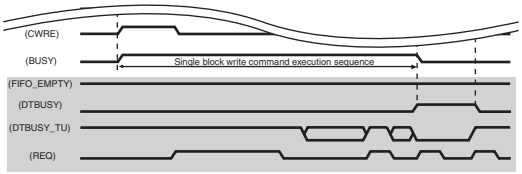
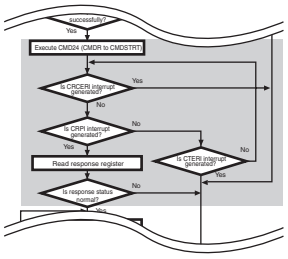
The 33-MHz peripheral clock is needed, and bits CSEL3 to CSEL0 should be set to 0001 for a 16.5-Mbps transfer clock of the MMCIF.

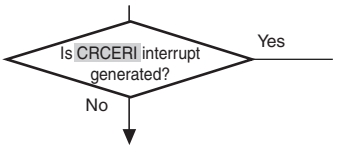
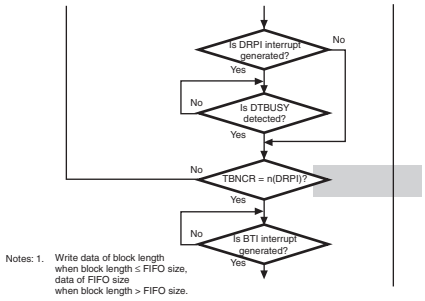
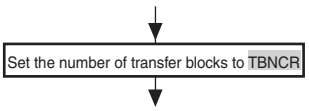
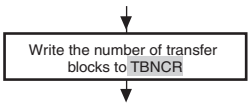
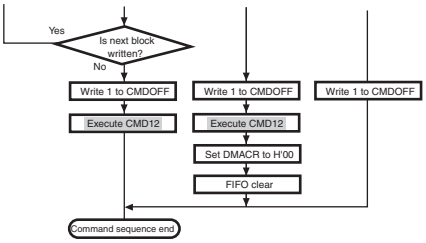
Page: 1053
Revision (See Manual for Details): Changed

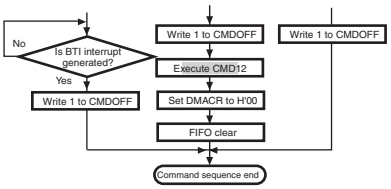
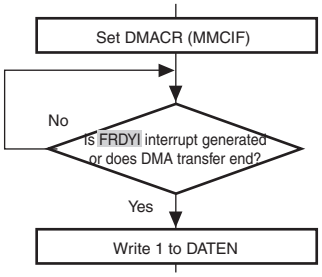
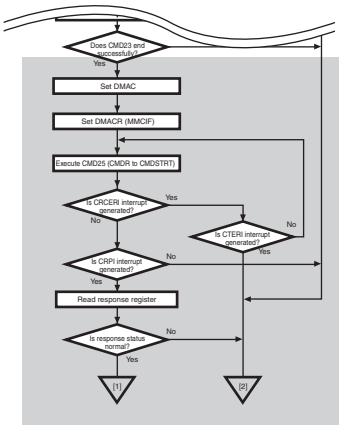
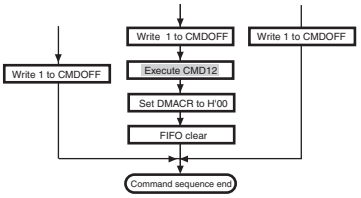
Bit	Bit Name	Description
7	CLKON	Clock On 0: Stops the transfer clock output from the CLK/SCLK pin. 1: Outputs the transfer clock from the CLK/SCLK pin.

Item	Page	Revision (See Manual for Details)
31.3.19 DMA Control Register (DMACR)	1055	Restrictions added Set this register before executing a multiblock transfer command (CMD18 or CMD25). Auto mode cannot be used for open-ended multiblock transfer.
31.4 Operation 31.4.1 Operations in MMC Mode (1) Operation of Broadcast Commands	1059	Deleted …In this case, ~~the transfer clock of CLKON should be divided by 100 and~~ the transfer clock frequency should be set sufficiently slow.
		Corrected and deleted The individual MMC compares its CID and data on the MMC_CMD, and if different, aborts CID output. A single MMC in which the CID can be entirely output enters the acknowledge state. ~~When the R2 response is necessary, CTOCR should be set to H'01.~~
(4) Operation of Commands without Data Transfer	1062	Corrected For a command that is related to time-consuming processing such as flash memory write/erase, the MMC indicates the data busy state via the MMC_DAT. … • Whether the data busy state is entered or not is determined by the DTBUSY bit in CSTR. …
Figure 31.5 Example of Command Sequence for Commands without Data Transfer (with Data Busy State)	1064	Changed 

Item	Page	Revision (See Manual for Details)
(4) Operation of Commands without Data Transfer Figure 31.6 Operational Flowchart for Commands without Data Transfer	1065	Changed 
(5) Commands with Read Data	1066	Changed • The end of the command sequence is detected by polling the BUSY flag in CSTR or by the data transfer end flag (DTI) or the multiblock transfer (pre-defined) end flag (BTI).
	1067	Added Note: In multiblock transfer, if you terminate the command sequence (by writing 1 in the CMDOFF bit) before the command response reception is completed (CRPI = 1), the command response cannot be received correctly. To receive a command response, continue the command sequence (by setting the RD_CONTI bit to 1) until the reception of the command response is completed.

Item	Page	Revision (See Manual for Details)
Figure 31.11 Operational Flowchart for Commands with Read Data (Single Block Transfer)	1071	Changed 
Figure 31.12 Operational Flowchart for Commands with Read Data (Open-ended Multiblock Transfer) (2)	1073	Changed 
(6) Commands with Write Data Figure 31.15 Example of Command Sequence for Commands with Write Data (Block Size ≤ FIFO Size)	1078	Changed 
Figure 31.19 Operational Flowchart for Commands with Write Data (Single Block Transfer)	1082	Changed 

Item	Page	Revision (See Manual for Details)
Figure 31.21 Operational Flowchart for Commands with Write Data (Pre-defined Multiblock Transfer) (1)	1085	Corrected 
Figure 31.21 Operational Flowchart for Commands with Write Data (Pre-defined Multiblock Transfer) (2)	1086	Corrected (arrow deleted) 
31.5 Operations Using DMAC Figure 31.25 Operational Flowchart for Read Sequence (Pre-defined Multiblock Transfer) (1)	1093	Corrected 
Figure 31.27 Operational Flowchart for Pre-defined Multiblock Read Transfer in Auto Mode (1)	1096	Corrected 
31.5.2 Operation of Write Sequence Figure 31.29 Operational Flowchart for Write Sequence (Open-ended Multiblock Transfer) (2)	1102	Changed 

Item	Page	Revision (See Manual for Details)
Figure 31.30 Operational Flowchart for Write Sequence (Pre-defined Multiblock Transfer) (2)	1104	Changed 
Figure 31.31 Operational Flowchart for Write Sequence (Stream Write Transfer)	1105	Changed 
31.5.2 Operation of Write Sequence Figure 31.32 Operational Flowchart for Pre-defied Multiblock Write Transfer in Auto Mode (1)	1106	Changed 
Figure 31.32 Operational Flowchart for Pre-defied Multiblock Write Transfer in Auto Mode (2)	1107	Changed 

Item	Page	Revision (See Manual for Details)
Section 34 Pin Function Controller (PFC)	1141	Added Note: The signals related to the SDHI can be selected only on the models that include them.
Table 34.1 Multiplexed Pins	1142, 1144, 1145	Added and changed

Port	Port Function (Related Module)	Other Function (Related Module)
E	PTE6 input (port)	AFE_RXIN input (AFEIF)/IIC_SCL input/output (IIC)
	PTE5 input (port)	AFE_RDET input (AFEIF)/IIC_SDA input/output (IIC)
F	PTF0 input (port)	ADTRG input (ADC)
T	PTT4 input/output (port)	SCIF0_CTS input (SCIF)/TPU_TO1 output (TPU)
	PTT3 input/output (port)	SCIF0_RTS output (SCIF)/TPU_TO0 output (TPU)
	PTT2 input/output (port)	SCIF0_TxD output (SCIF)/IrTX output (IrDA)
	PTT1 input/output (port)	SCIF0_RxD input (SCIF)/IrRX input(IrDA)
	PTT0 input/output (port)	SCIF0_SCK input/output (SCIF)
U	PTU4 input/output (port)	SIOF1_SYNC input/output (SIOF)/SD_DAT2 input/output (SDHI)
	PTU3 input/output (port)	SIOF1_MCLK input (SIOF)/SD_DAT1 input/output (SDHI)/ TPU_TI3B input (TPU)
	PTU2 input/output (port)	MMC_DAT input/output (MMC)/ SIOF1_TxD output (SIOF)/SD_DAT0 input/output (SDHI)/ TPU_TI3A input (TPU)
	PTU1 input/output (port)	MMC_CMD input/output (MMC)/ SIOF1_RxD input (SIOF)/SD_CMD input/output (SDHI)/ TPU_TI2B input (TPU)
	PTU0 input/output (port)	MMC_CLK output (MMC)/ SIOF1_SCK input/output (SIOF)/SD_CLK output (SDHI)/ TPU_TI2A input (TPU)

Item	Page	Revision (See Manual for Details)
Table 34.1 Multiplexed Pins	1145	Added and changed

Port	Port Function (Related Module)	Other Function (Related Module)
V	PTV4 input/output (port)	MMC_VDDON output (MMC)/SCIF1_CTS input (SCIF)/ LCD_VEPWC output (LCDC)/TPU_TO3 output (TPU)
	PTV2 input/output (port)	SIM_D input/output (SIM)/SCIF1_TxD output (SCIF)/SD_CD input (SDHI)
	PTV1 input/output (port)	SIM_RST output (SIM)/SCIF1_RxD input (SCIF)/ SD_WP input (SDHI)
	PTV0 input/output (port)	SIM_CLK output (SIM)/SCIF1_SCK input/output (SCIF)/SD_DAT3 input/output (SDHI)

34.1.6 Port F Control Register (PFCR)	1155	Changed

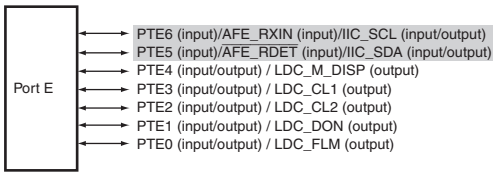
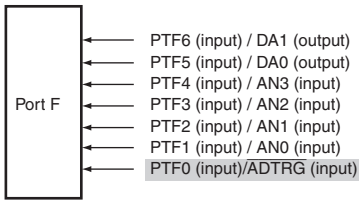
Bit	Bit Name	Description
1	PF0MD1	PF0 Mode
0	PF0MD0	00: Other functions (See table 34.1.)
		01: Reserved
		10: Port input (Pull-up MOS: On)
		11: Port input (Pull-up MOS: Off)

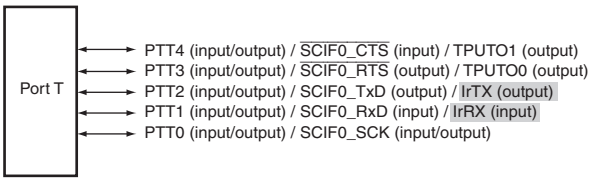
Item	Page	Revision (See Manual for Details)
34.1.21 Pin Select Register C (PSELC)	1174, 1175	Deleted and Amended

Bit	Bit Name	Description
15	PSELC15	MMC_CLK/SIOF1_SCK/SD_CLK/TPU_TI2A Select as PTU0 Other Functions 00: Select SIOF1_SCK 01: Select TPU_TI2A 10: Select MMC_CLK 11: Select according to PSELB0 setting Reserved when PSELB0 = 0 Select SD_CLK when PSELB0 = 1
14	PSELC14	
13	PSELC13	MMC_CMD/SIOF1_RxD/SD_CMD/TPU_TI2B Select as PTU1 Other Functions 00: Select SIOF1_RxD 01: Select TPU_TI2B 10: Select MMC_CMD 11: Select according to PSELB0 setting Reserved when PSELB0 = 0 Select SD_CMD when PSELB0 = 1
12	PSELC12	
11	PSELC11	SIM_RST/SCIF1_RxD/SD_WP Select as PTV1 Other Functions 00: Select SCIF1_RxD 01: Reserved 10: Select SIM_RST 11: Select according to PSELB0 setting Reserved when PSELB0 = 0 Select SD_WP when PSELB0 = 1
10	PSELC10	
9	PSELC9	SIM_D/SCIF1_TxD/SD_CD Select as PTV2 Other Functions 00: Select SCIF1_TxD 01: Reserved 10: Select SIM_D 11: Select according to PSELB0 setting Reserved when PSELB0 = 0 Select SD_CD when PSELB0 = 1
8	PSELC8	

Item	Page	Revision (See Manual for Details)
34.1.22 Pin Select Register D (PSELD)	1176, 1177	Amended

Bit	Bit Name	Description
14 13	PSELD14 PSELD13	MMC_DAT/SIOF1_TxD/SD_DAT0/TPU_TI3A Select as PTU2 Other Functions 00: Select SIOF1_TxD 01: Select TPU_TI3A 10: Select MMC_DAT 11: Select according to PSELB0 setting Reserved when PSELB0 = 0 Select SD_DAT0 when PSELB0 = 1
10 9	PSELD10 PSELD9	SIOF1_MCLK/SD_DAT1/TPU_TI3B Select as PTU3 Other Functions 00: Select SIOF1_MCLK 01: Select TPU_TI3B 10: Reserved 11: Select according to PSELB0 setting Reserved when PSELB0 = 0 Select SD_DAT1 when PSELB0 = 1
6 5	PSELD6 PSELD5	SIOF1_SYNC/SD_DAT2 Select as PTU4 Other Functions 00: Select SIOF1_SYNC 01: Reserved 10: Reserved 11: Select according to PSELB0 setting Reserved when PSELB0 = 0 Select SD_DAT2 when PSELB0 = 1
2 1	PSELD2 PSELD1	SIM_CLK/SCIF1_SCK/SD_DAT3 Select as PTV0 Other Functions 00: Select SCIF1_SCK 01: Reserved 10: Select SIM_CLK 11: Select according to PSELB0 setting Reserved when PSELB0 = 0 Select SD_DAT3 when PSELB0 = 1

Item	Page	Revision (See Manual for Details)
Section 35 I/O Ports 35.5 Port E Figure 35.5 Port E	1187	Changed 
35.5.2 Port E Data Register (PEDR) Table 35.5 Port E Data Register (PEDR) Read/Write Operations	1188	Added and changed Separate tables have been provided for conditions n = 0 to 4 and n = 5 and 6.
	1189	Deleted **PECR State** **PEnMD1** / ~~**PEnMD0**~~ / **Pin State** / **Read** / **Write** 0 / ~~0~~ / Other function / PEDR value / Value is written to PEDR, but does not affect pin state. ~~1~~ / ~~Reserved~~ / ~~—~~ / ~~—~~ 1 / ~~0~~ / ~~Input (Pull-up MOS on)~~ / ~~Pin state~~ / ~~Value is written to PEDR, but does not affect pin state.~~ ~~1~~ / Input (Pull-up MOS off) / Pin state / Value is written to PEDR, but does not affect pin state. Note: n= 5 or 6
35.6 Port F Figure 35.6 Port F	1190	Changed 
35.6.2 Port F Data Register (PFDR)	1191	Deleted PFDR is a register that stores data for pins PTF6 to PTF0. Bits PF6DT to PF0DT correspond to pins PTF6 to PTF0. When the function is general input port, if the port is read, the corresponding pin level is read. …

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Table 35.6 Port F Data Register (PFDR) Read/Write Operations</td><td>1191</td><td>Changed
PFCR State
<table>
<tr><th>PFnMD1</th><th>PFnMD0</th><th>Pin State</th><th>Read</th><th>Write</th></tr>
<tr><td>0</td><td>1</td><td>Reserved</td><td>—</td><td>—</td></tr>
</table></td></tr>
<tr><td>35.16 Port T
Figure 35.16 Port T</td><td>1211</td><td>Changed
 
</td></tr>
<tr><td>Section 36 User Debugging Interface (H-UDI)
36.3 Register Descriptions</td><td>1220</td><td>Added
ID register (SDID)
Shift register</td></tr>
<tr><td>36.3.3 Shift Register</td><td>1221</td><td>Added
Shift register is a 32-bit register. The upper 16-bits are set in SDIR at Update-IR.
If shifted in, the shift-in value is shift out after the value of the 32-bit shift register is shifted out.</td></tr>
<tr><td>36.3.4 Boundary Scan Register (SDBSR)</td><td>1221</td><td>Changed
SDBSR is a 434-bit shift register, located on the PAD, for controlling the …</td></tr>
</table>

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Table 36.3 Pins and Boundary Scan Register Bits</td><td>1222, 1225, 1226, 1227</td><td>Changed
<table>
<tr><th>Bit</th><th>Pin Name</th><th>I/O</th></tr>
<tr><td>395</td><td>RD/WR</td><td>OUT</td></tr>
<tr><td>389</td><td>WE1/DQMLU/WE</td><td>OUT</td></tr>
<tr><td>354</td><td>RD/WR</td><td>Control</td></tr>
<tr><td>348</td><td>WE1/DQMLU/WE</td><td>Control</td></tr>
<tr><td>194</td><td>SCIF0_RxD/IrRX/PTT1</td><td>IN</td></tr>
<tr><td>193</td><td>SCIF0_TxD/IrTX/PTT2</td><td>IN</td></tr>
<tr><td>155</td><td>SCIF0_RxD/IrRX/PTT1</td><td>OUT</td></tr>
<tr><td>154</td><td>SCIF0_TxD/IrTX/PTT2</td><td>OUT</td></tr>
<tr><td>117</td><td>SCIF0_RxD/IrRX/PTT1</td><td>Control</td></tr>
<tr><td>116</td><td>SCIF0_TxD/IrTX/PTT2</td><td>Control</td></tr>
</table></td></tr>
<tr><td>36.3.5 ID Register (SDID)</td><td>1230</td><td>Deleted and changed`
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>31 to 0</td><td>DID31 to DID0</td><td>Device ID31 to ID0
Device ID register that is stipulated by JTAG.
H'002F200F (initial value) for this SH7720 Group.
H'002F2447 (initial value) for this SH7721 Group.
Upper four bits may be changed by the chip version.
SDIDH corresponds to bits 31 to 16.
SDIDL corresponds to bits 15 to 0.</td></tr>
</table></td></tr>
</table>

Item	Page	Revision (See Manual for Details)
Section 37 List of Registers 37.1 Register Addresses	1238, 1240, 1253	Amended and the following registers deleted: SPI control register_0 (SPICR_0) SPI control register_1 (SPICR_1)

Register Name	Abbreviation	Number of Bits	Address	Module	Access Size
Interrupt request register 9	IRR9	8	H'A408 0028		8
~~Interrupt request register 10~~	~~IRR10~~	~~8~~	~~H'A408 002A~~		~~8~~
Interrupt request register 0	IRR0	8	H'A414 0004		8
SDRAM mode register	SDMR3	—	H'A4FD 5xxx		16
Port A data register	PADR	8	H'A405 0140	I/O port	8
Port B data register	PBDR	8	H'A405 0142		8

Item	Page	Revision (See Manual for Details)
37.2 Register Bits	1256 to 1288	Amended and SPICR_0 and SPICR_1 deleted.

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
IPRG		SCIF0				SCIF1			INTC
	—	—	—	—	—	—	—	—	
IPRH		PINTA				PINTB			
IRR9	PCCIR	USBHIR	—	CMIR	—	USBFI1R	USBFI0R	—	
IRR0	—	TMU_SUNIR	IRQ5R	IRQ4R	IRQ3R	IRQ2R	IRQ1R	IRQ0R	
IRR1	—	—	—	—	DEI3R	DEI2R	DEI1R	DEI0R	
IRR2	—	—	—	SSLIR	—	—	—	LCDCIR	
IPRD		—		—	TMU (TMU_SUN1)				
CMNCR	—	BSD	—	MAP	BLOCK	DPRTY1	DPRTY0	DMAIW2	BSC
SDCR	—	—	DEEP	—	RFSH	RMODE	PDOWN	BACTV	
CVR	CNFV1	CNFV0	INTV1	INTV0	—	ALTV2	ALTV1	ALTV0	USBF
CTLR0	—	—	—	RWUPS	RSME	—	ASCE	—	
TSRH	—	—	—	—	—	D10	D9	D8	
CMDTYR	—	TY6	TY5	TY4	TY3	TY2	TY1	TY0	MMC
RSPTYR	—	—	RTY5	RTY4	RTY3	RTY2	RTY1	RTY0	
RSPR16	RSPR167	RSPR166	RSPR165	RSPR164	RSPR163	RSPR162	RSPR161	RSPR160	MMC
RSPRD	—	—	—	RSPRD4	RSPRD3	RSPRD2	RSPRD1	RSPRD0	
PACR	PA7MD1	PA7MD0	PA6MD1	PA6MD0	PA5MD1	PA5MD0	PA4MD1	PA4MD0	PFC
PECR	—	—	PE6MD1	—	PE5MD1	—	PE4MD1	PE4MD0	
	PE3MD1	PE3MD0	PE2MD1	PE2MD0	PE1MD1	PE1MD0	PE0MD1	PE0MD0	
PSELB	PSELB15	PSELB14	PSELB13	PSELB12	PSELB11	PSELB10	PSELB9	PSELB8	
	—	—	—	—	—	—	—	PSELB0	
PADR	PA7DT	PA6DT	PA5DT	PA4DT	PA3DT	PA2DT	PA1DT	PA0DT	I/O port
PJDR	—	PJ6DT	PJ5DT	PJ4DT	PJ3DT	PJ2DT	PJ1DT	PJ0DT	

Item	Page	Revision (See Manual for Details)
37.3 Register States in Each Operating Mode	1289 to 1304	Amended, and SPICR_0 and SPICR_1 deleted.

Register Abbreviation	Power-On Reset*[1]	Manual Reset*[1]	Software Standby	Module Standby	Sleep	Module
IRR9	Initialized	Initialized	Retained	—	Retained	INTC
~~IRR10~~	~~Initialized~~	~~Initialized~~	~~Retained~~	~~—~~	~~Retained~~	
IRR0	Initialized	Initialized	Retained	—	Retained	
UCLKCR	Initialized	Retained	Retained	—	Retained	CPG
~~MCLKCR~~	~~Initialized~~	~~Retained~~	~~Retained~~	~~—~~	~~Retained~~	
FRQCR	Initialized*[6]	Retained	Retained	—	Retained	
WTCNT	Initialized*[6]	Retained	Retained	—	Retained	WDT
WTCSR	Initialized*[6]	Retained	Retained	—	Retained	
SCIMR	Initialized	Initialized	Retained	Retained	Retained	IrDA~~(SCIF0)~~
ADDRA	Initialized	Initialized	Initialized	Initialized	Retained	ADC
ADDRB	Initialized	Initialized	Initialized	Initialized	Retained	
ADDRC	Initialized	Initialized	Initialized	Initialized	Retained	
ADDRD	Initialized	Initialized	Initialized	Initialized	Retained	
ADCSR	Initialized	Initialized	Initialized	Initialized	Retained	
DADR0	Initialized	Initialized	Retained	Retained	Retained	DAC
PADR	Initialized	Retained	Retained	–	Retained	I/O port

Notes: .....
5. Changes according to the status of the PC card.
6. Not initialized by a power-on reset due to the WDT.

Section 38 Electrical Characteristics

38.3 DC Characteristics

Table 38.4 DC Characteristics (1) [Common]

Changed

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog (A/D, D/A) power supply voltage		AV_{CC}	3.0	3.3	3.6	V	When not in use, connect to $V_{CC}Q$.
Analog USB power supply voltage		AV_{CC}_USB	3.0	3.3	3.6	V	When not in use, connect to $V_{CC}Q$.
Current consumption	Normal operation	I_{CC}	—	230	300	mA	V_{CC} = 1.5V Iϕ = 133 MHz
		$I_{CC}Q$	—	60	80	mA	$V_{CC}Q$, $V_{CC}Q1$ = 3.3 V Bϕ = 66 MHz

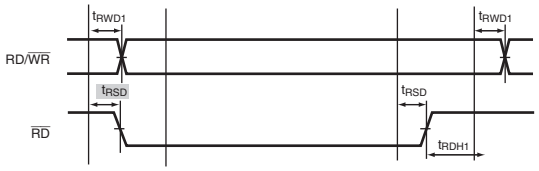
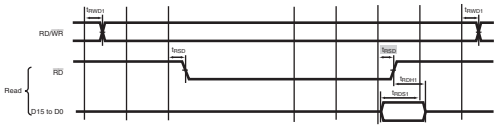
Item	Page	Revision (See Manual for Details)
Table 38.4 DC Characteristics (2-a) [Except USB Transceiver, I^2C, ADC, and DAC Analog Related Pins]	1311	Table title amended Added and deleted

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input high voltage	PTF5 to PTF6	V_{IH}	2.2	—	AV_{CC} + 0.3	V	
	~~AN0~~/PTF1 to ~~AN3~~/PTF4		2.0	—	AV_{CC} + 0.3	V	
	Other input pins		2.2	—	$V_{CC}Q$ + 0.3	V	
Input low voltage	PTF5 to PTF6	V_{IL}	−0.3	—	AV_{CC} × 0.2	V	
	~~AN0~~/PTF1 to ~~AN3~~/PTF4		−0.3	—	AV_{CC} × 0.2	V	
	Other input pins		−0.3	—	$V_{CC}Q$ × 0.2	V	

Table 38.4 DC Characteristics (2-c) [USB Transceiver Related Pins]	1313	Notes: 2. AV_{CC}_USB should satisfy the condition $V_{CC}Q \leq AV_{CC}$_USB and be supplied between AV_{CC}_USB and AV_{SS}_USB.
38.4.2 Control Signal Timing Table 38.8 Control Signal Timing	1319	Changed

Item	Symbol	Min.	Unit
$\overline{\text{RESETP}}$ pulse width	t_{RESPW}	20*3	tcyc*2*4
$\overline{\text{RESETM}}$ pulse width	t_{RESPW}	20*3	tcyc*2*4

38.4.3 AC Bus Timing Table 38.9 Bus Timing	1322	Changed Conditions: Clock Mode 0, $V_{CC}Q$ = 2.7 to 3.6 V, …

Item	Page	Revision (See Manual for Details)
Figures 38.14 to 38.19	1326 to 1331	The description of "Asynchronous" deleted from the figure title
38.4.6 SDRAM Timing	1349 to 1352	Figures 38.37 to 38.40 in Rev 2.00 removed
Figure 38.39 PCMCIA Memory Card Interface Bus Timing	1351	Changed 
Figure 38.40 PCMCIA Memory Card Interface Bus Timing (TED[3:0] = B'0010, TEH[3:0] = B'0001, Software Wait 1, Hardware Wait 1)	1352	Changed 
38.4.8 Peripheral Module Signal Timing Table 38.10 Peripheral Module Signal Timing	1355	Changed Conditions: $V_{CC}Q$ = 2.7 to 3.6 V, $V_{CC}Q1$ = 2.7 to 3.6 V or 1.65 to 1.95 V, V_{CC} = 1.4 to 1.6 V, AV_{CC} = 3.0 to 3.6 V, Ta = –20 to 75°C
38.4.9 16-Bit Timer Pulse Unit (TPU) Table 38.11 16-Bit Timer Pulse Unit	1356	Changed Conditions: $V_{CC}Q$ = 2.7 to 3.6 V, $V_{CC}Q1$ = 2.7 to 3.6 V or 1.65 to 1.95 V, V_{CC} = 1.4 to 1.6 V, AV_{CC} = 3.0 to 3.6 V, Ta = -20 to 75°C Note: * Peripheral clock (Pϕ) cycle.
38.4.10 RTC Signal Timing Table 38.12 RTC Signal Timing	1357	Changed Conditions: $V_{CC}Q$ = 2.7 to 3.6 V, $V_{CC}Q1$ = 2.7 to 3.6 V or 1.65 to 1.95 V, V_{CC} = 1.4 to 1.6 V, AV_{CC} = 3.0 to 3.6 V, Ta = -20 to 75°C

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>38.4.11 SCIF Module Signal Timing
Table 38.13 SCIF Module Signal Timing</td><td>1358</td><td>Changed and deleted
Conditions: $V_{CC}Q$ = 2.7 to 3.6 V, $V_{CC}Q1$ = 2.7 to 3.6 V or 1.65 to 1.95 V, V_{CC} = 1.4 to 1.6 V, AV_{CC} = 3.0 to 3.6 V, Ta = -20 to 75°C
<table>
<tr><th>Module</th><th>Item</th><th>Symbol</th><th>Min.</th></tr>
<tr><td>SCIF</td><td>$\overline{RTS}$ delay time</td><td>t_{RTSD}</td><td>—</td></tr>
<tr><td></td><td>$\overline{CTS}$ setup time ~~(Clock time)~~</td><td>t_{CTSS}</td><td>100</td></tr>
<tr><td></td><td>$\overline{CTS}$ hold time ~~(Clock time)~~</td><td>t_{CTSH}</td><td>100</td></tr>
</table></td></tr>
<tr><td>Figure 38.51 SCIF Input/Output Timing in Synchronous Mode</td><td>1359</td><td>Figure title amended</td></tr>
<tr><td>38.4.13 SIOF Module Signal Timing
Table 38.15 SIOF Module Signal Timing</td><td>1362</td><td>Changed
Conditions: $V_{CC}Q$ = 2.7 to 3.6 V, $V_{CC}Q1$ = 2.7 to 3.6 V or 1.65 to 1.95 V, V_{CC} = 1.4 to 1.6 V, AV_{CC} = 3.0 to 3.6 V, Ta = -20 to 75°C</td></tr>
<tr><td>38.4.14 AFEIF Module Signal Timing
Table 38.16 AFEIF Module Signal Timing</td><td>1365</td><td>Changed
Conditions: $V_{CC}Q$ = 2.7 to 3.6 V, $V_{CC}Q1$ = 2.7 to 3.6 V or 1.65 to 1.95 V, V_{CC} = 1.4 to 1.6 V, AV_{CC} = 3.0 to 3.6 V, Ta = -20 to 75°C
Note: t_{Pcyc} is a cycle time (ns) of a peripheral clock (Pϕ).</td></tr>
<tr><td>38.4.15 USB Module Signal Timing
Table 38.17 USB Module Clock Timing</td><td>1366</td><td>Changed and deleted
<table>
<tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figure</th></tr>
<tr><td>EXTAL_USB clock frequency (48 MHz)</td><td>t_{FREQ}</td><td>47.9</td><td>48.1</td><td>MHz</td><td>38.60</td></tr>
<tr><td>Clock rise time</td><td>t_{R48}</td><td>—</td><td>6</td><td>ns</td><td></td></tr>
<tr><td>Clock fall time</td><td>t_{F48}</td><td>—</td><td>6</td><td>ns</td><td></td></tr>
<tr><td>~~Duty (t_{HIGH}/t_{LOW})~~</td><td>~~t_{DUTY}~~</td><td>~~90~~</td><td>~~110~~</td><td>~~%~~</td><td></td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>38.4.16 LCDC Module Signal Timing
Table 38.20 LCDC Module Signal Timing</td><td>1368</td><td>Conditions added
Conditions: $V_{CC}Q$ = 2.7 to 3.6 V, $V_{CC}Q1$ = 2.7 to 3.6 V or 1.65 to 1.95 V, V_{CC} = 1.4 to 1.6 V, AV_{CC} = 3.0 to 3.6 V, Ta = -20 to 75°C</td></tr>
<tr><td>38.4.17 SIM Module Signal Timing
Table 38.21 SIM Module Signal Timing</td><td>1369</td><td>Changed
Conditions: $V_{CC}Q$ = 2.7 to 3.6 V, $V_{CC}Q1$ = 2.7 to 3.6 V or 1.65 to 1.95 V, V_{CC} = 1.4 to 1.6 V, AV_{CC} = 3.0 to 3.6 V, Ta = -20 to 75°C
<table>
<tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th></tr>
<tr><td>SIM_CLK clock cycle</td><td>t_{SMCYC}</td><td>2 x tpcyc</td><td>16 x tpcyc</td></tr>
</table></td></tr>
<tr><td>38.4.18 MMCIF Module Signal Timing
Table 38.22 MMCIF Module Signal Timing</td><td>1370</td><td>Changed
Conditions: $V_{CC}Q$ = 2.7 to 3.6 V, $V_{CC}Q1$ = 2.7 to 3.6 V or 1.65 to 1.95 V, V_{CC} = 1.4 to 1.6 V, AV_{CC} = 3.0 to 3.6 V, Ta = -20 to 75°C</td></tr>
<tr><td>38.4.19 H-UDI Related Pin Timing
Table 38.23 H-UDI Related Pin Timing</td><td>1372</td><td>Conditions: VccQ = VccQ_RTC = 2.7 to 3.6 V, VccQ1 = 2.7 to 3.6 V or 1.65 to 1.95 V, Vcc = Vcc_PLL1 = Vcc_PLL2 = Vcc_RTC = 1.4 to 1.6 V, AVcc = AVcc_USB = 3.0 to 3.6 V, Ta = -20 to 75°C</td></tr>
<tr><td>Table 38.24 and 38.25</td><td>1374</td><td>Condition changed
[Before change] AVcc = 3.3 ± 0.3V → [After change] AVcc = 3.0 to 3.6 V</td></tr>
<tr><td>38.7 AC Characteristic Test Conditions</td><td>1375</td><td>Changed
• Input pulse level: VccQ to VssQ, VccQ1 to VssQ1</td></tr>
</table>

Item	Page	Revision (See Manual for Details)
Appendix A. Pin States Table A.1 Pin States	1377 to 1384	Changed

Category									
PLBG 0256GA-A	PLBG 0256KA-A	Pin Name	Power-On Reset	Manual Reset	Software Standby	Hardware Standby	Bus Release	I/O	Handling of Unused Pins
A17	A16	AN0/PTF1	Z	Z/I	Z/Z	Z/Z	I/I	I/I	Pull-up
B13	E16	USB2_pwr_en /PTH1	Z	O/P	O/K	Z/Z	O/P	O/IO	Pull-up
B16	A17	USB2_M	Z*2	L	Z	Z	I	IO	Pull-down
B17	A18	USB1_P	Z*1	Z*1	Z	Z	I	IO	Open
B18	A21	USB1_M	Z*1	Z*1	Z	Z	I	IO	Open
C14	E17	$\overline{\text{ADTRG}}$/PTF0	V	I/P	Z/K	Z/Z	I/P	I/I	Open
C16	D16	USB2_P	Z*2	L	Z	Z	I	IO	Pull-down
C19	B20	$\overline{\text{USB1\_ovr\_current}}$ /USBF_VBUS	I	I/I	I/I	I/I	I/I	I/I	Pull-down
D17	A19	USB1d_DMNS / PINT11/ AFE_RLYCNT /PCC_BVD2/ PTG3	Z	I/I/O/I/P	I/I/O/Z/P	Z/Z/Z/Z/Z	I/I/O/I/P	I/I/O/I/IO	Pull-up
H18	H17	SIM_RST/SCIF1_RxD/ SD_WP/PTV1	Z	O/Z/I/P	Z/Z/Z/K	Z/Z/Z/Z	O/I/I/P	O/I/I/IO	Pull-up
K17	L20	SCIF0_TxD/IrTX/PTT2	V	Z/Z/P	Z/Z/K	Z/Z/Z	O/O/P	O/O/IO	Open
L17	L21	SCIF0_RxD/IrRX/ PTT1	V	Z/Z/P	Z/Z/K	Z/Z/Z	I/I/P	I/I/IO	Open
L18	M20	IRQ3/$\overline{\text{IRL3}}$/PTP3	V	I/I/P	I/I/K	Z/Z/Z	I/I/P	I/I/IO	Open
N18	P20	AUDATA2/PTJ3	X	O/P	O/K	Z/Z	O/P	O/IO	Open
N19	N18	AUDATA1/PTJ2	X	O/P	O/K	Z/Z	O/P	O/IO	Open
N20	R17	AUDATA3/PTJ4	X	O/P	O/K	Z/Z	O/P	O/IO	Open
P4	R5	Vss	—	—	—	—	—	—	
P17	P21	Vcc	—	—	—	—	—	—	
P18	R20	AUDATA0/PTJ1	X	O/P	O/K	Z/Z	O/P	O/IO	Open
P19	P18	AUDCK/PTJ6	V	O/P	O/K	Z/Z	O/P	O/IO	Open
P20	T17	VssQ	—	—	—	—	—	—	
R1	P4	VccQ1	—	—	—	—	—	—	
R2	T2	A11	O	O	OZ	Z	Z	O	Open
R3	R2	A13	O	O	OZ	Z	Z	O	Open
R4	R1	A15	O	O	OZ	Z	Z	O	Open

Item	Page	Revision (See Manual for Details)
Appendix A. Pin States Table A.1 Pin States	1384 to 1387	Changed

Category									
PLBG 0256GA-A	PLBG 0256KA-A	Pin Name	Power-On Reset	Manual Reset	Software Standby	Hardware Standby	Bus Release	I/O	Handling of Unused Pins
R17	T20	AUDSYNC/PTJ0	X	O/P	O/K	Z/Z	O/P	O/IO	Open
R18	R21	ASEMD0	I	I	I	I	I	I	Pull-up
R19	R18	TRST/PTL7	I	I/P	Z/K	Z/Z	I/P	I/IO	Pull-down
R20	U17	VccQ	—	—	—	—	—	—	
T1	T5	A16	O	O	OZ	Z	Z	O	Open
T2	V1	A6	O	O	OZ	Z	Z	O	Open
T3	V2	A5	O	O	OZ	Z	Z	O	Open
T4	T1	A12	O	O	OZ	Z	Z	O	Open
T17	U20	TMS/PTL6	I	I/P	Z/K	Z/Z	I/P	I/IO	Pull-up
T18	T18	TCK/PTL3	I	I/P	Z/K	Z/Z	I/P	I/IO	Pull-up
T19	U21	PCC_RESET /PINT7/PTK3	V	O/I/P	O/I/P	Z/Z/Z	O/I/P	O/I/IO	Open
T20	V18	ASEBRKAK/PTJ5	V	O/P	O/K	Z/Z	O/P	O/IO	Open
U1	R4	VssQ1	—	—	—	—	—	—	
U2	T4	A9	O	O	OZ	Z	Z	O	Open
U3	W1	A4	O	O	OZ	Z	Z	O	Open
U4	AA3	A10	O	O	OZ	Z	Z	O	Open
U5	Y5	D11	Z	Z	Z	Z	Z	IO	Pull-up
U6	Y6	D8	Z	Z	Z	Z	Z	IO	Pull-up
U19	V21	PCC_RDY/PINT6/ PTK2	V	I/I/P	Z/I/P	Z/Z/Z	I/I/P	I/I/IO	Open
V15	Y19	DREQ0/PINT0 /PTM6	V	I/I/P	Z/I/P	Z/Z/Z	I/I/P	I/I/IO	Open
V19	AA21	PCC_VS2/PINT5/ PTK1	V	I/I/P	Z/I/P	Z/Z/Z	I/I/P	I/I/IO	Open
W2	AA2	A2	O	O	OZ	Z	Z	O	Open
W3	AA1	A1	O	O	OZ	Z	Z	O	Open
W19	Y21	PCC_VS1/PINT4/ PTK0	V	I/I/P	Z/I/P	Z/Z/Z	I/I/P	I/I/IO	Open

Item	Page	Revision (See Manual for Details)
Table A.1 Pin States	1388	Table notes changed and added. Notes: *1 The conditions for setting USB1_P and USB1_M to Z (open) are as follows: … *2 After negation of RESETP, USB2_P and USB2_M go low after tens of EXTAL_USB clock cycles have been input.
Table A.1 Pin States	1389	Table legends deleted and added. ~~B: Input buffer on, output buffer on~~ X: Undefined
B. Product Lineup	1390, 1391	Table of product lineup replaced