RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU	Document No.	TN-SH7-A875A/E	Rev.	1.00	
Title	SH7455 Group, SH7456 Group User's Manu Hardware Errata Rev. B	Information Category	Technical Notification			
Applicable Product	SH7455 Group, SH7456 Group	Lot No.			56 Group are Rev.	1.10

We inform you of the corrections of "SH7455 Group, SH7456 Group User's Manual: Hardware Rev. 1.10 (Published on September 22, 2011)".

When you use "SH7455 Group, SH7456 Group User's Manual: Hardware Rev. 1.10", should be used together the attached errata.

In addition, the corrections in the following are also included in the attached errata (Rev. B).

- Technical update TN-SH7-A827A/E: Errata (Rev. A)
- Technical update TN-SH7-A859A/E: Errata to User's Manual Regarding CAN Module

Attached Document: "SH7455 Group, SH7456 Group User's Manual: Hardware Rev. 1.10" Errata Rev. B - 11 sheets



*Changes/additions are written in reds and underlined.

Rev.	Page	Part	Contents					
			Incorrect desc	cription is corrected (the 12 th line).				
Added		25.4.6 (3)	Error:	4. To stop receiving when MST bit	t = <mark>"1xx</mark> ", se	t RCVD bit in	the	
in	25-23	Receive		ICCR1 register to "1", then read th				
Rev. A		Operation	Correction:	4. To stop receiving when MST bit			e ICCR	
		oporation	001100110111	register to "1", then read the ICDR			010010	
		32.7.1	Description of	the bit 29 to 24 (PSL5 to PSL0 bit)		Pay CC Statu		
Added		FlexRay CC		CCSV) is corrected.			3 1000	
in	32-76							
Rev. A		Status Vector	Error:	Set to B'000100 when leaving HA				
		Register	Correction:	Set to <u>B'000000</u> when leaving HA				
				C Characteristics - Output Level Vo			d with	
			Driving Ability	Set to "Increased" : Incorrect desc	ription is co	rrected.		
			Error:					
			Item		Symbol	Min.	Unit	
			Output	PA0 to PA13, PB0, PB1, PB3,	V _{OH}	Vcc –1.1	V	
			high-level	PC0 to PC3, PC5, PC6, PC14,				
			voltage	PD0 to PD10, PE15, PF0, PF1,				
			(normal	PF4, PF5, PG0 to PG4, PH0 to				
			output and	PH15, PJ0 to PJ7, PJ10 to PJ15,				
			driving	PK0, PK5, PK6, PK8 to PK14,				
			ability)*1	PL2 to PL6, PL8, PL9				
			Correction:					
			Item		Symbol	Min.	Unit	
			Output	PA0 to PA13, PB0, PB1, PB3,	V _{OH}	Vcc -0.5	V	
		Table 38.6	high-level	PC0 to PC3, PC5, PC6, PC14,	0.1			
			voltage	PD0 to PD10, PE15, PF0, PF1,				
		DC	(normal	PF4, PF5, PG0 to PG4, PH0 to				
		Characteristics	output and	PH15, PJ0 to PJ7, PJ10 to PJ15,				
Added		 Output Level 	driving	PK0, PK5, PK6, PK8 to PK14,				
in	38-6	Voltage:	ability)*	PL2 to PL6, PL8, PL9				
Rev. A	30-0	When 3.3 V is						
Rev. A		Used with	Error:					
		Driving Ability	Item		Symbol	Max.	Unit	
		Set to	Output	PA0 to PA13, PB0, PB1, PB3,	VoL	0.9	V	
		"Increased"	low-level	PC0 to PC3, PC5, PC6, PC14,	01			
		morodood	voltage	PD0 to PD10, PE15, PF0, PF1,				
			(normal	PF4, PF5, PG0 to PG4, PH0 to				
			output and	PH15, PJ0 to PJ7, PJ10 to PJ15,				
			driving	PK0, PK5, PK6, PK8 to PK14,				
			ability)*1	PL2 to PL6, PL8, PL9				
			Correction:			1		
			Item		Symbol	Max.	Unit	
			Output	PA0 to PA13, PB0, PB1, PB3,	Vol	<u>0.4</u>	V	
			low-level	PC0 to PC3, PC5, PC6, PC14,				
			voltage	PD0 to PD10, PE15, PF0, PF1,				
			(normal	PF4, PF5, PG0 to PG4, PH0 to				
			output and	PH15, PJ0 to PJ7, PJ10 to PJ15,				
		1	driving	PK0, PK5, PK6, PK8 to PK14,				
			ability)*1	PL2 to PL6, PL8, PL9				



Rev.	Page	Part				Conte	nts						
	0-		Table 38.25 RSPI	I Timing	: Incorrect			orrected.					
			Error:	0									
			Item		Symbol		Min.	Max.	Uni	t Figures			
				Slave			<u>2 x t_{cyc}</u>	-	ns	00.001			
Added			setup time	Slave	t _{su}	23 1 2		-	115	38.23			
in	38-22	Table 38.25	Setup time							00.20			
	30-22	RSPI Timing											
Rev. A		U U	Correction:										
			Item		Symbol		Min.	Max.	Uni	U			
				Slave	t _{su}	<u> 25 - 2</u>	<u>x t_{cvc}</u>	-	ns				
			setup time							38.23			
			Table 38.28 DRI T corrected. Error: Item DIN3, DIN4 sampl undefined time bef initialization level r	ing edge fore DIN1	Sy	rmbol tar	de is On Min. 8) : Incorre Max.	ect deso Unit ns				
			(when direct reset		(be								
			DIN3, DIN4 sampl			tbr	12	-					
Added in	38-27	Table 38.28 DRI Timing (When Special	undefined time bet initialization level r	fore DIN1		lDI	12	-	ns				
Rev. A		Mode is On)											
			Correction:										
			Item		Syn	nbol	Min.	Max.	Unit	Figures			
						DIN3, DIN4 sample undefined time bef	fore DIN1		tar	8	-	ns	38.25 to 38.28
		1	initialization level r	elease									
		Firmer 20.00	initialization level r DIN3, DIN4 sampl undefined time <u>aftr</u> initialization level r	ing edge <u>er</u> DIN1 [·] elease		tbr	12	-	ns				
Added in Rev. A	38-28	Figure 38.28 Minimum Edge Count at DIN1 Initialization Level in Delayed Reset Mode	DIN3, DIN4 sampl undefined time after initialization level r Figure 38.28 Min Mode (Minimum V	ing edge er DIN1 release imum Eo Width at Nn (n = 2	dge Coun Initializatio	t at DIN	N1 Initial	ization L	evel in				
in	38-28	Minimum Edge Count at DIN1 Initialization Level in	DIN3, DIN4 sampl undefined time aftu initialization level r Figure 38.28 Min Mode (Minimum V Error: DIN Correction: DIN	ing edge er DIN1 elease imum Ec Width at Nn (n = 2 Nn (n = 3	dge Coun Initializatio 2, 3, 4) 3, 4)	t at DIN on Leve	V1 Initial I) : Incor	ization L rect desc	evel in ription i	s corrected.			
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Date: October 1, 2013

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Added in Rev. B	12-7	12.3.2 Flash Access Status Register (FASTAT)	Description of the bit 7 (ROMAE bit) in the Flash Access Status Register (FASTAT) is corrected. Error: An access command is issued to an address other than ROM program/erase addresses H'FD80 0000 to H'FD8F FFFF when the user boot MAT is selected. Correction: An access command is issued to an address other than ROM program/erase addresses H'FD80 0000 to H'FD80 7FFF when the user boot MAT is selected.
Added in Rev. B	12-22	Figure 12.7 Command State Transitions in ROM Read Mode and P/E Mode	Figure 12.7 Command State Transitions in ROM Read Mode and P/E Mode : Incorrect description is corrected. Error: ROM read mode FENTRY = H0001 When set from Command miss or access miss Status register dear Command The access miss state Command miss or Correction: ROM read mode FENTRY = H0001 When set from the access miss state Command miss or access miss state Command miss or access miss state Command miss Status register Command Co
Added in Rev. B	12-35	12.9.4 Reset during Programming or Erasure	Description of Reset during Programming or Erasure is added. -Description: <u>When a hardware reset by "L" level input to the RESET# pin, switching the</u> power off, or a FCU reset by setting the FRESET bit in the FRESETR register, is <u>executed during programming or erasure</u> , the whole data in the programming or <u>erasure area becomes undefined</u> . When the data in an area have become <u>undefined</u> , erase the area before using it again.



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Added in Rev. B	24-10	24.3.3 RSPli Pin Control Register (SPiPCR)	Description of the bit 5 (MOIFE bit) in the RSPIi Pin Control Register (SPiPCR) is corrected. Error: - When the MOIFE bit is cleared to "0", RSPIi outputs <u>on the MOSIi</u> <u>pin the last data unit from the previous serial transfer</u> during the SSL negation period. - 0: MOSIi output value equals final <u>data</u> from previous transfer Correction: - When the MOIFE bit is cleared to "0", RSPIi outputs <u>the final output</u> <u>level of the previous serial transfer to the MOSIi pin during the SSL negation period (When the CPHA bit is "0", MOSIi output value is <u>undefined</u>). - 0: MOSIi output value equals final <u>output level</u> from previous transfer (When the CPHA bit is "0", MOSIi output value is undefined). </u>
Added in Rev. B	24-25	24.3.13 RSPIi Command Registers 0 to 3 (SPiCMD0 to SPiCMD3)	Description of the bit 13 (SPNDEN bit) in the RSPIi Command Registers 0 to 3 (SPiCMD0 to SPiCMD3) is corrected. Error: - If the SPNDEN bit is "0", the RSPIi sets the next-access delay to 1 RSPCK. - 0: A next-access delay of 1 RSPCK Correction: - If the SPNDEN bit is "0", the RSPIi sets the next-access delay to 1 RSPCK <u>+ 2 Pck</u> . - 0: A next-access delay of 1 RSPCK <u>+ 2 Pck</u>
Added in Rev. B	24-29	Table 24.7 MOSIi Signal Value Determination during SSL Negation Period	Table 24.7 MOSIi Signal Value Determination during SSL Negation Period : Incorrect description is corrected. Error: MOIFE MOIFV MOSIi Signal Value during SSL Negation Period 0 0, 1 Final data from previous transfer 1 0 Always "L" 1 1 Always "H" Correction: MOIFE MOIFV MOIFIE MOIFV MOIFV MOSII Signal Value during SSL Negation Period 0 0, 1 Final output level of the previous transfer (When the CPHA bit is "0", MOSII output value is undefined) 1 0 Always "L" 1 1 Always "H"
Added in Rev. B	24-35	Figure 24.11 RSPI Transfer Format (CPHA = "0")	Figure 24.11 RSPI Transfer Format (CPHA = "0") : Incorrect description is corrected. Error: Start Serial transfer period End (CPOL = "0") RSPCKi (CPOL = "1") Sampling MISOI SSLi (CPOL = "0") SSLi (CPOL = "1") Sampling MISOI SSLi (CPOL = "1") Sampling MOSII MOSII MISOI



Added in Rev. B 24-35 Figure 24.12 RSPT Transfer (CPHA = *1*) Seriel transfer Format (CPHA = *1*): Incorrect description is corrected. Error: Seriel transfer rev. B 24-35 Figure 24.12 RSPT Transfer (CPHA = *1*) Seriel transfer particle series Seriel transfer particle series Poil Miso Series Table 26.3 Rev. B Table 26.3 Register Configuration Series Series Performant Particle Series Performant Particle Added in Rev. B 26-5 Table 26.3 Register Configuration Table 26.3 Register Name The values after reset of the CANI Clock Select Register (CICLKR) (i = 0 to 3) are corrected. CAND Clock Select Register COLLR H00 HFFFF Bat7 8.16.32 26-15 Correction: The values after reset of the CANI Clock Select Register COLLR Performat Part 8.16.32 26-15 Correction: CAND Clock Select Register COLLR H00 HFFFF Bat7 8.16.32 26-15 Correction: CANO Clock Select Register COLLR Performat Part 8.16.32 26-15 Correction: CAND Clock Select Register COLLR H00 HFFFF Bat7 8.16.32 26-15 Correction: CANO Clock Select Register COLLR Performat Part 8.16.32 26-15 Correction: CAND Clock Select Register COLLR H00 HFFFF Bat7 8.16.32 26-15 Correction: CANO Clock Select Register COLLR Performat 7.10 Coll Select Register COLLR Perfore Bat7 8.16.32	Rev.	Page	Part	Contents
Added in Rev. B 24-35 Figure 24.12 RSPI Transfer Format (CPHA = "1") Sumpling (CPCA = "1") Sumpling (CPCA = "1") Model in Rev. B 24-35 Figure 24.12 RSPI Transfer Format (CPHA = "1") Sumpling (CPCA = "1") Sumpling (CPCA = "1") Sumpling (CPCA = "1") Model in Rev. B 24-35 Figure 24.12 RSPI Transfer Format (CPHA = "1") Sumpling (CPCA = "1") Sumpling (CPCA = "1") Sumpling (CPCA = "1") Table 26.3 Register Rev. B Table 26.3 Register Configuration The values after reset of the CANI Clock Select Register (CICLKR) (i = 0 to 3) are corrected. Error: Register Name Register Name CANI Clock Select Register C2CLKR H00 HFFFF 8647 HFFFF 8647 8.16.32 26-15 CANI Clock Select Register C3CLKR H00 HFFFF 8647 HFFFF 8647 8.16.32 26-15 CANI Clock Select Register C3CLKR H00 HFFFF 8647 HFFFF 8647 8.16.32 26-15 CANI Clock Select Register C3CLKR H00 HFFFF 8647 HFFFF 8647 8.16.32 26-15 CANI Clock Select Register C3CLKR H00 HFFFF 8647 HFFFF 8647 8.16.32 26-15 CANI Clock Select Register C3CLKR H00 HFFFF 8647 HFFFF 8647 8.16.32 26-15 CANI Clock Select Register C3CLKR H00 HFFFF 8647 HFFFF 8647 16.32 26-15 CANI Clock Select Register C3CLKR H00 HFFFF 8647 HFFFF 8647 16.32 26-1				Figure 24.12 RSPI Transfer Format (CPHA = "1") : Incorrect description is corrected. Error:
Added in Rev. B 26-5 Table 26.3 Register Configuration Table 26.3 Register Configuration Table 26.3 Register Configuration Register Name Abbreviation Rest Configuration Abbreviation Rest Configuration After Rest From Configuration Page Configuration Abbreviation Rest Configuration After Rest Configuration Page Configuration Added in Rev. B 26-5 Table 26.3 Register Configuration Table 26.3 Register Name Configuration After Reset Configuration Abbreviation After Reset Configuration After Reset Configuration Page Configuration Added in Rev. B 26-5 Table 26.3 Register Configuration Table 26.3 Register Name Configuration After Reset Configuration Page Configuration After Reset Configuration Page Reset Configuration Page Reset Configuration After Reset Configuration Page Reset Configuration Page Reset Reset Configuration Pa Address Reset Reset Reset Reset Reset Reset Reset Reset Reset Res	in	24-35	RSPI Transfer Format	RSPCKi (CPOL = "0") RSPCK (CPOL = "1") Sampling timing MOSIi MISOi SSLi tit
Added in Rev. B 26-5 Table 26.3 Register Configuration The values after reset of the CANi Clock Select Register (CiCLKR) (i = 0 to 3) are corrected. Error: Added in Rev. B 26-5 Table 26.3 Register Configuration The values after reset of the CANi Clock Select Register (CiCLKR) (i = 0 to 3) are corrected. Error: Register Name Abbreviation After H00 HTFFFF 6847 8, 16, 32 26-15 CANI Clock Select Register COLKR H00 HTFFFF 8847 8, 16, 32 26-15 CANI Clock Select Register COLKR H00 HTFFFF 8847 8, 16, 32 26-15 CANI Clock Select Register COLKR H00 HTFFFF 8847 8, 16, 32 26-15 CANI Clock Select Register COLKR H00 HTFFFF 8847 8, 16, 32 26-15 CANI Clock Select Register COLKR H00 HTFFFF 8847 8, 16, 32 26-15 CANI Clock Select Register COLKR Undefined HTFFF 7847 8, 16, 32 26-15 CANI Clock Select Register COLKR Undefined HTFFF 7847 8, 16, 32 26-15 CANI Clock Select Register COLKR Undefined HTFFF 7847 8, 16, 32 26-15 CANI Clock Select Register COLKR Undefined HTFFF 7847<				Start Serial transfer period End
Added rable 26.3 Rev. B 26-5 Table 26.3 Register Name Added HOR in Register CAND Clock Select Register C2CLKR HOQ H*FFFF 7847 8, 16, 32 26-5 Register Correction: Register Register CAND Clock Select Register C2CLKR HOQ H*FFFF 7847 8, 16, 32 26-5 Register Configuration After Register Name Abbreviation After HOQ H*FFFF 7847 8, 16, 32 26-5 CANO Clock Select Register COLKR HOQ H*FFFF 7847 8, 16, 32 26-5 : CANO Clock Select Register C2CLKR CANO Clock Select Register C3CLKR CANO Clock Select Register C3CLKR <				
Added in Rev. B 26-5 Table 26.3 Register Configuration The values after reset of the CANi Clock Select Register (CiCLKR) (i = 0 to 3) are corrected. Error: Added in Rev. B 26-5 Table 26.3 Register Configuration The values after reset of the CANi Clock Select Register (CiCLKR) (i = 0 to 3) are corrected. Error: Register Name Abbreviation After Reset P4 Address Size Page CAN0 Clock Select Register COLKR H'00 H'FFFF 7847 8, 16, 32 26-15 CAN2 Clock Select Register C2LKR H'00 H'FFFF 7847 8, 16, 32 26-15 CAN2 Clock Select Register C2LKR H'00 H'FFFF 9847 8, 16, 32 26-15 CAN3 Clock Select Register C3LKR H'00 H'FFFF 9847 8, 16, 32 26-15 CAN3 Clock Select Register C3LKR H'00 H'FFFF 9847 8, 16, 32 26-15 CAN0 Clock Select Register C3LKR Undefined H'FFFF 7847 8, 16, 32 26-15 CAN0 Clock Select Register C3LKR Undefined H'FFFF 7847 8, 16, 32 26-15 CAN1 Clock Select Register C1LKR Undefined H'FFFF 7847 8, 16, 32 2				(CPOL = "0")
Added in Rev. B26-5Table 26.3 Register ConfigurationTable 26.3 Register ConfigurationTable 26.3 Register ConfigurationTable 26.3 Register ConfigurationTable 26.3 Register CAN0 Clock Select Register COLKRH'00 H'D0 H'FFFF 7847H'FFF 7847 8, 16, 32 26-15BBAdded in Rev. B26-5Table 26.3 Register ConfigurationTable 26.4 Register COLKRAfter H'00 H'FFFF 7847Page H'FFFF 7847A 8, 16, 32 26-15Page 26-15CAN2 Clock Select Register ConfigurationC1CLKR H'00 H'FFFF 7847H'0, 32 26-15H'00 26-15CAN3 Clock Select Register ConfigurationC3CLKR H'00 H'FFFF 7847H'0, 32 26-15H'00 26-15CAN3 Clock Select Register CAN0 Clock Select Register COLKRC3CLKR Undefined H'FFFF 7847H 6, 32 26-15Page 26-15CAN1 Clock Select Register CAN1 Clock Select Register COLKRC3CLKR Undefined H'FFFF 7847H 6, 32 26-15CAN2 Clock Select Register CAN1 Clock Select Register C2CLKRC3CLKR Undefined H'FFFF 7847H 6, 32 26-15CAN2 Clock Select Register C3CLKRC3CLKR Undefined H'FFFF 7847H 6, 32 26-15CAN2 Clock Select Register C3				
Added in Rev. B26-5Table 26.3 Register ConfigurationRegister NameAbbreviation COLKRResetP4 AddressSizePage SizeAdded in Rev. B26-5Table 26.3 Register ConfigurationTable 26.3 Register CAN2 Clock Select RegisterC2CLKRH'00H'FFFF 78478, 16, 3226-15CAN2 Clock Select RegisterC2CLKRH'00H'FFFF 88478, 16, 3226-15CAN3 Clock Select RegisterC3CLKRH'00H'FFFF 98478, 16, 3226-15CAN0 Clock Select RegisterCOLKRUndefinedH'FFFF 88478, 16, 3226-15CAN1 Clock Select RegisterC1CLKRUndefinedH'FFFF 88478, 16, 3226-15CAN1 Clock Select RegisterC1CLKRUndefinedH'FFFF 78478, 16, 3226-15CAN2 Clock Select RegisterC1CLKRUndefinedH'FFFF 78478, 16, 3226-15CAN2 Clock Select RegisterC2CLKRUndefinedH'FFFF 78478, 16, 3226-15CAN2 Clock Select RegisterC2CLKRUndefinedH'FFFF 78478, 16, 3226-15CAN2 Clock Select RegisterC2CLKR				corrected.
Added in Rev. B26-5Table 26.3 Register ConfigurationTable 26.3 Register ConfigurationTable 26.3 Register CANO Clock Select RegisterCICLKRH'00 H'00 H'FFFF 8847H'FFF 8847 8, 16, 32 26-158, 16, 32 26-1526-55 1CAN2 Clock Select Register ConfigurationC2CLKRH'00 H'00 H'FFFF 8847H'FFFF 8847 8, 16, 32 26-158, 16, 32 26-1526-15CAN3 Clock Select Register ConfigurationC3CLKRH'00 H'00 H'FFFF 9847H'FFF 9847 8, 16, 32 26-158, 16, 32 26-15CAN3 Clock Select Register ConfigurationC3CLKRH'00 H'00 H'FFFF 9847H'FFF 9847 8, 16, 32 26-15Correction:Image: CaN3 Clock Select Register ConfigurationAfter ResetP4 Address P4 AddressSize Page 26-15CAN1 Clock Select Register C1CLKRC1CLKR Undefined H'FFFF 7847N, 16, 32 26-1526-15CAN1 Clock Select Register C1CLKRC1CLKR Undefined H'FFFF 7847N, 16, 32 26-1526-15CAN2 Clock Select Register C1CLKRC1CLKR Undefined H'FFFF 7847N, 16, 32 26-1526-15CAN2 Clock Select Register C2CLKRC2CLKR Undefined H'FFFF 8847N,				
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Register NameAbbreviationAfter ResetP4 AddressSizePageCAN0 Clock Select RegisterCOCLKRUndefinedH'FFFF 68478, 16, 3226-15::::::::CAN1 Clock Select RegisterC1CLKRUndefinedH'FFFF 78478, 16, 3226-15::::::::CAN1 Clock Select RegisterC1CLKRUndefinedH'FFFF 78478, 16, 3226-15::::::::CAN2 Clock Select RegisterC2CLKRUndefinedH'FFFF 88478, 16, 3226-15:::::::::		26-5		
Register NameAbbreviationResetP4 AddressSizePageCAN0 Clock Select RegisterCOCLKRUndefinedH'FFF 68478, 16, 3226-15::::::::CAN1 Clock Select RegisterC1CLKRUndefinedH'FFF 78478, 16, 3226-15::::::::CAN1 Clock Select RegisterC1CLKRUndefinedH'FFF 78478, 16, 3226-15::::::::CAN2 Clock Select RegisterC2CLKRUndefinedH'FFF 88478, 16, 3226-15::::::::	Rev. B			Correction:
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CAN1 Clock Select Register C1CLKR Undefined H'FFFF 7847 8, 16, 32 26-15 : <td:< td=""> : : <td:< td=""></td:<></td:<>				CAN0 Clock Select Register C0CLKR Undefined H'FFFF 6847 8, 16, 32 26-15
CAN2 Clock Select Register C2CLKR Undefined H'FFFF 8847 8, 16, 32 26-15 : <td:< td=""> <td:< td=""></td:<></td:<>				CAN1 Clock Select Register C1CLKR Undefined H'FFFF 7847 8, 16, 32 26-15
				CAN2 Clock Select Register C2CLKR Undefined H'FFFF 8847 8, 16, 32 26-15



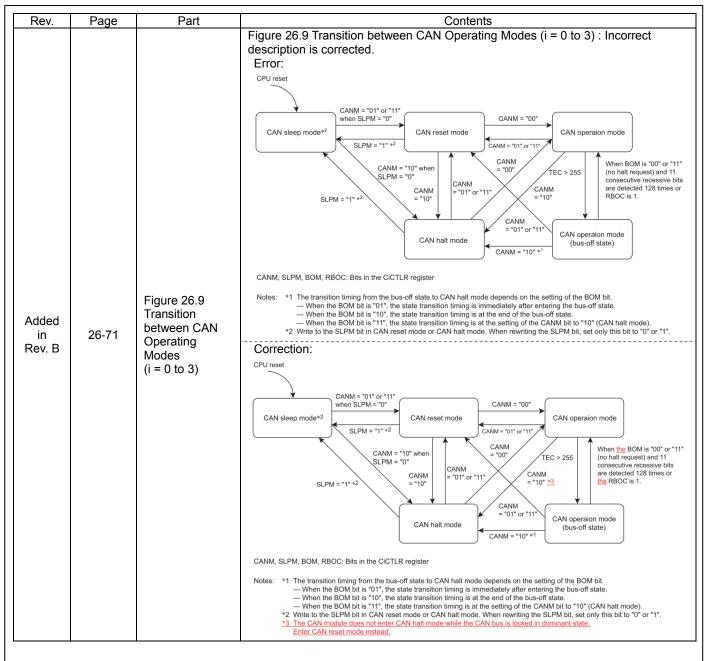
20.0.0	to 3) is c Error:	Bit:		6 -	in the	CANi 4	Clock Se	lect Reg	gister (C	iCLKR) (i =
20.0.0			-	-	5	4	3	2	1	0
20.0.0	After		-	-	_	· ·	•			0
20.0.0	After	Reset:	0			_	_	_	_	CCLKS
22.2.2				0	0	<u>0</u>	0	0	0	0
00.0.0				••					<aft< td=""><td>er Reset: <u>H'0</u></td></aft<>	er Reset: <u>H'0</u>
00.0.0	Bit	Abbrevia	ation	After Reset	R	w	Descripti	on		
26.3.2 CANi Clock	4	_		<u>0</u>	?	0	Reserved Should be	Bit e written	with "0"	and read a
Select Register (CiCLKR)							undefined	value.		
(i = 0 to 3)	Correct	tion:								
		Bit:	7	6	5	4	3	2	1	0
	Δfter	Reset:	0	-	-			0	0	CCLKS
	7 (10)	110301.	0	U	<u> </u>	JIIdelli		-	-	°,
								<	After Re	set: Undefine
				After	_					
		Abbrevia								
	т	_		ondenne	<u>.u</u> :	U	Should be	e written	with "0"	and read a
							undefined	value.		
								Ni Rece	vive FIF	O Pointer
26 3 11				After						
CANi Receive	Bit			Reset						
FIFO Pointer	7 to 0	CIRFPCR	<	Undefine	a <u>R</u>	vv				
	Correc	tion:								
(i = 0 to 3)				After						
	Bit			Reset					inter fo	
	7 to 0	CIRFPUR	K	Undefine	ea <u>′</u>	VV				
								Ni Trans	smit FIF	O Pointer
	Error:	Register (CITEP	'CR) (I =	0 to 3) IS CO	prrected.			
26.3.13 CANi Transmit FIFO Pointer				After	_					
									inter for	the transm
				2						
	Correct	tion:								
(i = 0 to 3)				After						
	Bit 7 to 0			Reset						
		CITFPCR	2	Undefine	ed ?	W		مما ماما	inter for	the transmi
	26.3.11 CANi Receive FIFO Pointer Control Register (CiRFPCR) (i = 0 to 3) 26.3.13 CANi Transmit FIFO Pointer Control Register (CiTFPCR)	(i = 0 to 3) After Control Error: 26.3.11 CANi Receive FIFO Pointer Control Register (CiRFPCR) (i = 0 to 3) Bit 7 to 0 Correct Bit 7 to 0 Error: 26.3.13 CANi Transmit FIFO Pointer Control Register (CiTFPCR) (i = 0 to 3) Bit 7 to 0 Correct Correct Correct Correct Correct Correct After A	(i = 0 to 3) Correction: Bit Abbrevia 4 - 26.3.11 Setting value of the Control Register (Control Register (Cirreption)) CANi Receive Bit Abbrevia 7 to 0 Cirreption) (i = 0 to 3) Bit Abbrevia 26.3.13 Setting value of the Control Register (Cirreption) Correction: Bit Abbrevia 7 to 0 Cirreption) 26.3.13 Setting value of the Control Register (Cirreption) Bit Abbrevia 26.3.13 Setting value of the Control Register (Cirreption) Bit Abbrevia 7 to 0 Cirreption Correction: Correction: 26.3.13 Bit Abbrevia 7 to 0 Cirreption 26.3.13 CANi Transmit FifO Pointer Correction: Correction: 26.3.13 CANi Transmit Fito 0 Correction: Error: 26.3.13 Bit Abbrevia Correction: Error: 26.3.13 Bit Abbrevia Error: Error: Error: 26.3.13 Bit Abbrevia Err	(i = 0 to 3)Correction:BitAbbreviationAfter Reset:0BitAbbreviation4-26.3.11Setting value of the bit 7CANi ReceiveSetting value of the bit 7FIFO PointerControl Register (CiRFPCR)(i = 0 to 3)BitAbbreviation7 to 026.3.13Setting value of the bit 7Control RegisterCorrection:(i = 0 to 3)BitAbbreviation7 to 0Control RegisterCorrection:26.3.13Setting value of the bit 7Control RegisterControl Register (CiTFPControl RegisterCorrection:26.3.13BitCANi TransmitFiFO PointerControl RegisterCorrection:(i = 0 to 3)BitAbbreviation(i = 0 to 3)BitBitAbbreviation	(i = 0 to 3) Correction: Bit Abbreviation After Reset: 0 Control Register (CiRFPCR) 0 Cirection: After Reset To 0 CiRFPCR Undefine Correction: Bit Abbreviation After Reset To 0 Control Register (CiTFPCR) (i = Error: After Reset Control Register (CiTFPCR) After Reset To 0 Control Register (CiTFPCR) After Reset After Reset To 0 CiTFPCR Undefine Correction: After Reset To 0 CiTFPCR Undefi	(i = 0 to 3) Correction: Bit Abbreviation Reset R After Reset: 0 0 0 1 Bit Abbreviation Reset R 4 - Undefined ? 26.3.11 Setting value of the bit 7 to 0 (CiRFPC Control Register (CiRFPCR) (i = 0 to 3) After 26.3.11 CANi Receive FIFO Pointer Control Register (CiRFPCR) After Correction: Bit Abbreviation Reset R 7 to 0 CiRFPCR Undefined ? Correction: (i = 0 to 3) Setting value of the bit 7 to 0 (CiTFPCR Undefined ? Correction: 26.3.13 Setting value of the bit 7 to 0 (CiTFPCR Undefined ? Setting value of the bit 7 to 0 (CiTFPCR) (i = 0 to 3) 26.3.13 Setting value of the bit 7 to 0 (CiTFPCR) (i = 0 to 3) Error: After 26.3.13 Bit Abbreviation Reset R 7 to 0 CiTFPCR Undefined ? Correction: (i = 0 to 3) Bit Abbreviation Reset R 7 to 0 CiTFPCR Undefined R	(i = 0 to 3) Image: Correction: Bit 7 6 5 4 After Reset: 0 0 0 Undefined After Reset: 0 0 0 Undefined 7 After Reset: 0 0 0 Undefined 7 0 After Reset: 0 0 0 Undefined 7 0 After Reset: 0 0 0 Undefined 7 0 26.3.11 CANI Receive FIFO Pointer Control Register (CiRFPCR) After Reset R W Correction: 6 After Reset R W Correction: Correction: After Reset R W Control Register (CiRFPCR) Undefined ? W Correction: Correction: After Reset R W Control Register (CiRFPCR) Undefined ? W W Control Register (CiTFPCR) Undefined ? W W 26.3.13 Setting value of the bit 7 to 0 (CiTFPCR bit) Control Register (CiTFPCR) I = 0 to 3)	(i = 0 to 3) Bit 7 6 5 4 3 Bit After Reset: 0 0 0 Undefined 0 After Reset: 0 0 0 Undefined 0 0 After Reset: 0 0 0 Correction: 0 Reserved Setting value of the bit 7 to 0 (CiRFPCR bit) in the CA Control Register (CiRFPCR) (i = 0 to 3) Setting value of the bit 7 to 0 (CiTFPCR bit) in the CA Control Register (CiRFPCR) Undefined 2 W The CPL FIFO is in Correction: If Abbreviation Reset R W Descripti 7 to 0 CiRFPCR Undefined 2 W The CPL FIFO is in Control Register Control Register (CiTFPCR) I = 0 to 3) is corrected. Error: 26.3.13 Setting value of the bit 7 to 0 ((i = 0 to 3) Correction: Bit 7 6 5 4 3 2 After Reset: 0 0 0 Undefined 0 0 After Reset: R W Description Setting value of the bit 7 to 0 (CIRFPCR bit) in the CANi Receed Control Register (CiRFPCR) (i = 0 to 3) is corrected. Error: After Reset R W Description 7 to 0 CIRFPCR Undefined R W The CPU-side por FIFO is increments Correction: If a Abbreviation Reset R W Description 7 to 0 CIRFPCR Undefined 2 W The CPU-side por FIFO is increments Control Register Control Register (CiTFPCR) (i = 0 to 3) is corrected. Error: After Reset R W Description 7 to 0 CIFPCR Undefined	(i = 0 to 3) Correction: Bit 7 6 5 4 3 2 1 After Reset: 0 0 0 Undefined 0 <td< td=""></td<>



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Rev. Added in Rev. B	Page 26-56	Part 26.3.20 CANi Error Interrupt Factor Judge Register (CiEIFR) (i = 0 to 4)) (i = 0 to 4 Abbreviation BLIF) IS COI After Reset 0 After	R R	w w	t) in the CANi Error Interrupt Factor Judge Register
	L		 				•
			 				 After this bit is set to "0" from "1", recessive bits are detected (bus lock is resolved). After this bit is set to "0" from "1", the CAN module enters CAN reset mode and then enters CAN operation mode again (internal reset). 0: No bus lock detected 1: Bus lock detected



Date: October 1, 2013





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	~		Table 26.9 Op description is Error:	eration in CAN Reset corrected.	t Mode and CAN Halt	Mode : Incorrect
			Mode	Receiver	Transmitter	Bus-Off
			CAN reset mode (forcible transition) CANM = "11"	CAN module enters CAN	CAN module enters CAN reset mode without waiting for	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
			CANM = "11 CAN reset mode CANM = "01"	CAN module enters CAN reset mode without waiting for the end of message reception.	reset mode after waiting for	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
			CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception* ² * ³ .	mode after waiting for the end of message transmission* ¹ * ⁴ .	[When the BOM bit is "00"] A halt request from a program will be acknowledged only after bus-off recovery. [When the BOM bit is "01"] CAN module enters automatically to CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is "10"] CAN module enters automatically to CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is "11"] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.
Added in	26-73	Table 26.9 Operation in CAN Reset	Notes: *1 If sever transmit transitio *2 If the C/ the CiEl *3 If a CAN halt moo *4 If a CAN	ssion. In a case that the CAN re n occurs when the bus is idle, th AN bus is locked <u>at the</u> dominar IFR register. I bus error occurs during recept de.	e transmitted, mode transition o set mode is being requested du ne next transmission ends, or th tt <u>level</u> , the program can detect ion after CAN halt mode is requ curs during transmission after C	ccurs after the completion of the first ring suspend transmission, mode e CAN module becomes a receiver. this state by monitoring the BLIF bit in ested, the CAN <u>mode transits to</u> CAN AN reset mode or CAN halt mode is
Rev. B		Mode and CAN	Mode	Receiver	Transmitter	Bus-Off
		Halt Mode	CAN reset mode (forcible transition) CANM = "11"	CAN module enters CAN reset mode without waiting for the end of message reception.	t CAN module enters CAN rese mode without waiting for the e of message transmission.	
			CAN reset mode CANM = "01"	CAN module enters CAN reset mode without waiting for the end of message reception.	t CAN module enters CAN rese mode after waiting for the end message transmission.* ¹ * ⁴ .	et CAN module enters CAN reset of mode without waiting for the end of bus-off recovery.
			CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception.* ² * ³ .	CAN module enters CAN halt mode after waiting for the end message transmission. *1a ² a ⁴ .	[When the BOM bit is "00"] of A halt request from a program will be acknowledged only after bus-off recovery. [When the BOM bit is "01"] CAN module enters automatically to CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from
						(regardless of a hair request non- a program). [When the BOM bit is "10"] CAN module enters automatically to CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is "11"] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.
			Notes: *1 If severa transmis transitio *2 If the C/ CiEIFR	ssion. In a case that the CAN re n occurs when the bus is idle, th AN bus is locked <u>in</u> dominant <u>sta</u>	e transmitted, mode transition o set mode is being requested du ne next transmission ends, or th ate, the program can detect this	ccurs after the completion of the first ring suspend transmission, mode e CAN module becomes a receiver. state by monitoring the BLIF bit in the the CAN bus is locked in dominant
			*3 If a CAN			ested, the CAN <u>module enters</u> CAN



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Added in Rev. B	28-11	28.3 Register Descriptions	 28.3 Register Descriptions : Incorrect description is corrected. Error: These flags are used to enable DMA transfer requests. Set these flags to "1" to enable a DMA transfer request, and set them to "0" to disable a request. To prevent incorrect DMA operation, only rewrite these bits from the DMA transfer masked state to the DMA transfer enabled state when DRI acquisition is enabled (DRIiDCAPCNT.DCPEN bit = "1"). Do not rewrite from the DMA transfer enabled state to the DMA transfer masked state when DRI acquisition is enabled (DRIiDCAPCNT.DCPEN bit = "1"). Do not rewrite from the DMA transfer enabled state to the DMA transfer masked state when DRI acquisition is enabled, since that can result in a DMA request not being handled. Correction: These flags are used to enable DMA transfer requests. Set these flags to "1" to enable a DMA transfer request, and set them to "0" to disable a DMA transfer request. To prevent incorrect DMA operation, only rewrite these bits from the DMA transfer request masked state to the DMA transfer request enabled state when DRI acquisition is enabled (DRIiDCAPCNT.DCPEN bit = "1"). Do not rewrite from the DMA transfer request enabled state to the DMA transfer request enabled state when DRI acquisition is enabled (DRIiDCAPCNT.DCPEN bit = "1"). Do not rewrite from the DMA transfer request enabled state to the DMA transfer request masked state when DRI acquisition is enabled.
Added in Rev. B	28-16	28.3.4 DRI0DIN DMA Transfer Enable Register (DRI0DINDEN)	28.3.4 DRI0DIN DMA Transfer Enable Register (DRI0DINDEN) : Incorrect description is corrected. Error: Also note that it is only possible to rewrite the DRI0DINDEN register bits from the transfer masked state to the transfer enabled state when DRI acquisition is enabled (DRIDCAPCNT.DCPEN bit = "1"). Do not rewrite from the transfer enabled state to the transfer masked state when DRI acquisition is enabled. Correction: Also note that it is only possible to rewrite the DRI0DINDEN register bits from the DMA acquisition is enabled. Correction: Also note that it is only possible to rewrite the DRI0DINDEN register bits from the DMA transfer request masked state to the DMA transfer request enabled state when DRI acquisition is enabled (DRIDCAPCNT.DCPEN bit = "1"). Do not rewrite from the DMA transfer request enabled state to the DMA transfer request enabled state to the DMA transfer request enabled state to the DMA transfer request masked state to the DMA transfer request enabled state to the DMA transfer request enabled state to the DMA transfer request masked state when DRI acquisition is enabled.
Added in Rev. B	28-21	28.3.8 DRI0DEC DMA Transfer Enable Register (DRI0DECDEN)	28.3.8 DRIODEC DMA Transfer Enable Register (DRIODECDEN) : Incorrect description is corrected. Error: If a DMA transfer request mask (disable) setting and an internal DMA transfer request occur at the same time, the DMA transfer request mask (disable) setting takes precedence. Also note that it is only possible to rewrite the DRIODECDEN register bits from the transfer masked state to the transfer enabled state when DEC counter operation is enabled (DRIDECnCNT.DECnEN bit = "1"). Do not rewrite from the transfer enabled state to the transfer masked state when DEC counter operation is enabled. Correction: If a DMA transfer request mask (disable) setting and an internal DMA transfer request mask (disable) setting takes precedence. Also note that it is only possible to rewrite the DRIODECDEN register bits from the transfer request mask (disable) setting takes precedence. Also note that it is only possible to rewrite the DRIODECDEN register bits from the DMA transfer request masked state to the DMA transfer request enabled state when DEC counter operation is enabled. Correction: If a DMA transfer request mask (disable) setting and an internal DMA transfer request mask (disable) setting takes precedence. Also note that it is only possible to rewrite the DRIODECDEN register bits from the DMA transfer request masked state to the DMA transfer request enabled state when DEC counter operation is enabled (DRIIDECnCNT.DECnEN bit = "1"). Do not rewrite from the DMA transfer request enabled state to the DMA transfer request masked state to the DMA transfer request masked state when DEC counter operation is enabled.



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1.001.		i dit	28.3.12 DRI0 DMA Transfer Enable Register (DRI0TRMDEN) : Incorrect
			description is corrected.
Added in Rev. B	28-27	28.3.12 DRI0 DMA Transfer Enable Register (DRI0TRMDEN)	 Error: Controls the enabled/disabled states for DRI0 transfer related DMA transfer requests. If one of these bits is set to "1", the corresponding DMA transfer request signal output is enabled. If a DMA transfer mask (disable) is set at the same time as an internal DMA transfer request, the DMA transfer mask (disable) takes precedence. Also note that when DRI acquisition is enabled (DRIiDCAPCNT.DCPEN bit = "1"), the DRI0TRMDEN register may only be rewritten from the transfer masked state to the transfer enabled state. Do not rewrite any bits in this register from the transfer enabled state to the transfer masked state when DRI acquisition is enabled. Correction: Controls the enabled/disabled states for DRI0 transfer related DMA transfer requests. If one of these bits is set to "1", the corresponding DMA transfer request signal output is enabled. If a DMA transfer mask (disable) is set at the same time as an internal DMA transfer mask (disable) is set at the same time as an internal DMA transfer mask (disable) is set at the same time as an internal DMA transfer request, the DMA transfer mask (disable) takes precedence. Also note that when DRI acquisition is enabled (DRIiDCAPCNT.DCPEN bit = "1"), the DRI0TRMDEN register may only be rewritten from the DMA transfer request masked state to the DMA transfer request enabled state. Do not rewrite any bits in this register from the DMA transfer request masked state to the DMA transfer request enabled state. Do not rewrite any bits in this register from the DMA transfer request enabled state to the DMA transfer request masked state to the DMA transfer request enabled state. Do not rewrite any bits in this register from the DMA transfer request enabled state to the DMA transfer request masked state to the DMA transfer request enabled state. Do not rewrite any bits in this register from the DMA transfer request enabled state to the DMA transfer request masked state to the DMA transfer request masked state to the DMA transfer request masked state to the DM
			Description of the bit 2 (FBSEN bit) in the FlexRay Operation Control Register
امعامام		32.4.1	(FXROC) is corrected.
Added in	32-13	FlexRay Operation	Error: - FRNVMn
Rev. B	02 10	Control Register	- FRNVMn
		(FXROC)	Correction: - <u>FRNMVn</u> - FRNMVn
Added in Rev. B	32-139	32.12.5 Configuration of NIT Start and Offset Correction Start	 32.12.5 Configuration of NIT Start and Offset Correction Start : Incorrect description is corrected. Error: For the FlexRay module the offset correction start is required to be the OCS bit in the FRGTUC4 register <u>o</u> the NIT bit <u>int</u> the FRGTUC4 register + 1 = k+1. Correction: For the FlexRay module the offset correction start is required to be the OCS bit in the FRGTUC4 register ≥ the NIT bit <u>in</u> the FRGTUC4 register + 1 = k+1.
			Table 32.8 State Transitions of FlexRay overall state Machine : Incorrect description is corrected.
			Error: T# Condition From To
			T1 Hard reset All states DEFALT CONFIG
			T2 Command CONFIG, bits CMD3 to <u>DEFALT CONFIG</u> CONFIG CMD0 in the FRSUCC1 register = B'0001
Added	Table 32.8 State Transitions	T15 Command CONFIG, bits CMD3 to HALT DEFALT_CONFIG CMD0 in the FRSUCC1 register = B'0001	
in Rev. B	32-145	of FlexRay overall state	
1.0V. D		overall state Machine	Correction:
			T# Condition From To
			T1 Hard reset All states DEFAULT CONFIG T2 Command CONFIG, bits CMD3 to CMD0 in the FRSUCC1 register = B'0001 DEFAULT CONFIG CONFIG
		T15 Command CONFIG, bits CMD3 to HALT <u>DEFAULT CONFIG</u> CMD0 in the FRSUCC1 register = B'0001	

