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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SY*-A0068A/E	Rev.	1.00
Title	S124 MCU Group, S128 MCU Group, S1JA MCU Group, S3A1 MCU Group, S3A3 MCU Group, S3A6 MCU Group, S3A7 MCU Group, addition of SPI Data Control Register (SPDCR) bit		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S124 MCU Group Renesas Synergy™ S128 MCU Group Renesas Synergy™ S1JA MCU Group Renesas Synergy™ S3A1 MCU Group Renesas Synergy™ S3A3 MCU Group Renesas Synergy™ S3A6 MCU Group Renesas Synergy™ S3A7 MCU Group	Lot No. All	Reference Document	S124 Microcontroller Group User's Manual Rev.1.30 S128 Microcontroller Group User's Manual Rev.1.10 S1JA Microcontroller Group User's Manual Rev.1.40 S3A1 Microcontroller Group User's Manual Rev.1.20 S3A3 Microcontroller Group User's Manual Rev.1.10 S3A6 Microcontroller Group User's Manual Rev.1.20 S3A7 Microcontroller Group User's Manual Rev.1.40		

The SPBYT bit of SPI Data Control Register (SPDCR) is added.

[before] example: S124

SPI Data Control Register (SPDCR)

Address(es): SPI0.SPDCR 4007 200Bh, SPI1.SPDCR 4007 210Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SPLW	SPRDTD	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SPRDTD	SPI Receive/Transmit Data Select	0: Read SPDR/SPDR_HA values from receive buffer 1: Read SPDR/SPDR_HA values from transmit buffer, but only if the transmit buffer is empty.	R/W
b5	SPLW	SPI Word Access/Halfword Access Specification	0: Set SPDR_HA to valid for halfword access 1: Set SPDR to valid for word access.	R/W
b7 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPRDTD bit (SPI Receive/Transmit Data Select)

The SPRDTD bit selects whether the SPDR/SPDR_HA reads values from the receive buffer or from the transmit buffer. If reading is from the transmit buffer, the last value written to SPDR/SPDR_HA register is read. Read the transmit buffer after generation of the transmit buffer empty interrupt (when SPSR.SPTEF is 1).

For details, see section 28.2.5, SPI Data Register (SPDR/SPDR_HA).

SPLW bit (SPI Word Access/Halfword Access Specification)

The SPLW bit specifies the access width for the SPDR register. Access to SPDR_HA in halfwords is valid when the SPLW bit is 0 and access to the SPDR register in words is valid when the SPLW bit is 1. In addition, when the

SPLW bit is 0, set the SPCMD0.SPB[3:0] bits (SPI data length setting bits) from 8 to 16 bits. When 20, 24, or 32 bits is specified, do not perform any operations.

[after]

SPI Data Control Register (SPDCR)

Address(es): SPI0.SPDCR 4007 200Bh, SPI1.SPDCR 4007 210Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SPBYT	SPLW	SPRDTD	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SPRDTD	SPI Receive/Transmit Data Select	0: Read SPDR/SPDR_HA values from receive buffer 1: Read SPDR/SPDR_HA values from transmit buffer, but only if the transmit buffer is empty.	R/W
b5	SPLW	SPI Word Access/Halfword Access Specification	0: Set SPDR_HA to valid for halfword access 1: Set SPDR to valid for word access.	R/W
b6	SPBYT	SPI Byte Access Specification	0: SPDR is accessed in halfword or word (SPLW is valid) 1: SPDR is accessed in byte (SPLW is invalid).	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

SPRDTD bit (SPI Receive/Transmit Data Select)

The SPRDTD bit selects whether the SPDR/SPDR_HA reads values from the receive buffer or from the transmit buffer. If reading is from the transmit buffer, the last value written to SPDR/SPDR_HA register is read. Read the transmit buffer after generation of the transmit buffer empty interrupt (when SPSR.SPTEF is 1).

For details, see section of SPI Data Register (SPDR/SPDR_HA).

SPLW bit (SPI Word Access/Halfword Access Specification)

The SPLW bit specifies the access width for the SPDR register. Access to SPDR_HA in halfwords is valid when the SPLW bit is 0 and access to the SPDR register in words is valid when the SPLW bit is 1. In addition, when the SPLW bit is 0, set the SPCMD0.SPB[3:0] bits (SPI data length setting bits) from 8 to 16 bits. When 20, 24, or 32 bits is specified, do not perform any operations.

SPBYT bit (SPI Byte Access Specification)

This bit is used to set the data width of access to the SPI Data Register (SPDR). When SPBYT = 0, use word or half word access to SPDR. When SPBYT = 1 (in that case, SPLW is invalid), use byte access to SPDR. When SPBYT = 1, set the SPI data length bits (SPB[3:0]) in the SPI Command Register n (SPCMDn) to 8 bits. If SPB[3:0] are set to 9 to 16, 20, 24, or 32 bit, subsequent operation is not guaranteed.