RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan Renesas Electronics Corporation

Product Category	MPU/MCU	Document No.	TN-RZ*-A047A/E	Rev.	1.00	
Title	RZ/T1 Group User's Manual: Hardware Correction and adding notifications about Eth and EtherCAT Slave Controller	Information Category	Technical Notification			
		Lot No.				
Applicable Product			Reference Document	RZ/T1 Group User's Manual: Hardw R01UH0483EJ0130 R		1.30

Correction and adding notification about EtherMAC and EtherCAT Slave Controller.

Correction of manual are below.

• Correction of EtherMAC:

No.	Page		Current description	า	Correct description
1	1324	28.2.2.5 RX Mode Register (GMAC_RXMODE) Function description of b31 AFILLTEREN 1 : Enables address filtering			28.2.2.5 RX Mode Register (GMAC_RXMODE) Function description of b31 AFILLTEREN 1 : Enables address filtering ^{Note} [Note] Even though Address filtering is enabled, MAC Control Frames (ex. Pause Packet) are always received regardless contents of MAC Address Register. MAC Control Frame is the frame tha the destination address is 01-80-C2-00-00-01.
2	1352	[Current description]28.3.1.3 (2) (e)Table 28.6 HWFNC_LongBuffer_GetArgument registersR4[15:0]Buffer LengthR4[23:16]ReservedAlways 0R4[31:24]UnusedR5[31:0]UnusedR6[31:0]UnusedR7[31:0]Unused			uffer length. Unit: bytes. 1 to 2048
		Return value re R0[1:0] R0[28:2]	gisters Result Unused		0xb and R0[29] = 1: Success 10b: Invalid system call 11b: The buffer is insufficient All 0
		R0[29]	Complete		0: Hardware function call not completed 1: Hardware function call completed
		R0[31:30]	Unused		All 0
		R1[31:0]	First logical add buffer	[31:27] 00001b [26] 1 [25:18] LLID [17:0] 0	



28.3.1.3 (2) (e)						
	28.6 HWFNC_LongBuffer_Ge	et				
Argum	ent registers					
R4	[15:0] Buffer Length	Required buffer length. Unit: bytes. 1 to 2048.				
	[23:16]	Reserved bits. Always set to 0				
	[31:24]	Not used in this Function call. Settings are ignored.				
R5	[31:0]	Not used in this Function call. Settings are ignored.				
R6	[31:0]	Not used in this Function call. Settings are ignored.				
R7	[31:0]	Not used in this Function call. Settings are ignored.				
R0	[1:0] Result	0xb and R0[29] = 1: Success 10b: Invalid system call 11b: The buffer is insufficient				
	[28:2]	Reserved bits. Always set to 0				
	[28:2] [29] Complete					
		Reserved bits. Always set to 0 0: Hardware function call not completed				



3	1353		t descript	ion]				
		28.3.1.3						
		Table 28.7 HWFNC_Short_Buffer_Get Argument registers						
		R4[15		Buffer Length	Required	buffer length. Unit: bytes. 1 to 512.		
		R4[13		Unused	Required			
		R5[31		Unused				
		R6[31		Unused				
		R7[31		Unused				
			.0]	ondood				
			value regi	isters				
		R0[1:0	D]	Result		0xb: Success		
						10b: Invalid system call		
						11b: The buffer is insufficient		
		R0[28		Unused		All O		
		R0[29]]	Complete		0: Hardware function call not completed 1: Hardware function call completed		
		R0[31	·301	Unused		All 0		
		R1[31		First logical ad	dress of the	[31:27] 00001b		
]	buffer		[26] 0		
						[25:18] SBID		
						[18:0] 0		
			t descripti	ion]				
		28.3.1.3		IC_Short_Buffer_G	`ot			
			ent registe		bet			
		R4		Suffer Length	Required bu	ffer length. Unit: bytes. 1 to 512.		
			[31:16]	Longui		this Function call. Settings are ignored.		
		R5	[31:0]			this Function call. Settings are ignored.		
		R6				Not used in this Function call. Settings are ignored.		
		R7	[31:0]		Not used in	this Function call. Settings are ignored.		
		Det		- 4				
		Return R0	value regi [1:0] Re			0xb: Success		
		RU	[1.0] Ke	Suit		10b: Invalid system call		
						11b: The buffer is insufficient		
			[28:2]			Reserved bits. Always set to 0		
			[29] Co	mplete		0: Hardware function call not completed		
			[]			1: Hardware function call completed		
			[31:30]			Reserved bits. Always set to 0		
		R1	[31:0] F	First logical add	ress of the	[31:27] 00001b		
			buffer	-		[26] 0		
						[25:18] SBID		
						[17:0] 0		



4 1353		[Current description] 28.3.1.3 (2) (e)					
		Table 28.8 HWFNC_Buffer_Release					
			ent registe				
		R4[31	:0]	First logical addres		t logical address of the buffer to be released	
				of the buffer		value is returned in R1 following a call of	
						FNC_LongBuffer_Get or	
		D5[24	.01	Unused		FNC_ShortBuffer_Get.	
		R5[31 R6[31		Unused			
		R7[31		Unused	-		
			.0]	Ulluseu			
		Return	value reg	isters			
		R0[1:0		Result		0xb: Success	
		_				10b: Invalid system call	
						11b: A buffer is not definable at the given address.	
		R0[28		Unused		All O	
		R0[29]	Complete		0: Hardware function call not completed	
						1: Hardware function call completed	
		R0[31		Unused		All O	
		R1[31	[31:0] Unused		All 0		
				IC_Buffer_Release			
		R4		First logical address	0xh S	uccess	
			of the b			nvalid system call	
						buffer is not definable at the given address.	
		R5	[31:0]			sed in this Function call. Settings are ignored.	
		R6	[31:0]		Not used in this Function call. Settings are ignored.		
		R7	[31:0]		Not us	ed in this Function call. Settings are ignored.	
		Return	value reg	isters			
		R0	[1:0] Re			0xb: Success	
						10b: Invalid system call	
						11b: The buffer is insufficient	
			[28:2]			Reserved bits. Always set to 0	
	1		[29] Co	mplete		0: Hardware function call not completed	
			1			1: Hardware function call completed	
		R1	[31:30] [31:0]			Reserved bits. Always set to 0 Reserved bits. Always set to 0	



5	1354	[Current descrip	tion		
5	1554	28.3.1.3 (2) (e)	lion		
			NC_Buffer_Return		
		Argument regist	ers		
		R4[31:0]	First logical addres	s of	First logical address of the buffer to be released
			the buffer		The value is returned in R1 following a call of
					HWFNC_LongBuffer_Get or
		R5[31:0]	First logical addres	s of	HWFNC_ShortBuffer_Get. First address of the part for release (the part of the
		10[01.0]	the part for release	3 01	buffer at addresses beginning from this address is
					released)
		R6[31:0]	Unused		
		R7[31:0]	Unused		
		Doturn volue re	niatoro		
		Return value reg R0[2:0]	Result		00xb: Success
		10[2.0]	Result		010b: Invalid system call
					011b: A buffer has not been defined at the address
					specified by R4.
					100b: The buffer at the address specified by R5
		R0[28:3]	Unused		has already been released.
		R0[29]	Complete		0: Hardware function call not completed
		-1 -1			1: Hardware function call completed
		R0[31:30]	Unused		All 0
		R1[31:0]	Unused		All O
		[Correct descrip	tion		
		28.3.1.3 (2) (e)	lionj		
		Table 28.9 HWF	NC_Buffer_Return		
		Argument regist			
		R4 [31:0] of the	First logical address		t logical address of the buffer to be released value is returned in R1 following a call of
		or the	Duilei		FNC_LongBuffer_Get or
				HW	FNC_ShortBuffer_Get.
		R5 [31:0]	First logical address		t address of the part for release (the part of the
		of the	part for release		er at addresses beginning from this address is
		DC [24:0]			ased)
		R6 [31:0]			used in this Function call. Settings are ignored. used in this Function call. Settings are ignored.
				1101	
		Return value re	5		
		R0 [2:0] R	esult		00xb: Success
					010b: Invalid system call 011b: A buffer has not been defined at the address
					specified by R4.
					100b: The buffer at the address specified by R5 has
					already been released.
		[28:3]			Reserved bits. Always set to 0
		[29] Co	omplete		0: Hardware function call not completed
			1		1: Hardware function call completed
		[31:30] R1 [31:0]			Reserved bits. Always set to 0 Reserved bits. Always set to 0
					Reserved Dits. Always set 10 U
L	I	1			



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6	1359	28.3.1.4 (2) (b)				28.3.1.4 (2) (b), 2-1)
			ading and releasing a b			[Example of reading and releasing a buffer]
			15:0] read from the BI			(3) The bits [15:0] read from the BUFID are bits
		[26:11] of the	cquired b	uffer	[26:11] of the address where the acquired buffer	
		starts.			starts.	
			bits of the address			The individual bits of the address where the
			starts are configured a	as follows	•	acquired buffer starts are configured as follows.
		[31:27]: 000				[31:27]: 00001b
			ivalent to the bits [15:8			[26:19]: Equivalent to the bits [15:8] in the
			ID ([26] of the start ad			BUFID ([26] of the start address is
_	1000		ays 1; [25:19] are LBID	[6:0])		always 1; [25:19] are LLID[6:0])
7	1360	[Current descri	ption]			
		28.3.1.4 (2) (c)				
			/FNC_MACDMA_RX_En	able		
		Argument regis				
		R4[31:0]	Unused			
		R5[31:0]	Unused			
		R6[31:0]	Unused			
		R7[6:0]	Reserved	A	lways	0
		R7[31:8]	Unused			
			• .			
		Return value re				
		R0[0]	Result			
			·			valid system call*1
		R0[28:1]	Unused			
		R0[29]	Complete			ardware function call not completed
		Dolo4 ool				ardware function call completed
		R0[31:30]	Unused		All 0	
		R1[31:0]	Unused		All 0	
		Correct describ	ational .			
		[Correct descrip	btion]			
		28.3.1.4 (2) (c)	/FNC_MACDMA_RX_En	ahla		
		Argument regis		able		
		R4 [31:0]		Notus	od in t	his Function call. Settings are ignored.
		R5 [31:0]				his Function call. Settings are ignored.
		R6 [31:0]				his Function call. Settings are ignored.
		R7 [31:0]				this Function call. Settings are ignored.
				NOUUS	eu III	une i uncuon can. settings are ignoreu.
		Return value re	aisters			
		R0 [0] Re			0: Su	22900
			oun			alid system call*1
		[28:1]				rved bits. Always set to 0
			omplete			rdware function call not completed
			ompiere			rdware function call completed
		[31:30	1			rved bits. Always set to 0
		R1 [31:0]	'I			rved bits. Always set to 0
					17626	iven bilo. Alwayo sel 10 0
L						



	1361	[Current description] 28.3.1.4 (2) (c)						
				NC_MACDMA_RX_Disa	able			
			ent registe					
		R4[0]		Forced reset	0	: This function is disabled while reception is		
						in progress.		
					1	: If the reception DMAC is enabled, it is disabled		
						even if reception is in progress (the reception		
						DMAC is forcibly reset).		
						Nothing is done if the reception DMAC is already		
			_			disabled.		
		R4[31		Unused				
		R5[31		Unused				
		R6[31		Unused				
		R7[6:0		Reserved	A	lways 0		
		R7[31	:8]	Unused				
		_						
			value regi					
		R0[0]		Result when R4[0] =	= 0	00b: Success		
						01b: Invalid system call (the buffer is in use		
						or reception is suspended)		
						10b: The function cannot be disabled since		
						reception is in progress.		
						11b: The function has already been		
				Popult when D 4101	. 1	disabled. 00b: Success		
				Result when R4[0] =	- 1	00b: Success 01b: Invalid system call (the buffer is in use		
						or reception is suspended)		
		R0[28	·11	Unused		All 0		
		R0[20		Complete		0: Hardware function call not completed		
		K0[29	J	Complete		1: Hardware function call completed		
		R0[31	.201	Unused				
			.301			All O		
		R1[31 [Correc 28.3.1.4	:0] t descripti 4 (2) (c)	Unused on]		All 0 All 0		
		R1[31 [Correc 28.3.1.4 Table 2	:0] t descripti 4 (2) (c)	Unused on] NC_MACDMA_RX_Disa rs	0: This in pr	All 0		
		R1[31 [Correc 28.3.1.4 Table 20 Argume	:0] t descripti 4 (2) (c) 8.11 HWFf ent registe	Unused on] NC_MACDMA_RX_Disa rs	0: This in pr 1: If th ever DM/	All 0		
		R1[31 [Correc 28.3.1.4 Table 20 Argume	:0] t descripti 4 (2) (c) 8.11 HWFt ent registe [0] Force	Unused on] NC_MACDMA_RX_Disa rs	0: This in pr 1: If th ever DMA Noth	All 0 a function is disabled while reception is ogress. e reception DMAC is enabled, it is disabled n if reception is in progress (the reception AC is forcibly reset).		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4	:0] t descripti 4 (2) (c) 8.11 HWFt ent registe [0] Force [0] Force [31:1]	Unused on] NC_MACDMA_RX_Disa rs	0: This in pr 1: If th ever DM/ Noth disa	All 0 a function is disabled while reception is rogress. e reception DMAC is enabled, it is disabled h if reception is in progress (the reception AC is forcibly reset). hing is done if the reception DMAC is already bled.		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4	:0] t descripti 4 (2) (c) 8.11 HWFt ent registe [0] Force [0] Force [31:1] [31:0]	Unused on] NC_MACDMA_RX_Disa rs	0: This in pr 1: If th ever DM/ Noth disa	All 0 a function is disabled while reception is rogress. e reception DMAC is enabled, it is disabled n if reception is in progress (the reception AC is forcibly reset). ning is done if the reception DMAC is already bled. ed in this Function call. Settings are ignored.		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R5	:0] t descripti 4 (2) (c) 8.11 HWFt ent registe [0] Force [0] Force [31:1] [31:0] [31:0]	Unused on] NC_MACDMA_RX_Disa rs	0: This in pr 1: If th ever DM/ Noth disa Not us Not us	All 0 a function is disabled while reception is rogress. e reception DMAC is enabled, it is disabled n if reception is in progress (the reception AC is forcibly reset). ning is done if the reception DMAC is already bled. ed in this Function call. Settings are ignored. ed in this Function call. Settings are ignored.		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4	:0] t descripti 4 (2) (c) 8.11 HWFt ent registe [0] Force [0] Force [31:1] [31:0]	Unused on] NC_MACDMA_RX_Disa rs	0: This in pr 1: If th ever DM/ Noth disa Not us Not us	All 0 a function is disabled while reception is rogress. e reception DMAC is enabled, it is disabled n if reception is in progress (the reception AC is forcibly reset). ning is done if the reception DMAC is already bled. ed in this Function call. Settings are ignored.		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R6 R5 R6 R7	:0] t descripti 4 (2) (c) 8.11 HWF1 ent registe [0] Force [0] Force [31:1] [31:0] [31:0] [31:0]	Unused on] NC_ MACDMA_RX_Disa rs ed reset	0: This in pr 1: If th ever DM/ Noth disa Not us Not us	All 0 a function is disabled while reception is rogress. e reception DMAC is enabled, it is disabled n if reception is in progress (the reception AC is forcibly reset). ning is done if the reception DMAC is already bled. ed in this Function call. Settings are ignored. ed in this Function call. Settings are ignored.		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R6 R7 Return	:0] t descripti 4 (2) (c) 8.11 HWFI ent registe [0] Force [0] Force [31:1] [31:0] [31:0] [31:0] value regi	Unused on] NC_ MACDMA_RX_Disa rs ed reset	0: This in pr 1: If th ever DM/ Not disa Not us Not us	All 0 a function is disabled while reception is rogress. e reception DMAC is enabled, it is disabled n if reception is in progress (the reception AC is forcibly reset). ning is done if the reception DMAC is already bled. ed in this Function call. Settings are ignored. ed in this Function call. Settings are ignored. sed in this Function call. Settings are ignored.		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R6 R5 R6 R7	:0] t descripti 4 (2) (c) 8.11 HWFI ent registe [0] Force [0] Force [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [31:0]	Unused on] NC_ MACDMA_RX_Disa rs ed reset	0: This in pr 1: If th ever DM/ Not disa Not us Not us	All 0 All 1 Biographic states of the second of the secon		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R6 R7 Return	:0] t descripti 4 (2) (c) 8.11 HWFI ent registe [0] Force [0] Force [31:1] [31:0] [31:0] [31:0] value regi	Unused on] NC_ MACDMA_RX_Disa rs ed reset	0: This in pr 1: If th ever DM/ Not disa Not us Not us	All 0 All 1 All 0 All 1 All 0 All 1 All 0 All 1 All 0 All 1 All 1 All 0 All 1 All 1 All 1 All 0 All 1 All 1 All 0 All 0 All 1 All 0 All 0 All 1 All 0 All 0 All 1 All 0 All 0 All 0 All 0 All 0 All 0 All 0 All 0 All 1 All 0 All 0		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R6 R7 Return	:0] t descripti 4 (2) (c) 8.11 HWFI ent registe [0] Force [0] Force [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [31:0]	Unused on] NC_ MACDMA_RX_Disa rs ed reset	0: This in pr 1: If th ever DM/ Not disa Not us Not us	All 0 All 1 All 1 All 0 All 1 All 1 All 1 All 0 All 1 All 1		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R6 R7 Return	:0] t descripti 4 (2) (c) 8.11 HWFI ent registe [0] Force [0] Force [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [31:0]	Unused on] NC_ MACDMA_RX_Disa rs ed reset	0: This in pr 1: If th ever DM/ Not disa Not us Not us	All 0 All 1 All 0 All 1 All 0 All 1 All 0 All 1 All 0 All 1 All 1		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R6 R7 Return	:0] t descripti 4 (2) (c) 8.11 HWFI ent registe [0] Force [0] Force [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [31:0]	Unused on] NC_ MACDMA_RX_Disa rs ed reset	0: This in pr 1: If th ever DM/ Not disa Not us Not us	All 0 All 10 All 10		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R6 R7 Return	:0] t descripti 4 (2) (c) 8.11 HWFI ent registe [0] Force [0] Force [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [31:0]	Unused on] NC_ MACDMA_RX_Disa rs ed reset	0: This in pr 1: If th ever DM/ Not disa Not us Not us	All 0 All 10 All 10 A		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R6 R7 Return	:0] t descripti 4 (2) (c) 8.11 HWFI ent registe [0] Force [0] Force [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [31:0]	Unused on] NC_MACDMA_RX_Disa rs ed reset sters Result when R4[0	0: This in pr 1: If th ever DM/ Notf disa Not us Not us Not us	All 0 All 10 All 10		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R6 R7 Return	:0] t descripti 4 (2) (c) 8.11 HWFI ent registe [0] Force [0] Force [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [31:0]	Unused on] NC_ MACDMA_RX_Disa rs ed reset	0: This in pr 1: If th ever DM/ Notf disa Not us Not us Not us	All 0 a function is disabled while reception is ogress. e reception DMAC is enabled, it is disabled in freception is in progress (the reception AC is forcibly reset). ning is done if the reception DMAC is already bled. ed in this Function call. Settings are ignored. in this Function call. Settings are ignored. ed in this Function call. Settings are ignored. in this Function call the buffer is in use or reception is suspended) 10b: The function cannot be disabled since reception is in progress. 11b: The function has already been disabled. 00b: Success		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R6 R7 Return	:0] t descripti 4 (2) (c) 8.11 HWFI ent registe [0] Force [0] Force [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [31:0]	Unused on] NC_MACDMA_RX_Disa rs ed reset sters Result when R4[0	0: This in pr 1: If th ever DM/ Notf disa Not us Not us Not us	All 0 All 0		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R6 R7 Return	:0] t descripti 4 (2) (c) 8.11 HWFP ent registe [0] Force [0] Force [31:1] [31:0] [31:0] [31:0] [31:0] Value regi [1:0] Result	Unused on] NC_MACDMA_RX_Disa rs ed reset sters Result when R4[0	0: This in pr 1: If th ever DM/ Notf disa Not us Not us Not us	All 0 a function is disabled while reception is ogress. e reception DMAC is enabled, it is disabled in if reception is in progress (the reception AC is forcibly reset). ning is done if the reception DMAC is already bled. ed in this Function call. Settings are ignored. oub: Success 01b: Invalid system call (the buffer is in use or reception is suspended) 10b: The function cannot be disabled since reception is in progress. 11b: The function has already been disabled. 00b: Success 01b: Invalid system call (the buffer is in use or reception is suspended) 10b: The function has already been disabled. 00b: Success 01b: Invalid system call (the buffer is in use or reception is suspended)		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R6 R7 Return	:0] t descripti 4 (2) (c) 8.11 HWFP ent registe [0] Force [0] Force [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] Value regi [1:0] Result [28:2]	Unused on] NC_ MACDMA_RX_Disa rs ed reset sters Result when R4[0 Result when R4[0	0: This in pr 1: If th ever DM/ Notf disa Not us Not us Not us	All 0 a function is disabled while reception is ogress. e reception DMAC is enabled, it is disabled if reception is in progress (the reception AC is forcibly reset). ning is done if the reception DMAC is already bled. ed in this Function call. Settings are ignored. oub: Success 01b: Invalid system call (the buffer is in use or reception is suspended) 10b: The function cannot be disabled since reception is in progress. 11b: The function has already been disabled. 00b: Success 01b: Invalid system call (the buffer is in use or reception is suspended) Reserved bits. Always set to 0		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R6 R7 Return	:0] t descripti 4 (2) (c) 8.11 HWFP ent registe [0] Force [0] Force [31:1] [31:0] [31:0] [31:0] [31:0] Value regi [1:0] Result	Unused on] NC_ MACDMA_RX_Disa rs ed reset sters Result when R4[0 Result when R4[0	0: This in pr 1: If th ever DM/ Notf disa Not us Not us Not us	All 0 a function is disabled while reception is ogress. e reception DMAC is enabled, it is disabled if reception is in progress (the reception AC is forcibly reset). ning is done if the reception DMAC is already bled. ed in this Function call. Settings are ignored. oub: Success 01b: Invalid system call (the buffer is in use or reception is suspended) 10b: The function cannot be disabled since reception is in progress. 11b: The function has already been disabled. 00b: Success 01b: Invalid system call (the buffer is in use or reception is suspended) Reserved bits. Always set to 0 0: Hardware function call not completed		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R6 R7 Return	:0] t descripti 4 (2) (c) 8.11 HWFI ent registe [0] Force [0] Force [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] [28:2] [29] Cor	Unused on] NC_ MACDMA_RX_Disa rs ed reset sters Result when R4[0 Result when R4[0	0: This in pr 1: If th ever DM/ Notf disa Not us Not us Not us	All 0 a function is disabled while reception is ogress. e reception DMAC is enabled, it is disabled if reception is in progress (the reception AC is forcibly reset). ning is done if the reception DMAC is already bled. ed in this Function call. Settings are ignored. oub: Success 01b: Invalid system call (the buffer is in use or reception is suspended) 10b: The function cannot be disabled since reception is in progress. 11b: The function has already been disabled. 00b: Success 01b: Invalid system call (the buffer is in use or reception is suspended) Reserved bits. Always set to 0 0: Hardware function call not completed 1: Hardware function call completed		
		R1[31 [Correc 28.3.1.4 Table 2 Argume R4 R4 R5 R6 R7 Return	:0] t descripti 4 (2) (c) 8.11 HWFP ent registe [0] Force [0] Force [31:0] [31:0] [31:0] [31:0] [31:0] [31:0] Value regi [1:0] Result [28:2]	Unused on] NC_ MACDMA_RX_Disa rs ed reset sters Result when R4[0 Result when R4[0	0: This in pr 1: If th ever DM/ Notf disa Not us Not us Not us	All 0 a function is disabled while reception is ogress. e reception DMAC is enabled, it is disabled if reception is in progress (the reception AC is forcibly reset). ning is done if the reception DMAC is already bled. ed in this Function call. Settings are ignored. oub: Success 01b: Invalid system call (the buffer is in use or reception is suspended) 10b: The function cannot be disabled since reception is in progress. 11b: The function has already been disabled. 00b: Success 01b: Invalid system call (the buffer is in use or reception is suspended) Reserved bits. Always set to 0 0: Hardware function call not completed		



9	1362	[Current description]							
		28.3.1.4 (2) (c)							
		Table 28.12 HWFNC_MACDMA_RX_Control							
			Argument registers						
		R4[8:0]	Interrupt source	Controls enabling or disabling of the interrupt					
				source corresponding to each bit.					
				0: Interrupts disabled					
		D 4[04:0]	L la cara d	1: Interrupts enabled (initial value)					
		R4[31:9]	Unused						
		R5[31:0]	Unused						
		R6[31:0]	Unused						
		R7[31:0]	Unused						
		Return value r	egisters						
		R0[0]	Result	0: Success					
				1: Invalid system call					
		R0[28:1]	Unused	All 0					
		R0[29]	Complete	0: Hardware function call not completed					
				1: Hardware function call completed					
		R0[31:30]	Unused	All 0					
		R1[31:0] Unused All 0							
		[Correct descr 28.3.1.4 (2) (c Table 28.12 HV Argument regi) VFNC_MACDMA_RX_C	ontrol					
			Interrupt source	Controls enabling or disabling of the interrupt					
				source corresponding to each bit.					
				0: Interrupts disabled					
				1: Interrupts enabled (initial value)					
		[31:9		Not used in this Function call. Settings are ignored.					
		R5 [31:0		Not used in this Function call. Settings are ignored.					
		R6 [31:0		Not used in this Function call. Settings are ignored.					
		R7 [31:0]	Not used in this Function call. Settings are ignored.					
		Return value r	eaisters						
		R0 [0] R		0: Success					
				1: Invalid system call					
		[28:1]	Reserved bits. Always set to 0					
		[29] (Complete	0: Hardware function call not completed					
			·	1: Hardware function call completed					
		[31:3		Reserved bits. Always set to 0					
				Reserved bits. Always set to 0					
		R1 [31:0		Reserved bits. Always set to 0					



10	1362	[Current des	cription]					
		28.3.1.4 (2) (c)						
		Table 28.13 HWFNC_MACDMA_RX_Errstat						
		Argument re	gisters					
		R4[31:0]	Unused					
		R5[31:0]	Unused					
		R6[31:0]	Unused					
		R7[31:0]	Unused					
		Return value						
		R0[3:0]	Result	[0]: Buffer Get fails				
				[1]: Always 0				
				[2]: Rx data size over 4096 words (16 KB)				
				[3]: HWFNC_MACDMA_Rx_Disable is				
				issued when forced reset is enabled.				
		R0[28:4]	Unused	All 0				
		R0[29]	Complete	0: Hardware function call not completed				
				1: Hardware function call completed				
		R0[31:30]	Unused	All O				
		R1[31:0]	Unused	All O				
			1					
			(c) HWFNC_MACDMA_RX_Err	stat				
		Argument re		Net used in this Equation call. Cattings are imported				
		R4 [31		Not used in this Function call. Settings are ignored.				
		R5 [31		Not used in this Function call. Settings are ignored.				
		R6 [31		Not used in this Function call. Settings are ignored.				
		R7 [31	:0]	Not used in this Function call. Settings are ignored.				
		Return value						
		R0 [3:0	0] Result	[0]: Buffer Get fails				
				[1]: Always 0				
				[2]: Rx data size over 4096 words (16 KB)				
				[3]: HWFNC_MACDMA_Rx_Disable is				
				issued when forced reset is enabled.				
		[28		Reserved bits. Always set to 0				
		[29] Complete	0: Hardware function call not completed				
				1: Hardware function call completed				
		[31	:30]	Reserved bits. Always set to 0				
		R1 [31	:0]	Reserved bits. Always set to 0				



11	1365	[Current descrip	tion]						
		28.3.1.4 (3) (d)							
		Table 28.14 HWFNC_MACDMA_TX_Start							
		Argument regist	gument registers						
		R4[31:0]	Address of the descriptor	Address of the transmission descriptor					
		R5[31:0]	Unused						
		R6[31:0]	Unused						
		R7[6:0]	Reserved	Always 0					
		R7[31:7]	Unused						
			• .						
		Return value req							
		R0[1:0]	Result	0: Success					
		D0[00.0]	Linus e d	1: Invalid system call					
		R0[28:2]	Unused	All O					
		R0[29]	Complete	0: Hardware function call not completed					
		D0[04:00]	Linus ed	1: Hardware function call completed All 0					
		R0[31:30]	Unused						
		R1[31:0]	Unused	All U					
		[Correct descrip	tion						
		28.3.1.4 (3) (d)	lionj						
			FNC_MACDMA_ TX_Start						
		Argument regist							
			Address of the descriptor	Address of the transmission descriptor					
		R5 [31:0]		Not used in this Function call. Settings are ignored.					
		R6 [31:0]		Not used in this Function call. Settings are ignored.					
		R7 [6:0]		Reserved bits. Always set to 0					
		[31:7]		Not used in this Function call. Settings are ignored.					
		Return value ree		·					
		R0 [1: 0] R	esult	0: Success					
				1: Invalid system call					
		[28: 1]		Reserved bits. Always set to 0					
		[29] Co	omplete	0: Hardware function call not completed					
				1: Hardware function call completed					
		[31:30]		Reserved bits. Always set to 0					
		R1 [31:0]		Reserved bits. Always set to 0					



12	1365	[Current descri	ption]					
		28.3.1.4 (3) (d)						
		Table 28.15 HWFNC_MACDMA_TX_Errstat						
		Argument registers						
		R4[31:0]	Unused					
		R5[31:0]	Unused					
		R6[31:0]	Unused					
		R7[31:0]	Unused					
		· · · ·						
		Return value re	egisters					
		R0[1:0]	Result	[0]: Memory Access Violation				
				[1]: Memory Access Timeout				
		R0[28:2]	Unused	All O				
		R0[29]	Complete	0: Hardware function call not completed				
				1: Hardware function call completed				
		R0[31:30]	Unused	All O				
		R1[31:0]	Unused	All O				
		[Correct descri						
		28.3.1.4 (3) (d)						
			/FNC_MACDMA_TX_Er	rstat				
		Argument regis	sters					
		R4 [31:0]		Not used in this Function call. Settings are ignored.				
		R5 [31:0]		Not used in this Function call. Settings are ignored.				
		R6 [31:0]		Not used in this Function call. Settings are ignored.				
		R7 [31:0]		Not used in this Function call. Settings are ignored.				
		Deturner						
		Return value re						
		R0 [1:0] F	Kesult	[0]: Memory Access Violation				
		[00:0]		[1]: Memory Access Timeout				
		[28:2]		Reserved bits. Always set to 0				
			omplete	0: Hardware function call not completed				
		104-00	N1	1: Hardware function call completed				
		[31:30	ון	Reserved bits. Always set to 0				
		R1 [31:0]		Reserved bits. Always set to 0				

Г

		5 (2) (c)			
		8.16 HW	FNC_Direct_Memory_Transfer		
	Name Function		HWFNC_Direct_Memory_Transfer		uffer RAM or from the buffer RAM to the data
	Function	F	RAM.		RAM to the buffer RAM. For transfer from the
		k		HWFN	C_INT_BUF (however, data transfer from the data
		ent regist	ters		-
	R4[31		Address where the source for transfer starts		Specifies the address where the source area for transfer starts.
	R5[31	:0]	Address where the destination area for transfer starts	nation	Specifies the address where the destination area for transfer starts.
	R6[31 R7[31		Number of bytes for transfe Unused	er	Specifies the number of bytes for transfer.
					I
	Return R0[1:0	value reg	gisters Result	00h.	Success
		0]		01b:	Invalid system call (transfer from the buffer RAM to the buffer RAM has been specified)
	R0[28	·21	Unused	All 0	An exception has occurred
	R0[20		Complete	-	ardware function call not completed
				1: Ha	ardware function call completed
	R0[31		Unused	All 0	
	R1[31	:0]	Address where the exception occurred		n an exception has occurred, this is the ess where it occurred. In other cases, all 0s.
	28.3.1.	t descrip 5 (2) (c) 8.16 HW	FNC_Direct_Memory_Transfer		
	28.3.1.	5 (2) (c) 8.16 HW on	FNC_Direct_Memory_Transfer HWFNC_Direct_Memory_Transfer Transfers data from the data RAM RAM. Data cannot be transferred from buffer RAM to the buffer RAM,	to the b the but use HW	uffer RAM or from the buffer RAM to the data ffer RAM to the buffer RAM. For transfer from the /FNC_INT_BUF (however, data transfer from the
	28.3.1.3 Table 2 Name Function	5 (2) (c) 8.16 HW 1 on	FNC_Direct_Memory_Transfer HWFNC_Direct_Memory_Transfer Transfers data from the data RAM RAM. Data cannot be transferred from buffer RAM to the buffer RAM, data RAM to the data RAM is por	to the b the but use HW	ffer RAM to the buffer RAM. For transfer from the /FNC_INT_BUF (however, data transfer from the
	28.3.1.3 Table 2 Name Function	5 (2) (c) 8.16 HW 10 00 1 1 1 1 1 1 1 1 1 1 1 1 1	FNC_Direct_Memory_Transfer HWFNC_Direct_Memory_Transfer Transfers data from the data RAM RAM. Data cannot be transferred from buffer RAM to the buffer RAM, data RAM to the data RAM is por	to the b the but use HM ssible).	ffer RAM to the buffer RAM. For transfer from the /FNC_INT_BUF (however, data transfer from the
	28.3.1. Table 2 Name Function	5 (2) (c) 8.16 HW 10 10 10 10 10 10 10 10 10 10	FNC_Direct_Memory_Transfer HWFNC_Direct_Memory_Transfer Transfers data from the data RAM RAM. Data cannot be transferred from buffer RAM to the buffer RAM, data RAM to the data RAM is por ters Address where the source are transfer starts Address where the destination for transfer starts	to the but the but use HM ssible). a for	fer RAM to the buffer RAM. For transfer from the /FNC_INT_BUF (however, data transfer from the Specifies the address where the source area for transfer starts. Specifies the address where the destination area for transfer starts.
	28.3.1.1 Table 2 Name Function Argume R4 R5 R6	5 (2) (c) 8.16 HW 10 10 10 10 10 10 10 10 10 10	FNC_Direct_Memory_Transfer HWFNC_Direct_Memory_Transfer Transfers data from the data RAM RAM. Data cannot be transferred from buffer RAM to the buffer RAM, data RAM to the data RAM is por ters Address where the source are transfer starts Address where the destination	to the but the but use HM ssible). a for	fer RAM to the buffer RAM. For transfer from the /FNC_INT_BUF (however, data transfer from the Specifies the address where the source area for transfer starts. Specifies the address where the destination area for transfer starts. Specifies the number of bytes for transfer.
	28.3.1. Table 2 Name Function Argume R4 R5	5 (2) (c) 8.16 HW 10 10 10 10 10 10 10 10 10 10	FNC_Direct_Memory_Transfer HWFNC_Direct_Memory_Transfer Transfers data from the data RAM RAM. Data cannot be transferred from buffer RAM to the buffer RAM, data RAM to the data RAM is por ters Address where the source are transfer starts Address where the destination for transfer starts	to the but the but use HM ssible). a for	fer RAM to the buffer RAM. For transfer from the /FNC_INT_BUF (however, data transfer from the Specifies the address where the source area for transfer starts. Specifies the address where the destination area for transfer starts. Specifies the number of bytes for transfer.
	28.3.1.1 Table 2 Name Function R4 R5 R6 R7 Return	5 (2) (c) 8.16 HW 10 10 10 10 10 10 10 10 10 10	FNC_Direct_Memory_Transfer HWFNC_Direct_Memory_Transfer Transfers data from the data RAM RAM. Data cannot be transferred from buffer RAM to the buffer RAM, data RAM to the data RAM is por ters Address where the source are transfer starts Address where the destination for transfer starts Number of bytes for transfer gisters	to the but use HM ssible). a for area	fer RAM to the buffer RAM. For transfer from the /FNC_INT_BUF (however, data transfer from the for transfer starts. Specifies the address where the destination area for transfer starts. Specifies the number of bytes for transfer. Not used in this Function call. Settings are ignored.
	28.3.1. Table 2 Name Function R4 R5 R6 R7	5 (2) (c) 8.16 HW 10 10 10 10 10 10 10 10 10 10	FNC_Direct_Memory_Transfer HWFNC_Direct_Memory_Transfer Transfers data from the data RAM RAM. Data cannot be transferred from buffer RAM to the buffer RAM, data RAM to the data RAM is por ters Address where the source are transfer starts Address where the destination for transfer starts Number of bytes for transfer gisters	to the but the but use HM ssible). a for a for a rea 00b: 1 01b: 1 F	fer RAM to the buffer RAM. For transfer from the /FNC_INT_BUF (however, data transfer from the Specifies the address where the source area for transfer starts. Specifies the address where the destination area for transfer starts. Specifies the number of bytes for transfer. Not used in this Function call. Settings area
	28.3.1.1 Table 2 Name Function R4 R5 R6 R7 Return	5 (2) (c) 8.16 HW 100 110 110 110 110 110 128 128 128 128 128 128 128 128	FNC_Direct_Memory_Transfer HWFNC_Direct_Memory_Transfer Transfers data from the data RAM RAM. Data cannot be transferred from buffer RAM to the buffer RAM, data RAM to the data RAM is porter ters Address where the source are transfer starts Address where the destination for transfer starts Number of bytes for transfer gisters Result	to the but the but use HM ssible). a for a for a rea 00b: \$ 01b: I F 10b: / Rese	fer RAM to the buffer RAM. For transfer from the /FNC_INT_BUF (however, data transfer from the ////////////////////////////////////
	28.3.1.1 Table 2 Name Function R4 R5 R6 R7 Return	5 (2) (c) 8.16 HW 100 110 110 110 110 110 128 128 128 128 128 128 128 128	FNC_Direct_Memory_Transfer HWFNC_Direct_Memory_Transfer Transfers data from the data RAM RAM. Data cannot be transferred from buffer RAM to the buffer RAM, data RAM to the data RAM is por ters Address where the source are transfer starts Address where the destination for transfer starts Number of bytes for transfer gisters	to the but use HM ssible). a for a rea 00b: 3 01b: 1 F 10b: 7 Rese 0: Ha	fer RAM to the buffer RAM. For transfer from the /FNC_INT_BUF (however, data transfer from the ////////////////////////////////////
	28.3.1.1 Table 2 Name Function R4 R5 R6 R7 Return	5 (2) (c) 8.16 HW 100 110 110 110 110 110 128 128 128 128 128 128 128 128	FNC_Direct_Memory_Transfer HWFNC_Direct_Memory_Transfer Transfers data from the data RAM RAM. Data cannot be transferred from buffer RAM to the buffer RAM, data RAM to the data RAM is porter ters Address where the source are transfer starts Address where the destination for transfer starts Number of bytes for transfer gisters Result	to the but use HM ssible). a for a rea 01b: 1 F 10b: 7 Rese 0: Ha 1: Ha	fer RAM to the buffer RAM. For transfer from the /FNC_INT_BUF (however, data transfer from the ////////////////////////////////////



		28.3.1.5 (2) (c) Table 28.17 HWFNC_Direct_Memory_Replace						
		Name		WFNC_Direct_Memory_Replace				
		Function	on F	Replaces the specified memory	y area ir	the data RAM or buffer RAM with a defined data		
			p	attern. The number of words t	o be wri	tten must be at least four.		
		Argument registers						
		R4[31	:0]	Pattern		Specifies the data pattern for writing.		
		R5[31	:0]	Start address		Specifies the address where the destination		
		R6[31	·01	Number of words		area for writing starts. Specifies the number of words to be written.		
		R7[31		Unused		Specifies the number of words to be written.		
		Return	value reg					
		R0[1:0	J	Result	-	0b: Success 1b: Invalid system call		
					Ŭ	The set address was specified in byte		
						units or the setting for the number of		
						words to be transferred is three or fewer.		
		DOLOO		Unucod		0b: An exception has occurred.		
		R0[28 R0[29		Unused Complete		II 0 : Hardware function call not completed		
		1020	1	Complete		: Hardware function call completed		
		R0[31		Unused		II 0		
		R1[31	:0]	Address where		/hen an exception has occurred, this is the		
			the exception occurred			ddress where it occurred. In other cases, all 0s.		
		Name Functio	on F p	attern. The number of words t	y area ir	the data RAM or buffer RAM with a defined data tten must be at least four. (A words unit is 32 bits)		
		Argume R4	ent regist [31:0] I			Specifies the data pattern for writing.		
		R5		Start address		Specifies the address where the destination area for writing starts.		
		R6		Number of words		Specifies the number of words to be written.		
		R7	[31:0]			Not used in this Function call. Settings are ignored.		
		R0	[1:0] R	esult		 b: Success b: Invalid system call The set address was specified in byte units or the setting for the number of 		
					10	words to be transferred is three or fewer. b: An exception has occurred.		
			[28:2]		Re	eserved bits. Always set to 0		
			[29] Co	omplete		Hardware function call not completed Hardware function call completed		
			[31:30]		Re	eserved bits. Always set to 0		
		R1		Address where the exception occurred		hen an exception has occurred, this is the ldress where it occurred. In other cases, all 0s.		
					au			



15	1369	28.3.2 Table 28.18 Interrupt related Operations for Transmission	28.3.2 Table 28.18 Interrupt related Operations for Transmission
		Conditions for Asserting and De-asserting Interrupts of TX FIFO error interrupt	Conditions for Asserting and De-asserting Interrupts of TX FIFO error interrupt
		This interrupt is generated when information is further updated while the GMAC_TXID/GMAC_TXRESULT register is holding the maximum number of items of information (four). Take care, since the oldest of the retained information will have been overwritten when this error occurs. Reading the GMAC_TXID/GMAC_TXRESULT register leads to clearing of the retained information and restoring normal operation.	This interrupt is generated when information is further updated while the GMAC_TXID/GMAC_TXRESULT register is holding the maximum number of items of information (four). Take care, since the oldest of the retained information will have been overwritten when this error occurs. Reading the GMAC_TXID/GMAC_TXRESULT register repeatedly until the value of the GMAC_TXFIFO.TRBFR bit becomes 0 leads to clearing of the retained information and restoring normal operation.
16	1373	28.3.3.2 (1) Tx frame control information	28.3.3.2 (1) Tx frame control information
	_	Item Explanation	Item Explanation
		TX_WORD[12:0] Specifies the number of words in the Ethernet frame to be transmitted. The number of valid bytes in the last word is specified by using TX_EOB[1:0].	TX_WORD[12:0] Specifies the number of words in the Ethernet frame to be transmitted (A word unit is 32 bits). The number of valid bytes in the last word is specified by using TV FORMER:
		TCPIP ACC OFF 1: Disables the TCPIP accelerator. 0: Enables the TCPIP accelerator.	TX_EOB[1:0]. TCPIP ACC OFF ^{*2} 1: Disables the TCPIP accelerator.
		APAD Padding is inserted because the	0: Enables the TCPIP accelerator.
		frame length is less than 64 octets.	APAD Padding is automatically inserted if the frame length is less than 64 octets.
			Note2: Disable the TCPIP accelerator if the following
			frames are sent;
			 IPv6 frames without UDP or TCP packet iEEE802.3 + IEEE802.2 (LLC) frames
17	1374	28.3.3.2 (2) (a) Figure 28.16 Format for Transmission Data (TCPIP Accelerator Enabled, VLAN Tag included)	28.3.3.2 (2) (a) Figure 28.16 Format for Transmission Data (TCPIP Accelerator Enabled, VLAN Tag included)
		Destination MAC address(6bytes)	Destination MAC address(6bytes)
		Source MAC address(6bytes)	Source MAC address(6bytes)
		Padding(2bytes) VLAN tag(2bytes)	Padding(2bytes) VLAN tag(2bytes)
		Type/Length(2bytes) VLAN tag(2bytes)	Type/Length(2bytes) VLAN Info(2bytes)
		Frame payload(Max. 1500bytes)	Frame payload(Max. 1500bytes)
18	1376	 28.3.3.3 Creating transmit descriptors Note that this function is subject to the following restrictions: If Linked Long Buffer is specified as a descriptor with Release Bit = 1 Only the buffer that includes the address specified by the descriptor is released. The buffer linked with the released buffer is not released. 	 28.3.3.3 Creating transmit descriptors Note that this function is subject to the following restrictions: If Linked Long Buffer is specified as a descriptor with Release Bit = 1 Only the buffer that includes the address specified by the descriptor is released. The buffer linked with the released buffer is not released.
19	1379	28.3.4.6 Format of receive data If a frame is received by using Ethernet MAC, 64-bit receive frame information is suffixed to the frame data. The Ethernet frame size, error status, and other information can be obtained from the receive frame information. Receive frame information begins at a 64-bit boundary. Therefore, the size of padding at the end of Ethernet frames changes according to the frame size.	28.3.4.6 Format of receive data If a frame is received by using Ethernet MAC, 64-bit receive frame information is suffixed to the frame data. The Ethernet frame size, error status, and other information can be obtained from the receive frame information. Receive frame information begins at a 64-bit boundary. Therefore, the size of next padding at the end of Ethernet frames changes according to the frame size.



20	1380,		ception frame information		Reception frame information
	1381	item	Explanation	item	Explanation
		IPNG	If this field is set to '1', it indicates that the checksum of the IPv4 header	IPNG Note	If this field is set to '1', it indicates that the checksum of the IPv4 header conflict
			conflicts with the calculation result of		with the calculation result of the TCPI
			the TCPIP accelerator.		accelerator.
		TCPNG	If this field is set to '1', it indicates that	TCPNG	If this field is set to '1', it indicates that th
			the checksum of the TCP or UDP	Note	checksum of the TCP or UDP heade
			header conflicts with the calculation		conflicts with the calculation result of th
		IPV6NG	result of the TCPIP accelerator. If this field is set to '1', it indicates that	IPV6NG	TCPIP accelerator. If this field is set to '1', it indicates that the
		IF VOING	the IPv6 extended header is one from	Note	IPv6 extended header is one from amon
			among routing, Hopby-Hop, or		routing, Hopby-Hop, or Destination Op
			Destination Opt, and that the value of		and that the value of the header lengt
			the header length field is incorrect.		field is incorrect.
		OUT_OF_LI ST	If this field is set to '1', it indicates that a protocol number not listed below was	OUT_OF_ LIST Note	If this field is set to '1', it indicates that protocol number not listed below wa
		51	detected in the IPv6 extended header.	LIST	detected in the IPv6 extended header.
			06h: TCP header		06h: TCP header
			11h: UDP header		11h: UDP header
			00h: Hop-by-Hop		00h: Hop-by-Hop 3Ch: Destination Opt
			3Ch: Destination Opt 2Ch: Fragment		2Ch: Fragment
			2Bh: Routing		2Bh: Routing
			3Bh: No next header		3Bh: No next header
			32h: ESP header		32h: ESP header
		T)(DEID	33h: AH header		33h: AH header
		TYPEIP	If this field is set to '1', it indicates that an IP packet was received. If this field is set to '1', it indicates that	TYPEIP Note	If this field is set to '1', it indicates that a IP packet was received.
		MAACL	an 802.3 (LLC/SNAP) packet was received.	MAACL Note	If this field is set to '1', it indicates that a 802.3 (LLC/SNAP) packet was received.
		PPPOE	If this field is set to '1', it indicates that a PPPoE packet was received.	PPPOE Note	If this field is set to '1', it indicates that PPPoE packet was received.
		VTAG	If this field is set to '1', it indicates that the packet included a VLAN tag.	VTAG ^{Note}	If this field is set to '1', it indicates that the packet included a VLAN tag.
					e fields are invalid if TCPIP r is disabled.
21	1386	28.3.5.1 Transr	mission with Use of the TCPIP Accelerator	28.3.5.1 Tran	smission with Use of the TCPIP Accelerato
			esult of calculating the UDP checksum of transmission is 0000h, write FFFFh to n field.	checksum	the result of calculating the UD of a packet for transmission is 0000 n to the checksum field.
				IPv4 does length, the	ne value of the header length field on not match with that of actual header transmission may never end.
22	1387	When TCPIP	ntion with Use of the TCPIP Accelerator PACC is enabled, two bytes of padding P accelerator are inserted in the MAC	28.3.5.2 Rec When TCP	eption with Use of the TCPIP Accelerator IPACC is enabled, two bytes of paddir PIP accelerator are inserted in the MA
		headers of re	ceived frames.	headers of	received frames. reception TCPIP accelerator is enable
			ed packet includes TCP/UDP, the FCS		ved packet includes TCP/UDP, the FC
		field is ove	rwritten by the checksum value of	field is ov	erwritten by the checksum value
			his checksum value can be used for		This checksum value can be used for
			ne total checksum value of fragmented		the total checksum value of fragmente
		TCP/UDP page	ckets.	TCP/UDP p	
					the checksum of Pseudo Heade
					e calculated by software because th field is not contained in Pseud
					fragment packets.
23	1387		ption with Use of the TCPIP Accelerator		eption with Use of the TCPIP Accelerator
			hecksum field of the UDP header of the		checksum field of the UDP header
			cket is 0000h, checksum comparison		1 ,
		does not proc	ceea.		does not proceed. TCPNG bit is set t
				0.	
				1	



24	1389	[Current description] No description.
		[Correct description] Add the description in below.
		28.4.4 Erroneous Judgment of Checksum Validation at Reception
		(1) Target: Ethernet I frame and IEEE802.3 + IEEE802.2 (LLC+SNAP) frame
		When a frame is received under below conditions listed, IPNG field or TCPNG field of the Reception Frame Information may become "1" even the packet is valid. If these conditions are met, checksum value must be checked by software.
		 Value of the checksum field in IPv4, TCP header is 0x0000 or 0xFFFF A frame length that excluded IPv6, FCS is over 60 bytes. Payload of TCP or UDP is 1 byte and the data followed are not 0
		• The Value of the checksum of Pseudo header used for calculating the checksum of IPv6, TCP or UDP is over 21 bits
		(2) Target: IEEE802.3 + IEEE802.2 (LLC) frame
		If IEEE802.3 + IEEE802.2 (LLC) frame that does not have SNAP is received, TYPEIP field and IPNG field may become "1". In this case, Check the presence of SNAP by software and if SNAP is not present, handle that frame as valid.



٧o.	Page	Current description	Correct description					
1	1519	30.8.1 AL Control Register (AL_CONTROL)	30.8.1 AL Control Register (AL_CONTROL)					
		Description of b5	Description of b5					
		Value after reset: x	Value after reset: 0					
		Symbol:-	Symbol: DEVICEID					
		Bit Name: Reserved	Bit Name: Device ID Request					
		Description : When read, the value returned is	Description : Device ID Request					
		undefined. PDI:R(Clear)	0: No request 1: Device ID request					
			PDI:R(Clear)					
		ECAT:R/(W)	ECAT:R/(W)					
2	1520	30.8.2 AL Status Register (AL_STATUS)	30.8.2 AL Status Register (AL_STATUS)					
2	1520	Description of b5	Description of b5					
		Value after reset: x	Value after reset: 0					
		Symbol:—	Symbol: DEVICEID					
		Bit Name: Reserved	Bit Name: Device ID Status					
		Description : When read, the value returned is	Description : Device ID Status					
		undefined.	0: Device ID not valid					
			1: Device ID loaded					
3	1525	30.9.3 PDI Configuration Register (PDI_CONFIG)	30.9.3 PDI Configuration Register (PDI_CONFIG					
		Description of b7 to b5	Description of b7 to b5					
		Value after reset: 010	Value after report. 010					
		Value after reset: 010 Symbol:ONCHIPBUS	Value after reset: 010 Symbol:ONCHIPBUS					
		Bit Name: On-Chip Bus Type Indication	Bit Name: On-Chip Bus Type Indication					
		Description: Indicate the type of on-chip bus. In this	Description: Indicate the type of on-chip bus.					
		chip, the value is always 100.	this chip, the value is always 010 .					
4	1544	30.14.7 PHY Port Status n Register (PHY_STATUSn)	30.14.7 PHY Port Status n Register (PHY_STATUS)					
•	1011							
5	1580	[Current description] No description.						
		[Correct description] Add the description in below.						
		30.20 Configuration of Reset Circuit						
		The configuration of Reset Circuit of ESC is shown ECAT or Reset Request (0041h) by PDI have been	received, ESC will stop and RESET pin output					
		from ESC becomes "1". The RESET pin output from low, then it will reset the Ethernet PHY that con- generated.						
		low, then it will reset the Ethernet PHY that co	onnected outside. And ETHCRSTI interrupt ary to switch the CATRST bit in the ETHSFTRS me the ESC reset input goes from "1" to "0", th ESC reset input goes from "0" to "1", the ES will be started. The loading of EEPROM will b g of cancelling the reset of the Ethernet PHY, s					
		low, then it will reset the Ethernet PHY that con- generated. After ETHCRSTI interrupt is detected, it is necessar register from "1" to "0" to "1". To be noted, at the ti ESC reset output will be "0". At the time when the starts restarting and the loading of the EEPROM completed in about 1 ms. Be sure to set the timing that the restart of the Ethernet PHY will be after the	onnected outside. And ETHCRSTI interrupt ary to switch the CATRST bit in the ETHSFTRS me the ESC reset input goes from "1" to "0", the ESC reset input goes from "0" to "1", the ES will be started. The loading of EEPROM will be of cancelling the reset of the Ethernet PHY, s e start of ESC is completed. The timing chart RST bit in the ETHSFTRST register, not by the ase, since the PHYRESETOUT# pin does no reset state beforehand by the PHYRST bit in the					
		 low, then it will reset the Ethernet PHY that congenerated. After ETHCRSTI interrupt is detected, it is necessare gister from "1" to "0" to "1". To be noted, at the till ESC reset output will be "0". At the time when the starts restarting and the loading of the EEPROM completed in about 1 ms. Be sure to set the timing that the restart of the Ethernet PHY will be after the shown in Figure 30.3. It is also possible to reset the ESC with the CAT ECAT/PDI reset request (0040h/0041h). In this cautomatically go low, set the Ethernet PHY to the proceeding that the the treatment of the Ethernet PHY to the proceeding the the thermatically go low. 	onnected outside. And ETHCRSTI interrupt ary to switch the CATRST bit in the ETHSFTRS me the ESC reset input goes from "1" to "0", the ESC reset input goes from "0" to "1", the ES will be started. The loading of EEPROM will be of cancelling the reset of the Ethernet PHY, s e start of ESC is completed. The timing chart RST bit in the ETHSFTRST register, not by the ase, since the PHYRESETOUT# pin does not reset state beforehand by the PHYRST bit in the					

