

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU	Document No.	TN-RZ*-A052A/E	Rev.	1.00
Title	RZ/T1 Group User's Manual: Hardware Collection for ATCM Wait Control Register		Information Category	Technical Notification	
Applicable Product	RZ/T1 Group	Lot No.	Reference Document	RZ/T1 Group User's Manual: Hardware Rev1.40 R01UH0483EJ0140 Rev.1.40	
		All lots			

Incorrect description regarding ATCM Wait Control Register (SYTATCMWAIT) have been found.

This document describes corrections for the incorrect description.

1.Detail of a correction

Page	Description															
105	<p>[Current description]</p> <p>2.4.1 ATCM Wait Control Register (SYTATCMWAIT)</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Symbol</th> <th>Bit Name</th> <th>Description</th> <th>R/W</th> </tr> </thead> <tbody> <tr> <td>b1, b0</td> <td>ATCMWAIT[1:0]</td> <td>ATCM Wait Setting *1</td> <td>b1 b0 0 0: 1-wait with optimization 0 1: 1-wait without optimization 1 0: 0-wait 1 1: Setting prohibited</td> <td>R/W</td> </tr> <tr> <td>b31 to b2</td> <td>-</td> <td>Reserved</td> <td>These bits are read as 0. The write value should be 0.</td> <td>R/W</td> </tr> </tbody> </table> <p>Note 1. When the CPU clock frequency is 450 MHz/600 MHz, set these bits for "1-wait with optimization" or "1-wait without optimization". "0-wait" can be set only when the CPU clock frequency is 150 MHz or 300 MHz. It cannot be set when the frequency is 450 MHz/600 MHz.</p>	Bit	Symbol	Bit Name	Description	R/W	b1, b0	ATCMWAIT[1:0]	ATCM Wait Setting *1	b1 b0 0 0: 1-wait with optimization 0 1: 1-wait without optimization 1 0: 0-wait 1 1: Setting prohibited	R/W	b31 to b2	-	Reserved	These bits are read as 0. The write value should be 0.	R/W
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