Date: Jan. 16, 2023

# RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

| Product Category | MPU/MCU | | Document No. | TN-RZ*-A0108A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | RZ/G2H and RZ/G2N Correction/Additional for 59. Serial-ATA Gen3, SATA INT Status Register (SATAINTSTAT) | | Information Category | Technical Notification | | |
| Applicable Product | RZ/G Series, 2nd Generation<br>RZ/G2H<br>RZ/G2N | Lot No.<br>All lots | Reference Document | RZ/G Series, 2nd Generation<br>User's Manual: Hardware Rev.1.10<br>(R01UH0808EJ0110) | | |

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Correction/Additional for 59. Serial-ATA Gen3, SATA INT Status Register (SATAINTSTAT).

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2H

RZ/G2N

[Section number and title]

Section 59. Serial-ATA Gen3

(c) 2023. Renesas Electronics Corporation. All rights reserved.

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 59. Serial-ATA Gen3, Page 59-3, 59.1.4 Register Configuration. SATA INT mask register attribute of R/W is corrected.

Current (from):

### 59.1.4 Register Configuration

Table 59.2 shows the register configuration of the SATA interface. The set of registers shown below are allocated to the register map space.

The area allocated for the SATA interface is from H'EE30_0000 to H'EE4F_FFFF (2-Mbyte space).

These registers must not be accessed in any access sizes other than those listed in the table.

Addresses other than those listed below must not be write-accessed to. If written to, operation is not guaranteed. If read, an undefined value is read.

**Table 59.2 Register Configuration**

Add the offsets under “address” below to H'EE30_0000.

| | | | | | | Second Generation RZ/G Series Products | | | |
|---|---|---|---|---|---|---|---|---|---|
| Name | Symbol | R/W | Address | Initial Value | Access Size (Available Bit Size) | RZ/G2H | RZ/G2M V1.3 RZ/G2M V3.0 | RZ/G2N | RZ/G2E |
| **Serial-ATA HOST control registers** | | | | | | | | | |
| BIST config register | BISTCONF | R/W | H'102C | H'0000_0000 | 32 | √ | — | √ | — |
| Shadow data register | SDATA | R/W | H'1100 | H'0000_FFFF | 32 | √ | — | √ | — |
| Shadow error register | SSERR | R | H'1104 | H'0000_00FF | 32 | √ | — | √ | — |
| Shadow features register | SSFEATURES | W | H'1104 | H'0000_00FF | 32 | √ | — | √ | — |
| Shadow sector CNT register | SSECCNT | R/W | H'1108 | H'0000_00FF | 32 | √ | — | √ | — |
| Shadow LBA low register | SLBALOW | R/W | H'110C | H'0000_00FF | 32 | √ | — | √ | — |
| Shadow LBA mid register | SLBAMID | R/W | H'1110 | H'0000_00FF | 32 | √ | — | √ | — |
| Shadow LBA high register | SLBAHIGH | R/W | H'1114 | H'0000_00FF | 32 | √ | — | √ | — |
| Shadow device/head register | SDEVHEAD | R/W | H'1118 | H'0000_00FF | 32 | √ | — | √ | — |
| Shadow status register | SSSTATUS | R | H'111C | H'0000_007F | 32 | √ | — | √ | — |
| Shadow command register | SSCOM | W | H'111C | H'0000_00FF | 32 | √ | — | √ | — |
| Shadow alternate status register | SSALTSTS | R | H'1204 | H'0000_007F | 32 | √ | — | √ | — |
| Shadow device control register | SSDEVCON | W | H'1204 | H'0000_0000 | 32 | √ | — | √ | — |
| SATA extend ICC register | SATAEICCR | R | H'1220 | H'0000_0000 | 32 | √ | — | √ | — |
| SATA extend auxiliary register | SATAEAUXR | R | H'1224 | H'0000_0000 | 32 | √ | — | √ | — |
| SATA extend DEVSLP register | SATAEDEVSLPR | R/W | H'1228 | H'0000_0000 | 32 | √ | — | √ | — |
| SCR Sstatus register | SCRSSTS | R | H'1400 | H'0000_0000 | 32 | √ | — | √ | — |
| SCR Serror register | SCRSERR | R/WC1 | H'1404 | H'0000_0000 | 32 | √ | — | √ | — |
| SCR Scontrol register | SCRSCON | R/W | H'1408 | H'0000_0000 | 32 | √ | — | √ | — |
| SCR Sactive register | SCRSACT | R/W | H'140C | H'0000_0000 | 32 | √ | — | √ | — |
| SATA INT status register | SATAINTSTAT | RC | H'1508 | H'7F00_0000 | 32 | √ | — | √ | — |
| SATA INT mask register | SATAINTMASK | R/W | H'150C | H'0000_09FC | 32 | √ | — | √ | — |
| PHY STOP Register | PHYSTOP | R/W | H'1568 | H'0000_0000 | 32 | √ | — | √ | — |

Correct (to):

### 59.1.4 Register Configuration

Table 59.2 shows the register configuration of the SATA interface. The set of registers shown below are allocated to the register map space.

The area allocated for the SATA interface is from H'EE30_0000 to H'EE4F_FFFF (2-Mbyte space).

These registers must not be accessed in any access sizes other than those listed in the table.

Addresses other than those listed below must not be write-accessed to. If written to, operation is not guaranteed. If read, an undefined value is read.

**Table 59.2 Register Configuration**

Add the offsets under “address” below to H'EE30_0000.

| | | | | | | Second Generation RZ/G Series Products | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | **Symbol** | **R/W** | **Address** | **Initial Value** | **Access Size (Available Bit Size)** | **RZ/G2H** | **RZ/G2M V1.3 RZ/G2M V3.0** | **RZ/G2N** | **RZ/G2E** |
| **Serial-ATA HOST control registers** | | | | | | | | | |
| BIST config register | BISTCONF | R/W | H'102C | H'0000_0000 | 32 | √ | — | √ | — |
| Shadow data register | SDATA | R/W | H'1100 | H'0000_FFFF | 32 | √ | — | √ | — |
| Shadow error register | SSERR | R | H'1104 | H'0000_00FF | 32 | √ | — | √ | — |
| Shadow features register | SSFEATURES | W | H'1104 | H'0000_00FF | 32 | √ | — | √ | — |
| Shadow sector CNT register | SSECCNT | R/W | H'1108 | H'0000_00FF | 32 | √ | — | √ | — |
| Shadow LBA low register | SLBALOW | R/W | H'110C | H'0000_00FF | 32 | √ | — | √ | — |
| Shadow LBA mid register | SLBAMID | R/W | H'1110 | H'0000_00FF | 32 | √ | — | √ | — |
| Shadow LBA high register | SLBAHIGH | R/W | H'1114 | H'0000_00FF | 32 | √ | — | √ | — |
| Shadow device/head register | SDEVHEAD | R/W | H'1118 | H'0000_00FF | 32 | √ | — | √ | — |
| Shadow status register | SSSTATUS | R | H'111C | H'0000_007F | 32 | √ | — | √ | — |
| Shadow command register | SSCOM | W | H'111C | H'0000_00FF | 32 | √ | — | √ | — |
| Shadow alternate status register | SSALTSTS | R | H'1204 | H'0000_007F | 32 | √ | — | √ | — |
| Shadow device control register | SSDEVCON | W | H'1204 | H'0000_0000 | 32 | √ | — | √ | — |
| SATA extend ICC register | SATAEICCR | R | H’1220 | H'0000_0000 | 32 | √ | — | √ | — |
| SATA extend auxiliary register | SATAEAUXR | R | H’1224 | H'0000_0000 | 32 | √ | — | √ | — |
| SATA extend DEVSLP register | SATAEDEVSLPR | R/W | H’1228 | H'0000_0000 | 32 | √ | — | √ | — |
| SCR Sstatus register | SCRSSTS | R | H’1400 | H'0000_0000 | 32 | √ | — | √ | — |
| SCR Serror register | SCRSERR | R/WC1 | H'1404 | H'0000_0000 | 32 | √ | — | √ | — |
| SCR Scontrol register | SCRSCON | R/W | H'1408 | H'0000_0000 | 32 | √ | — | √ | — |
| SCR Sactive register | SCRSACT | R/W | H'140C | H'0000_0000 | 32 | √ | — | √ | — |
| SATA INT status register | SATAINTSTAT | R/WC0 RC[*3] | H'1508 | H'7F00_0000 | 32 | √ | — | √ | — |
| SATA INT mask register | SATAINTMASK | R/W | H'150C | H'0000_09FC | 32 | √ | — | √ | — |
| PHY STOP Register | PHYSTOP | R/W | H'1568 | H'0000_0000 | 32 | √ | — | √ | — |

Current (from):

| Name | Symbol | R/W | Address | Initial Value | Access Size (Available Bit Size) | Second Generation RZ/G Series Products | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | RZ/G2H | RZ/G2M V1.3 RZ/G2M V3.0 | RZ/G2N | RZ/G2E |
| Rx DMA setup FIS dword 0 register | DMADW0 | R/W | H'1620 | H'0000_0000 | 32 | √ | — | √ | — |
| Rx DMA setup FIS dword 1 register | DMADW1 | R/W | H'1624 | H'0000_0000 | 32 | √ | — | √ | — |
| Rx DMA setup FIS dword 2 register | DMADW2 | R/W | H'1628 | H'0000_0000 | 32 | √ | — | √ | — |
| Rx DMA setup FIS dword 3 register | DMADW3 | R/W | H'162C | H'0000_0000 | 32 | √ | — | √ | — |
| Rx DMA setup FIS dword 4 register | DMADW4 | R/W | H'1630 | H'0000_0000 | 32 | √ | — | √ | — |
| Rx DMA setup FIS dword 5 register | DMADW5 | R/W | H'1634 | H'0000_0000 | 32 | √ | — | √ | — |
| Rx DMA setup FIS dword 6 register | DMADW6 | R/W | H'1638 | H'0000_0000 | 32 | √ | — | √ | — |

Notes: See the descriptions of individual registers for the R/W attributes of the valid bits.
1. Bits 15 to 0 of the data bus are used.
2. Bits 7 to 0 of the data bus are used.

Correction (to):

| Name | Symbol | R/W | Address | Initial Value | Access Size (Available Bit Size) | Second Generation RZ/G Series Products | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | RZ/G2H | RZ/G2M V1.3 RZ/G2M V3.0 | RZ/G2N | RZ/G2E |
| Rx DMA setup FIS dword 0 register | DMADW0 | R/W | H'1620 | H'0000_0000 | 32 | √ | — | √ | — |
| Rx DMA setup FIS dword 1 register | DMADW1 | R/W | H'1624 | H'0000_0000 | 32 | √ | — | √ | — |
| Rx DMA setup FIS dword 2 register | DMADW2 | R/W | H'1628 | H'0000_0000 | 32 | √ | — | √ | — |
| Rx DMA setup FIS dword 3 register | DMADW3 | R/W | H'162C | H'0000_0000 | 32 | √ | — | √ | — |
| Rx DMA setup FIS dword 4 register | DMADW4 | R/W | H'1630 | H'0000_0000 | 32 | √ | — | √ | — |
| Rx DMA setup FIS dword 5 register | DMADW5 | R/W | H'1634 | H'0000_0000 | 32 | √ | — | √ | — |
| Rx DMA setup FIS dword 6 register | DMADW6 | R/W | H'1638 | H'0000_0000 | 32 | √ | — | √ | — |

Notes: See the descriptions of individual registers for the R/W attributes of the valid bits.

1. Bits 15 to 0 of the data bus are used.
2. Bits 7 to 0 of the data bus are used.
3. ISM in the ATAPI Control Register (ATAPI_CONTROL1) = 1 : R/WC0
   ISM in the ATAPI Control Register (ATAPI_CONTROL1) = 0 : RC
   For details, refer to section 59.3.4, Interrupt Modes.

[Description]

Error correction of descriptions for "R/W" of SATA INT Status Register (SATAINTSTAT)

Descriptions for "Notes" were added.

[Reason for Correction]

General error correction. (The contents of the 59.3.4 Interrupt Modes are not reflected to register explanation. )

[Correction]

2. Section 59. Serial-ATA Gen3, Page 59-41 to 59-42, 59.2.31 SATA INT Status Register (SATAINTSTAT), Bit-11 to 0, R/W attributes are corrected.

Current (from):

### 59.2.31 SATA INT Status Register (SATAINTSTAT)

| RZ/G2H | RZ/G2M V1.3, RZ/G2M V3.0 | RZ/G2N | RZ/G2E |
|---|---|---|---|
| √ | — | √ | — |

Bits 31 to 24 of the SATA INT status register are Shadow Status bits and mirror the value of the shadow status register. As with the shadow status register, accessing this register for read causes the ATA-sourced host_int_ata_intrq interrupt signal to be negated. (* The real entity of the register lies on the device side; the host side value is handled as a mirror value.)

Bits 11 to 0 of this register identify the interrupt source of the host_intrq signal. The bits that are masked by the SATA INT mask register (SATAINTMASK) do not cause the host_intrq signal to be asserted when the corresponding interrupt source event occurs. In this case, the pertinent bit is not set either.

| Bit: | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | INT BSY | INT DRDY | INT DFSE | INTSST ATUS | INT DRQ | — | — | INT ERR | — | — | — | — | — | — | — | — |
| Initial value: | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

| Bit: | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | SDBF | SLUMR | PARTI R | VEND | BIST | SLUM | PARTI | DMAST | SERR | ERR | ERR CRT | ATA |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R | R | R | RC | RC | RC | RC | RC | RC | RC | RC | RC | RC | RC | RC |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 31 | INTBSY | B'0 | R | BSY bit |
| 30 | INTDRDY | B'1 | R | DRDY bit |
| 29 | INTDFSE | B'1 | R | DF/SE bit |
| 28 | INTSSTATUS | B'1 | R | Definition varies with the command. |
| 27 | INTDRQ | B'1 | R | DRQ bit. |
| 26, 25 | — | B'11 | R | Reserved<br>These bits are always read as 1. |
| 24 | INTERR | B'1 | R | ERR/CHK bit |
| 23 to12 | — | All 0 | R | Reserved<br>These bits are always read as 0. |
| 11 | SDBF | B'0 | RC | Set Device Bits FIS reception |
| 10 | SLUMR | B'0 | RC | A request for transition to the Slumber state has been received (for device-initiated power management, i.e. DIPM). |
| 9 | PARTIR | B'0 | RC | A request for transition to the Partial state has been received (for device-initiated power management, i.e. DIPM). |
| 8 | VEND | B'0 | RC | Vendor Specific FIS reception |
| 7 | BIST | B'0 | RC | BIST Active FIS reception |
| 6 | SLUM | B'0 | RC | Device rejects transition to Slumber Mode.<br>Refer to notes 2. |

Correction (to);

### 59.2.31 SATA INT Status Register (SATAINTSTAT)

| RZ/G2H | RZ/G2M V1.3, RZ/G2M V3.0 | RZ/G2N | RZ/G2E |
|---|---|---|---|
| √ | — | √ | — |

Bits 31 to 24 of the SATA INT status register are Shadow Status bits and mirror the value of the shadow status register. As with the shadow status register, accessing this register for read causes the ATA-sourced host_int_ata_intrq interrupt signal to be negated. (* The real entity of the register lies on the device side; the host side value is handled as a mirror value.)

Bits 11 to 0 of this register identify the interrupt source of the host_intrq signal. The bits that are masked by the SATA INT mask register (SATAINTMASK) do not cause the host_intrq signal to be asserted when the corresponding interrupt source event occurs. In this case, the pertinent bit is not set either.

| Bit: | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | INT BSY | INT DRDY | INT DFSE | INTSST ATUS | INT DRQ | — | — | INT ERR | — | — | — | — | — | — | — | — |
| Initial value: | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

| Bit: | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | SDBF | SLUMR | PARTI R | VEND | BIST | SLUM | PARTI | DMAST | SERR | ERR | ERR CRT | ATA |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R | R | R | R/WC0 RC*3 | R/WC0 RC*3 | R/WC0 RC*3 | R/WC0 RC*3 | R/WC0 RC*3 | R/WC0 RC*3 | R/WC0 RC*3 | R/WC0 RC*3 | R/WC0 RC*3 | R/WC0 RC*3 | R/WC0 RC*3 | R/WC0 RC*3 |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 31 | INTBSY | B'0 | R | BSY bit |
| 30 | INTDRDY | B'1 | R | DRDY bit |
| 29 | INTDFSE | B'1 | R | DF/SE bit |
| 28 | INTSSTATUS | B'1 | R | Definition varies with the command. |
| 27 | INTDRQ | B'1 | R | DRQ bit. |
| 26, 25 | — | B'11 | R | Reserved<br>These bits are always read as 1. |
| 24 | INTERR | B'1 | R | ERR/CHK bit |
| 23 to12 | — | All 0 | R | Reserved<br>These bits are always read as 0. |
| 11 | SDBF | B'0 | R/WC0 RC*3 | Set Device Bits FIS reception |
| 10 | SLUMR | B'0 | R/WC0 RC*3 | A request for transition to the Slumber state has been received (for device-initiated power management, i.e. DIPM). |
| 9 | PARTIR | B'0 | R/WC0 RC*3 | A request for transition to the Partial state has been received (for device-initiated power management, i.e. DIPM). |
| 8 | VEND | B'0 | R/WC0 RC*3 | Vendor Specific FIS reception |
| 7 | BIST | B'0 | R/WC0 RC*3 | BIST Active FIS reception |
| 6 | SLUM | B'0 | R/WC0 RC*3 | Device rejects transition to Slumber Mode.<br>Refer to notes 2. |

Current (from):

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 5 | PARTI | B'0 | RC | Device rejects transition to Partial Mode.<br>Refer to notes 2. |
| 4 | DMAST | B'0 | RC | Same meaning as DMA Setup FIS reception (fpdma_req signal asserted) |
| 3 | SERR | B'0 | RC | SCR SERROR register update |
| 2 | ERR | B'0 | RC | SCR SERROR register (SCRSERR) ERRE, ERRP, ERRC, ERRT, ERRM, and ERRI bits update |
| 1 | ERRCRT | B'0 | RC | SCR SERROR register (SCRSERR) ERRE, ERRP, and ERRT bits update<br>Refer to notes 1. |
| 0 | ATA | B'0 | RC | ATA source (equivalent to P-ATA's INTRQ) |

Notes: 1. When the "SCR SError register ERRE, ERRP, and ERRT bits update" interrupt bit is set, it indicates that the condition cannot be recovered by this host controller module. In such a case, take appropriate actions according to the operating state established before the error occurred and the value of the SCR SError register (SCRSERR).
Example:
1) When the ERRT bit of the SCR SError register (SCRSERR) is set on completion of a PIO Read (data-in) transfer:
The read data contains an error bit. Restart processing at the issuance of the command.
2) When the ERRE bit of the SCR SError register (SCRSERR) is set during DMA transfer:
The data that is being transferred contains an error but since it cannot be detected by the device, it is necessary to perform a software reset and restart processing at the issuance of the command.
3) When the ERRP bit of the SCR SError register (SCRSERR) is set:
Perform a hardware reset and re-execute the preceding operation.

2. When a "device rejects transition to Slumber Mode" or "device rejects transition to Partial Mode" interrupt occurs, no request is reissued (retried) to the device. If requests should be made again, reset the SCR SControl register with a correct value.

Correction (to):

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 5 | PARTI | B'0 | R/WC0<br>RC*3 | Device rejects transition to Partial Mode.<br>Refer to notes 2. |
| 4 | DMAST | B'0 | R/WC0<br>RC*3 | Same meaning as DMA Setup FIS reception (fpdma_req signal asserted) |
| 3 | SERR | B'0 | R/WC0<br>RC*3 | SCR SERROR register update |
| 2 | ERR | B'0 | R/WC0<br>RC*3 | SCR SERROR register (SCRSERR) ERRE, ERRP, ERRC, ERRT, ERRM, and ERRI bits update |
| 1 | ERRCRT | B'0 | R/WC0<br>RC*3 | SCR SERROR register (SCRSERR) ERRE, ERRP, and ERRT bits update<br>Refer to notes 1. |
| 0 | ATA | B'0 | R/WC0<br>RC*3 | ATA source (equivalent to P-ATA's INTRQ) |

Notes: 1. When the "SCR SError register ERRE, ERRP, and ERRT bits update" interrupt bit is set, it indicates that the condition cannot be recovered by this host controller module. In such a case, take appropriate actions according to the operating state established before the error occurred and the value of the SCR SError register (SCRSERR).
Example:
1) When the ERRT bit of the SCR SError register (SCRSERR) is set on completion of a PIO Read (data-in) transfer:
The read data contains an error bit. Restart processing at the issuance of the command.
2) When the ERRE bit of the SCR SError register (SCRSERR) is set during DMA transfer:
The data that is being transferred contains an error but since it cannot be detected by the device, it is necessary to perform a software reset and restart processing at the issuance of the command.
3) When the ERRP bit of the SCR SError register (SCRSERR) is set:
Perform a hardware reset and re-execute the preceding operation.

2. When a "device rejects transition to Slumber Mode" or "device rejects transition to Partial Mode" interrupt occurs, no request is reissued (retried) to the device. If requests should be made again, reset the SCR SControl register with a correct value.

3. ISM in the ATAPI Control Register (ATAPI_CONTROL1) = 1 : R/WC0
ISM in the ATAPI Control Register (ATAPI_CONTROL1) = 0 : RC
For details, refer to section 59.3.4, Interrupt Modes.

[Description]

Wrong descriptions for "R/W" of Bit [2:0] description table

Descriptions for "Notes" were added.

[Reason for Correction]

General Error Correction. ( The contents of the 59.3.4 Interrupt Modes are not reflected to register explanation. )

- end of document -