Date: Nov. 11, 2022

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0101A/E	Rev.	1.00
Title	RZ/G1H, G1M, G1N and G1E Document Correction for VSP1		Information Category	Technical Notification		
Applicable Product	RZ/G Series, RZ/G1H, RZ/G1M, RZ/G1N, RZ/G1E	Lot No. All lots	Reference Document	RZ/G Series, User's Manual: Hardware Rev.1.00 (R01UH0543EJ0100)		

This technical update describes document correction of RZ/G Series product.

[Summary]

Document correction for RZ/G Series, User’s Manual: Hardware Rev.1.00.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G1H

RZ/G1M

RZ/G1N

RZ/G1E

[Section number and title]

Section 28. VSP1

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 28. VSP1, Page 28-54, Section 28.2.5.9 WPFn Output Line Count Register (VI6_WPFn_LINE_CNT: n = 0, 1, 2, 3).

Current (from):

28.2.5.9 WPFn Output Line Count Register (VI6_WPFn_LINE_CNT: n = 0, 1, 2, 3)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	LINE_CNT [20:16]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LINE_CNT [15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 0	LINE_CNT [20:0]	All 0	R	Number of WPFn Output Lines From the value read from these bits, the number of lines output from VSP1 can be obtained. The value of these bits can be read only within a limited period; read these bits with the timing described later. These bits indicate the number of lines output from WPFn as an immediate value. In the frame buffer starting from VI6_WPFn_DSTM_ADDR_*, WPFn has completed data output up to the line number indicated in these bits. For example, when these bits are set to 1, valid data is output only in the first line. When one-frame processing is competed correctly, this value indicates the number of lines output from WPFn.

The LINE_CNT value is valid only for the period between a frame end interrupt (section 28.2.5.6) and next frame startup (section 28.2.5.1) or the period between a display list frame end interrupt (section 28.2.5.6) and next frame startup. This register value read outside these periods cannot be used.

The LINE_CNT value depends on the flipping mode (VI6_WPFn_OUTFMT.FLP) as shown in Figure 28.15. This correspondence is shown in Table 28.16.

Table 28.16 VSP1 Output Line Count According to VI6_WPFn_OUTFMT.FLP Setting

VI6_WPFn_OUTFMT.FLP Setting	Corresponding Case Shown in Figure 28.15
0	case 1
1	case 2

Correction (to):

28.2.5.9 WPFn Output Line Count Register (VI6_WPFn_LINE_CNT: n = 0, 1, 2, 3)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
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	—	—	—	—	—	—	—	—	—	—	—	LINE_CNT [20:16]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LINE_CNT [15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

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[Description]

Clerical error in Register bit assign table.

[Reason for Correction]

Correction of errors for Register bit assign table.

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