Date: Nov.14, 2022

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RZ*-A0102A/E	Rev.	1.00
Title	RZ/G1H, G1M, G1N and G1E Document Correction for Electrical Characteristics		Information Category	Technical Notification		
Applicable Product	RZ/G Series, RZ/G1H, RZ/G1M, RZ/G1N, RZ/G1E	Lot No. All lots	Reference Document	RZ/G Series, User's Manual: Hardware Rev.1.00 (R01UH0543EJ0100)		

This technical update describes document correction of RZ/G Series product.

[Summary]

Document correction for RZ/G Series, User’s Manual: Hardware Rev.1.00.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G1H,

RZ/G1M,

RZ/G1N,

RZ/G1E

[Section number and title]

Section 63. EC (Electrical Characteristics)

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 63. EC, Page 63-1, Section 63.1 Absolute Maximum Ratings.

Current (from):

RZ/G1H RZ/G1N RZ/G1M RZ/G1E

63.1 Absolute Maximum Ratings

Table 63.1.1 Absolute Maximum Ratings

Item	Value	Unit	Remarks
Power supply voltage (3.3 V) (VCCQ, VCCQ33_MLBP, VCCQ_SD (SDHI), VD331)	-0.3 to +4.6	V	H, M and N
Power supply voltage (3.3 V) (VCCQ, VCCQ_SD/VCCQ_MMC_SD (SDHI), VD331)			E
Power supply voltage (1.8 V) (AVDD, VCCQ18, VCCQ_ISO, VCCQ_SD (SDR50/SDR104), VDD_CPGPLL, VDDA_SATA0/1, VDDQ_LVDS, VCCQ18_MLBP, VDDQ_M0APLL, VDDQ_M1APLL, VDDQ_M0DPLL, VDDQ_M1DPLL, VDDQ_M1MPLL, DU/DU0_LVDS0/LVDS_PLL1_VCC (H/M), DU_LVDS1_PLL1_VCC (H only), VDD_MLBPLL, VDD_MLBPPLL0, VDD_MLBPPLL1)	-0.3 to +2.5	V	H, M and N (DU_LVDS1_PLL1_VCC: H only)
Power supply voltage (1.8 V) (AVDD, VCCQ18, VCCQ_SD/VCCQ_MMC_SD (SDR50/SDR104), VDD_CPGPLL, VDD_MLBPLL, VDDQ_M0APLL, VDDQ_M0DPLL)			E
Power supply voltage (1.5V) (VDDQ_M0)	-0.3 to +1.875	V	—
Power supply voltage (1.5V) (VDDQ_M1, VDDQ_M1A)			H and M
Power supply voltage (1.35 V) (VDDQ_M0)	-0.3 to +1.75	V	—
Power supply voltage (1.35 V) (VDDQ_M1, VDDQ_M1A)			H and M
Power supply voltage (1.0 V) (VDD)	-0.3 to +1.26	V	—
Power supply voltage (1.0 V) (VDD_DVFS, VDDD_SATA0/1)			H, M and N
Input voltage (3.3-V I/O, 3.3-V tolerant I/O)	-0.3 to VCCQ + 0.3	V	*1
Input voltage (3.3-V I/O)	-0.3 to VCCQ33_MLBP + 0.3	V	*1, H, M and N
Input voltage (3.3-V I/O [SDHI])	-0.3 to VCCQ_SD/VCCQ_MMC_SD + 0.3	V	*1, H, M, N and E
Input voltage (1.8-V I/O)	-0.3 to VCCQ18 + 0.3	V	*2, except for 3.3-V tolerant I/O
Input voltage (1.8-V I/O [SDHI (SDR50/SDR104)])	-0.3 to VCCQ_SD/VCCQ_MMC_SD + 0.3	V	*2, H, M, N and E
Input voltage (1.8-V I/O)	-0.3 to VCCQ18_MLBP + 0.3	V	*2, H, M and N
Input voltage (1.5-V I/O [DDR3])	-0.3 to VDDQ_M0/M1/M1A + 0.3	V	*3, H and E, M1/M1A: H

Correction (to):

63.1 Absolute Maximum Ratings

RZ/G1H RZ/G1N RZ/G1M RZ/G1E

Table 63.1.1 Absolute Maximum Ratings

Item	Value	Unit	Remarks
Power supply voltage (3.3 V) (VCCQ, VCCQ33_MLBP, VCCQ_SD (SDHI), VD331)	-0.3 to +4.6	V	H, M and N
Power supply voltage (3.3 V) (VCCQ, VCCQ_SD/VCCQ_MMC_SD (SDHI), VD331)			E
Power supply voltage (1.8 V) (AVDD, VCCQ18, VCCQ_ISO, VCCQ_SD (SDR50/SDR104), VDD_CPGPLL, VDDA_SATA0/1, VDDQ_LVDS, VCCQ18_MLBP, VDDQ_M0APLL, VDDQ_M1APLL, VDDQ_M0DPLL, VDDQ_M1DPLL, VDDQ_M1MPLL, DU/DU0_LVDS0/LVDS_PLL1_VCC (H/M), DU_LVDS1_PLL1_VCC (H only), VDD_MLBPLL, VDD_MLBPPLL0, VDD_MLBPPLL1)	-0.3 to +2.5	V	H, M and N (DU_LVDS1_PLL1_VCC: H only)
Power supply voltage (1.8 V) (AVDD, VCCQ18, VCCQ_SD/VCCQ_MMC_SD (SDR50/SDR104), VDD_CPGPLL, VDD_MLBPLL, VDDQ_M0APLL, VDDQ_M0DPLL)			E
Power supply voltage (1.5 V) (VDDQ_M0, VDDQ_M0BKUP))	-0.3 to +1.875	V	—
Power supply voltage (1.5 V) (VDDQ_M1,VDDQ_M1BKUP, VDDQ_M1A)			H and M
Power supply voltage (1.35 V) (VDDQ_M0, VDDQ_M0BKUP)	-0.3 to +1.75	V	—
Power supply voltage (1.35 V) (VDDQ_M1, VDDQ_M1BKUP, VDDQ_M1A)			H and M
Power supply voltage (1.0 V) (VDD)	-0.3 to +1.26	V	—
Power supply voltage (1.0 V) (VDD_DVFS, VDDD_SATA0/1)			H, M and N
Input voltage (3.3-V I/O, 3.3-V tolerant I/O)	-0.3 to VCCQ + 0.3	V	*1
Input voltage (3.3-V I/O)	-0.3 to VCCQ33_MLBP + 0.3	V	*1, H, M and N
Input voltage (3.3-V I/O [SDHI])	-0.3 to VCCQ_SD/VCCQ_MMC_SD + 0.3	V	*1, H, M, N and E
Input voltage (1.8-V I/O)	-0.3 to VCCQ18 + 0.3	V	*2, except for 3.3-V tolerant I/O
Input voltage (1.8-V I/O [SDHI (SDR50/SDR104)])	-0.3 to VCCQ_SD/VCCQ_MMC_SD + 0.3	V	*2, H, M, N and E
Input voltage (1.8-V I/O)	-0.3 to VCCQ18_MLBP + 0.3	V	*2, H, M and N
Input voltage (1.5-V I/O [DDR3])	-0.3 to VDDQ_M0/M1/M1A + 0.3	V	*3, H and E, M1/M1A: H

[Description]

Add VDDQ_M0BKUP or VDDQ_M1BKUP to the Item.

[Reason for Correction]

General error correction.

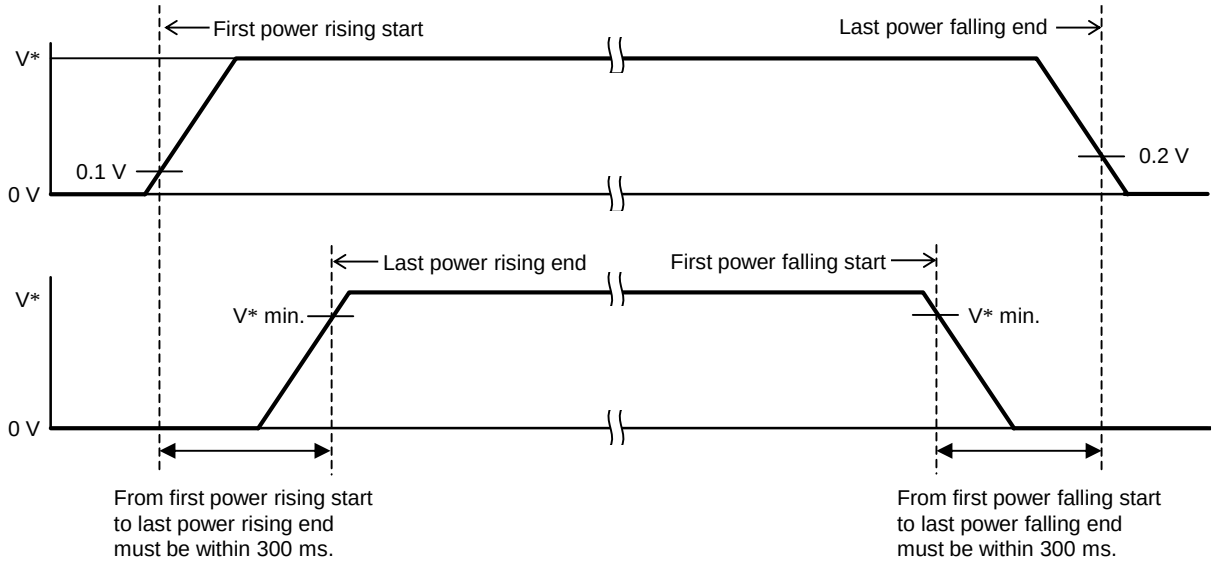
[Correction]

2. Section 63. EC, Page 63-8, Section 63.2 Power On and Power Off Wave Form.

Current (from):

63.3.2 Power On and Power Off Wave Form

RZ/G1H RZ/G1N RZ/G1M RZ/G1E

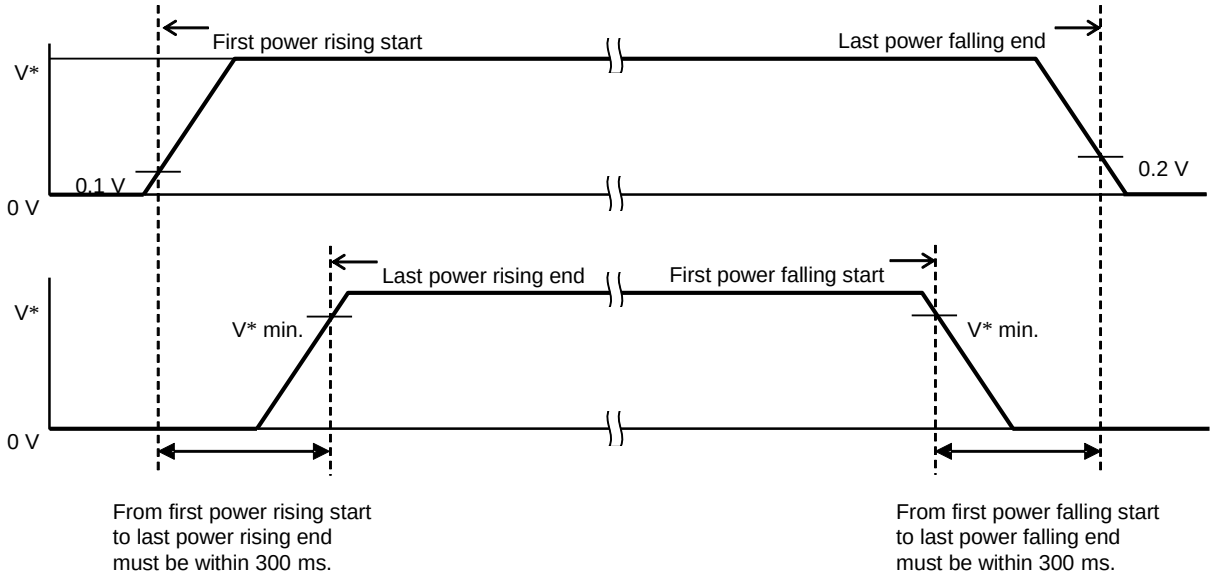


Note: For all V*, power off state must be 0 V (GND), power rising must be started from 0 V and power falling must be ended to 0 V (excluding DDR-SDRAM power-supply backup state).
Periods from 0 V to 0.1 V at power-on and from 0.2 V to 0 V at power-off should be shortened as much as possible.

Correction (to):

63.3.2 Power On and Power Off Wave Form

RZ/G1H RZ/G1N RZ/G1M RZ/G1E



From first power rising start to last power rising end must be within 300 ms.

From first power falling start to last power falling end must be within 300 ms.

Note: For all V*, power off state must be 0 V (GND), power rising must be started from 0 V and power falling must be ended to 0 V (excluding DDR- SDRAM power supply backup state).
Periods from 0 V to 0.1 V at power on and from 0.2 V to 0 V at power off should be shortened as much as possible
Regarding the wave forms of power rising and power falling, they need rmonotonious increase and decrease respectively to prevent malfunctions.

[Description]

Add note of the wave forms of power rising and falling.

[Reason for Correction]

General error correction.

[Correction]

3. Table 63.4.10 DC Characteristics (1.5-V I/O [DDR3]), Item: AC differential output cross point voltage, Remarks, Page63-19

Current (from):

RZ/G1H RZ/G1E

Table 63.4.10 DC Characteristics (1.5-V I/O [DDR3])

DDR3 channel 1 is available for H (VDDQ_M1, M1xxx signals)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
AC differential input cross point voltage	VIX (AC)	0.5 × VDDQ_M0, VDDQ_M1 - 0.15	—	0.5 × VDDQ_M0, VDDQ_M1 + 0.15	V	VDDQ_M0 = VDDQ_M1 = 1.425 to 1.575 V	M0DQS and M1DQS pins *2
AC differential output cross point voltage	VOX (AC)	VREF - 0.125	—	VREF + 0.125	V	—	M0CK, M0DQS, M1CK, and M1DQS pins (PU,PD not used, 5.5kohm used, 500ohm used)
High Hi-Z leak current	IOZH	—	—	4	µA	—	Other than M0ZQ and M1ZQ pins
Low Hi-Z leak current	IOZL	-4	—	—	µA	—	
High Hi-Z leak current	IOZH	—	—	5	µA	—	M0ZQ and M1ZQ pins
Low Hi-Z leak current	IOZL	-5	—	—	µA	—	
Pin capacitance	CL	—	—	15	pF	—	All pins*3
PLL power supply	*4	1.62	1.8	1.98	V	—	—

Notes: 1. Peak to peak ac noise on VREF may not exceed ±2 % of VREF.

2. The VIX (AC) indicates the voltage at which differential input signals cross each other. The typical value of VIX (AC) is expected to be 0.5 × VDDQ_M0, VDDQ_M1.

3. Except power supply pins.

4. VDDQ_M0APLL, VDDQ_M1APLL, VDDQ_M1MPLL, VDDQ_M0DPLL0 to VDDQ_M0DPLL3 pins.

Correction (to):

RZ/G1H RZ/G1E

Table 63.4.10 DC Characteristics (1.5-V I/O [DDR3])

DDR3 channel 1 is available for H (VDDQ_M1, M1xxx signals)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
AC differential input cross point voltage	VIX (AC)	0.5 × VDDQ_M0, VDDQ_M1 - 0.15	—	0.5 × VDDQ_M0, VDDQ_M1 + 0.15	V	VDDQ_M0 = VDDQ_M1 = 1.425 to 1.575 V	M0DQS and M1DQS pins *2
AC differential output cross point voltage	VOX (AC)	VREF - 0.125	—	VREF + 0.125	V	—	M0CK, M0DQS, M1CK, and M1DQS pins
High Hi-Z leak current	IOZH	—	—	4	µA	—	Other than M0ZQ and M1ZQ pins
Low Hi-Z leak current	IOZL	-4	—	—	µA	—	
High Hi-Z leak current	IOZH	—	—	5	µA	—	M0ZQ and M1ZQ pins
Low Hi-Z leak current	IOZL	-5	—	—	µA	—	
Pin capacitance	CL	—	—	15	pF	—	All pins*3
PLL power supply	*4	1.62	1.8	1.98	V	—	—

Notes: 1. Peak to peak ac noise on VREF may not exceed ±2 % of VREF.

2. The VIX (AC) indicates the voltage at which differential input signals cross each other. The typical value of VIX (AC) is expected to be 0.5 × VDDQ_M0, VDDQ_M1.

3. Except power supply pins.

4. VDDQ_M0APLL, VDDQ_M1APLL, VDDQ_M1MPLL, VDDQ_M0DPLL0 to VDDQ_M0DPLL3 pins.

[Description]

Delete the unnecessary information in the Remarks.

[Reason for Correction]

General error correction.

[Correction]

4. Table 63.4.12 DC Characteristics (1.35-V I/O [DDR3L]), Item: AC differential input cross point voltage, Remarks, page 63-21

Current (from):

RZ/G1M RZ/G1N

Table 63.4.12 DC Characteristics (1.35-V I/O [DDR3L])

DDR3 channel 1 is available for H (VDDQ_M1, M1xxx signals)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
AC differential input cross point voltage	VIX (AC)	0.5 × VDDQ_M0, VDDQ_M1 - 0.15	—	0.5 × VDDQ_M0, VDDQ_M1 + 0.15	V	VDDQ_M0 = VDDQ_M1 = 1.283 to 1.450 V	M0DQS and M1DQS pins *2
AC differential output cross point voltage	VOX (AC)	VREF - 0.125	—	VREF + 0.125	V	VDDQ_M0 = VDDQ_M1 = 1.450 V	M0CK, M0DQS, M1CK, and M1DQS pins (PU,PD not used, 5.5kohm used, 500ohm used)
High Hi-Z leak current	IOZH	—	—	4	µA	VDDQ_M0 = VDDQ_M1 = 1.450 V	Other than M0ZQ and M1ZQ pins
Low Hi-Z leak current	IOZL	-4	—	—	µA	VDDQ_M0 = VDDQ_M1 = 1.450 V	
High Hi-Z leak current	IOZH	—	—	5	µA	VDDQ_M0 = VDDQ_M1 = 1.450 V	M0ZQ and M1ZQ pins
Low Hi-Z leak current	IOZL	-5	—	—	µA	VDDQ_M0 = VDDQ_M1 = 1.450 V	
Pin capacitance	CL	—	—	15	pF	—	All pins*3
PLL power supply	*4	1.62	1.8	1.98	V	—	—

Notes: 1. Peak to peak ac noise on VREF may not exceed ±2 % of VREF.
2. The VIX (AC) indicates the voltage at which differential input signals cross each other. The typical value of VIX (AC) is expected to be 0.5 × VDDQ_M0, VDDQ_M1.
3. Except power supply pins.
4. VDDQ_M0APLL, VDDQ_M1APLL, VDDQ_M1MPLL, VDDQ_M0DPLL0 to VDDQ_M0DPLL3 pins.

Correction (to):

Table 63.4.12 DC Characteristics (1.35-V I/O [DDR3L]) RZ/G1M RZ/G1N

DDR3L channel 1 is available for H (VDDQ_M1, M1xxx signals)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
AC differential input cross point voltage	VIX (AC)	0.5 × VDDQ_M0, VDDQ_M1 - 0.15	—	0.5 × VDDQ_M0, VDDQ_M1 + 0.15	V	VDDQ_M0 = VDDQ_M1 = 1.283 to 1.450 V	M0DQS and M1DQS pins *2
AC differential output cross point voltage	VOX (AC)	VREF - 0.125	—	VREF + 0.125	V	VDDQ_M0 = VDDQ_M1 = 1.450 V	M0CK, M0DQS, M1CK, and M1DQS pins
High Hi-Z leak current	IOZH	—	—	4	µA	VDDQ_M0 = VDDQ_M1 = 1.450 V	Other than M0ZQ and M1ZQ pins
Low Hi-Z leak current	IOZL	-4	—	—	µA	VDDQ_M0 = VDDQ_M1 = 1.450 V	
High Hi-Z leak current	IOZH	—	—	5	µA	VDDQ_M0 = VDDQ_M1 = 1.450 V	M0ZQ and M1ZQ pins
Low Hi-Z leak current	IOZL	-5	—	—	µA	VDDQ_M0 = VDDQ_M1 = 1.450 V	
Pin capacitance	CL	—	—	15	pF	—	All pins*3
PLL power supply	*4	1.62	1.8	1.98	V	—	—

Notes: 1. Peak to peak ac noise on VREF may not exceed ±2 % of VREF.
2. The VIX (AC) indicates the voltage at which differential input signals cross each other. The typical value of VIX (AC) is expected to be 0.5 × VDDQ_M0, VDDQ_M1.
3. Except power supply pins.
4. VDDQ_M0APLL, VDDQ_M1APLL, VDDQ_M1MPLL, VDDQ_M0DPLL0 to VDDQ_M0DPLL3 pins.

[Description]

Delete the unnecessary information in the Remarks.

[Reason for Correction]

General error correction.

[Correction]

5. Section 63. EC, Page 63-24, Section 63.5A EXTAL Clock Input/output Timing. Added new section for clock input timing specifications.

Current (from):

— (None of section)

Correction (to):

63.5A EXTAL Clock Input/output Timing

63.5A.1 EXTAL Clock Input Timing

RZ/G1H RZ/G1N RZ/G1M RZ/G1E

Table 63.5A.1 EXTAL Clock Input Timing

Conditions: VCCQ/VDDQ = 3.3 V ± 0.3 V, VCCQ18/VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V,
Tc = -40 to +105 ℃

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks	Figure
EXTAL clock input frequency	MD[14:13] = LL	fEX	12.6	15.0	15.1	MHz	Frequency deviation: ±50 ppm or less	—
	MD[14:13] = LH		16.8	20.0	20.1	MHz		
	MD[14:13] = HL		22.0	26.0	26.1	MHz		
	MD[14:13] = HH		25.1	30.0	30.1	MHz		
EXTAL clock input cycle time	MD[14:13] = LL	tEXcyc	66.23	66.67	79.37	ns		Figure 63.5A.1
	MD[14:13] = LH		49.75	50.00	59.52	ns		
	MD[14:13] = HL		38.31	38.46	45.45	ns		
	MD[14:13] = HH		33.22	33.33	39.84	ns		
EXTAL clock input duty cycle time		tEXduty	0.4	0.5	0.6	tEXcyc		
EXTAL clock input low-level pulse width		tEXL	5	—	—	ns		
EXTAL clock input high-level pulse width		tEXH	5	—	—	ns		
EXTAL clock input rise time		tEXr	—	—	4	ns		
EXTAL clock input fall time		tEXf	—	—	4	ns		

Note: Set the MD9 pin to L (low) during power-on reset when using the EXTAL pin as external clock input and the XTAL pin must be open.
Not to exceed the specification of DDR3 operating frequency, Input the lower frequency of EXTAL or lower the multiplication rate of PLL.

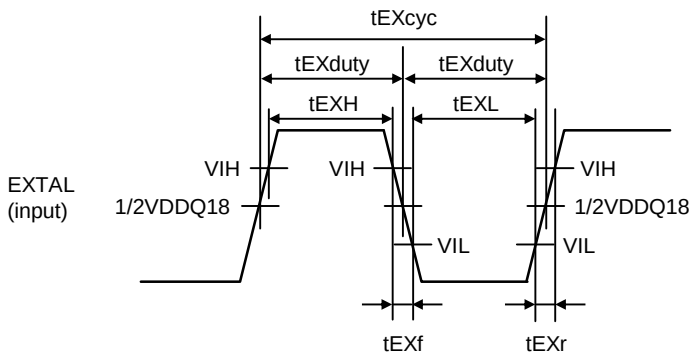


Figure 63.5A.1 EXTAL Clock Input Timing

Current (from):

— (None of section)

Correction (to):

63.5A.2 CLKOUT Clock Output Timing

RZ/G1H

Table 63.5A.2(1) CLKOUT Clock Output Timing (RZ/G1H)

Conditions: VDDQ = 3.3 ± 0.3 V, GND = VSSQ = 0 V, Tc = −40 to +105 °C,
CL = 40 pF

Item		Symbol	Min.	Typ.	Max.	Unit	Figure
CLKOUT clock output frequency	MD18 = L	fCKO	54.38	65.00	65.43	MHz	—
	MD18 = H		36.26	43.33	43.62	MHz	
CLKOUT clock output cycle time	MD18 = L	tCKOcyc	15.28	15.38	18.39	ns	Figure 63.5A.2
	MD18 = H		22.92	23.08	27.58	ns	
CLKOUT clock output duty cycle time		tCKOduty	0.4	0.5	0.6	tCKOcyc	

Table 63.5A.2(2) CLKOUT Clock Output Timing (RZ/G1M, RZ/G1N and RZ/G1E)

RZ/G1N RZ/G1M RZ/G1E

Conditions: VDDQ = 3.3 ± 0.3 V, GND = VSSQ = 0 V, Tc = −40 to +105 °C,
CL = 40 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
CLKOUT clock output frequency	fCKO	54.38	65.00	65.43	MHz	—
CLKOUT clock output cycle time	tCKOcyc	15.28	15.38	18.39	ns	Figure 63.5A.2
CLKOUT clock output duty cycle time	tCKOduty	0.4	0.5	0.6	tCKOcyc	

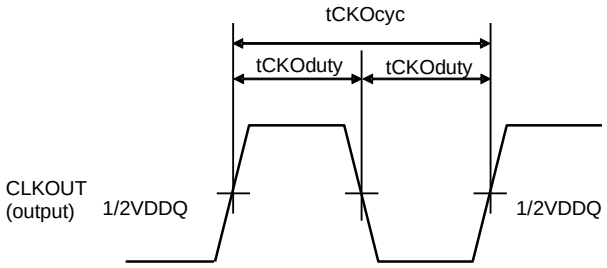


Figure 63.5A.2 CLKOUT Clock Output Timing

[Description]

Add the timing of EXTAL Clock Input and CLKOUT Clock Output.

[Reason for Correction]

Additional explanation.

[Correction]

6. Section 63. EC, Page 63-46, Section 63.10 Video Input Module (VIN). Correction of capture timing Figure 63.10.1

Current (from):

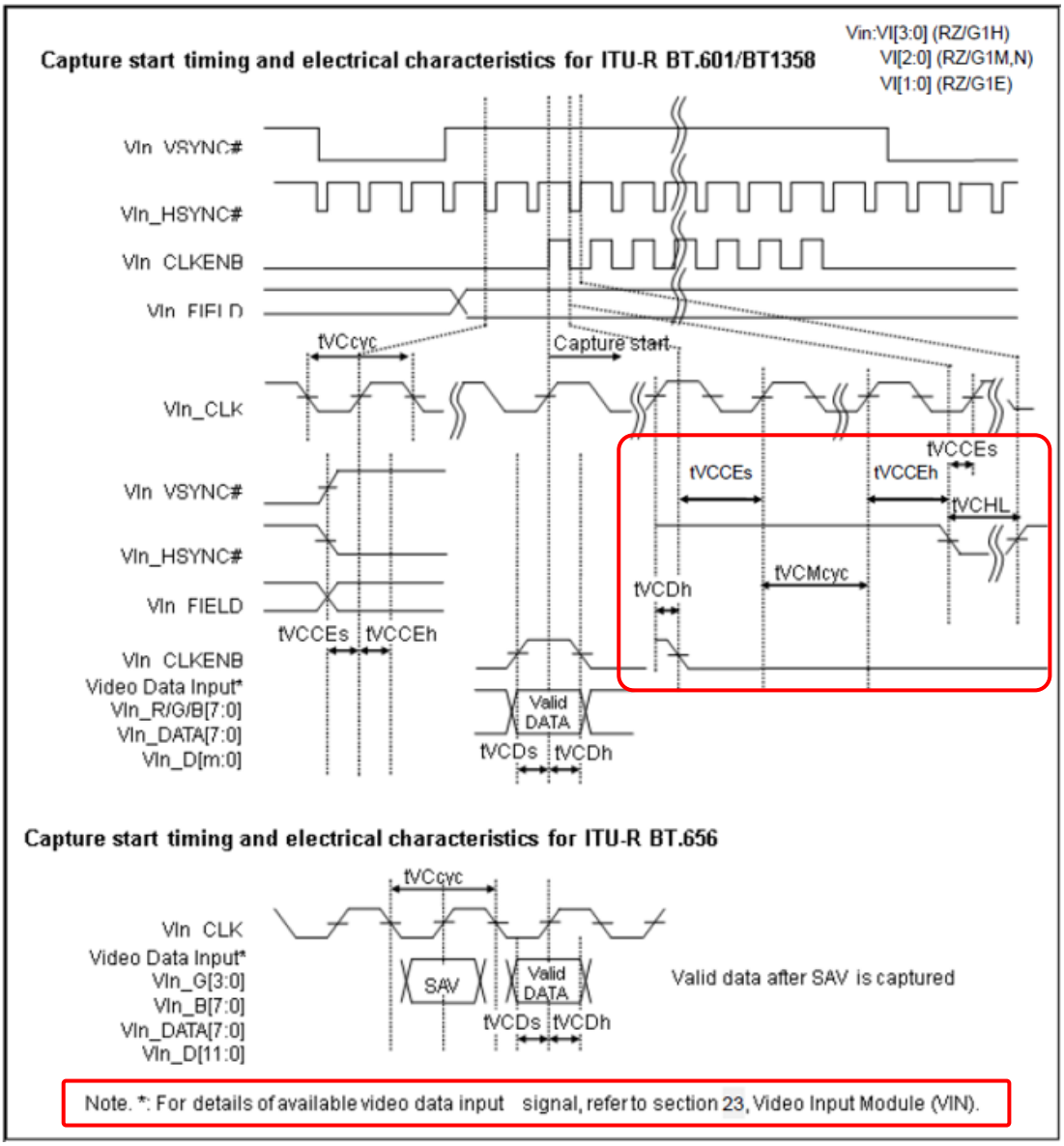


Figure 63.10.1 Capture start timing and electrical characteristics [H, M, N, E]

Correction (to):

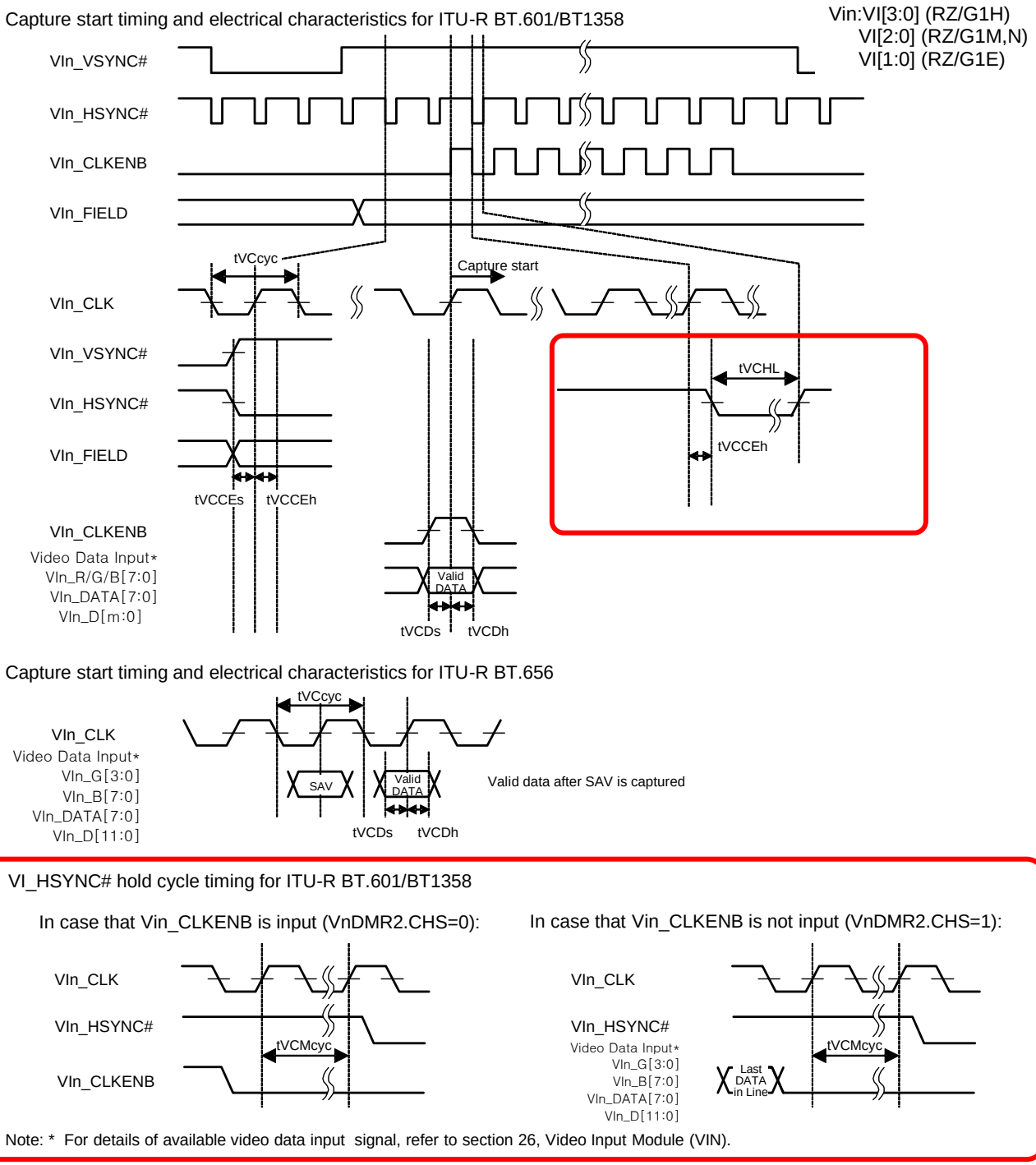


Figure 63.10.1 Capture start timing and electrical characteristics [H, M, N, E]

[Description]

Add figure of VI_HSYNC# hold cycle timing.

[Reason for Correction]

General error correction.

- End of Document -