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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A158A/E	Rev.	1.00
Title	RX64M, RX71M Group Modified high-impedance control in POE3.		Information Category	Technical Notification		
Applicable Product	RX71M Group、RX64M Group	Lot No. All	Reference Document	RX71M Group User's Manual: Hardware、(R01UH0493EJ0100) RX64M Group User's Manual: Hardware (R01UH0377EJ100)		

This document describes modifications in section 25.3 Operation for high-impedance control.

【Before】

25.3 Operation

The following shows the target pins and conditions for high-impedance control.

(1) MTU3 pins or GPT0 pins*1 (MTIOC3B/GTIOC0A, MTIOC3D/GTIOC0B)

When one of the following conditions is satisfied, the pins are placed in high-impedance state.

・Operation for detection of the POE0# input level

When the OCSR1.OCE1 bit is set to 1 while the ICSR1.POE0F and OCSR1.OSF1 flags are 1.

・Operation for comparison of the output levels on the MTIOC3B and MTIOC3D or GTIOC0A and GTIOC0B pins

When the OCSR1.OCF1 flag is set to 1 while the POECR2.MTU3BDZE bit is 1.

・SPOER setting

When the SPOER.MTUCH34HIZ bit is set to 1 while the POECR2.MTU3BDZE bit is 1.

・Conditions added by POECR4

When the ICSR2.POE4F flag is set to 1 while the POECR2.MTU3BDZE and POECR4.IC2ADDMT34ZE bits are 1.

When the ICSR3.POE8F flag and the ICSR3.POE8E bit are set to 1 while the POECR2.MTU3BDZE and POECR4.IC3ADDMT34ZE bits are 1.

When the ICSR4.POE10F flag and the ICSR4.POE10E bit are set to 1 while the POECR2.MTU3BDZE and POECR4.IC4ADDMT34ZE bits are 1.

When the ICSR5.POE11F flag and the ICSR5.POE11E bit are set to 1 while the POECR2.MTU3BDZE and POECR4.IC5ADDMT34ZE bits are 1.

・Detection of stopped oscillation

When the ICSR6.OSTSTF flag and the ICSR6.OSTSTE bit are set to 1 while the POECR2.MTU3BDZE bit is 1.

Note 1. The pins are enabled only when either MTU or GPT pins are selected in the MGSELR register.

(2) MTU4 pins or GPT1 pins*1 (MTIOC4A/GTIOC1A, MTIOC4C/GTIOC1B)

When one of the following conditions is satisfied, the pins are placed in high-impedance state.

- Operation for detection of the POE0# input level

  When the OCSR1.OCE1 bit is set to 1 while the ICSR1.POE0F and OCSR1.OSF1 flags are 1.
- Operation for comparison of the output levels on the MTIOC4A and MTIOC4C or GTIOC1A and GTIOC1B pins

  When the OCSR1.OCF1 flag is set to 1 while the POECR2.MTU4ACZE bit is 1.
- SPOER setting

  When the SPOER.MTUCH34HIZ bit is set to 1 while the POECR2.MTU4ACZE bit is 1.
- Conditions added by POECR4

  When the ICSR2.POE4F flag is set to 1 while the POECR2.MTU4ACZE and POECR4.IC2ADDMT34ZE bits are 1.

  When the ICSR3.POE8F flag and the ICSR3.POE8E bit are set to 1 while the POECR2.MTU4ACZE and POECR4.IC3ADDMT34ZE bits are 1.

  When the ICSR4.POE10F flag and the ICSR4.POE10E bit are set to 1 while the POECR2.MTU4ACZE and POECR4.IC4ADDMT34ZE bits are 1.

  When the ICSR5.POE11F flag and the ICSR5.POE11E bit are set to 1 while the POECR2.MTU4ACZE and POECR4.IC5ADDMT34ZE bits are 1.
- Detection of stopped oscillation

  When the ICSR6.OSTSTF flag and the ICSR6.OSTSTE bit are set to 1 while the POECR2.MTU4ACZE bit is 1.

Note 1. The pins are enabled only when either MTU or GPT pins are selected in the MGSELR register.

(3) MTU4 pins or GPT2 pins*1 (MTIOC4B/GTIOC2A, MTIOC4D/GTIOC2B)

When one of the following conditions is satisfied, the pins are placed in high-impedance state.

- Operation for detection of the POE0# input level

  When the OCSR1.OCE1 bit is set to 1 while the ICSR1.POE0F and OCSR1.OSF1 flags are 1.
- Operation for comparison of the output levels on the MTIOC4B and MTIOC4D or GTIOC2A and GTIOC2B pins

  When the OCSR1.OCF1 flag is set to 1 while the POECR2.MTU4BDZE bit is 1.
- SPOER setting

  When the SPOER.MTUCH34HIZ bit is set to 1 while the POECR2.MTU4BDZE bit is 1.
- Conditions added by POECR4

  When the ICSR2.POE4F flag is set to 1 while the POECR2.MTU4BDZE and POECR4.IC2ADDMT34ZE bits are 1.

  When the ICSR3.POE8F flag and the ICSR3.POE8E bit are set to 1 while the POECR2.MTU4BDZE and POECR4.IC3ADDMT34ZE bits are 1.

  When the ICSR4.POE10F flag and the ICSR4.POE10E bit are set to 1 while the POECR2.MTU4BDZE and POECR4.IC4ADDMT34ZE bits are 1.

  When the ICSR5.POE11F flag and the ICSR5.POE11E bit are set to 1 while the POECR2.MTU4BDZE and POECR4.IC5ADDMT34ZE bits are 1.
- Detection of stopped oscillation

  When the ICSR6.OSTSTF flag and the ICSR6.OSTSTE bit are set to 1 while the POECR2.MTU4BDZE bit is 1.

Note 1. The pins are enabled only when either MTU or GPT pins are selected in the MGSELR register.

(4) MTU6 pins (MTIOC6B, MTIOC6D)

When one of the following conditions is satisfied, the pins are placed in high-impedance state.

- Operation for detection of the POE4# input level

  When the OCSR2.OCE2 bit is set to 1 while the ICSR2.POE4F and OCSR2.OSF2 flags are 1.
- Operation for comparison of the output levels on the MTIOC6B and MTIOC6D pins

  When the OCSR2.OSF2 flag is set to 1 while the POECR2.MTU6BDZE bit is 1.
- SPOER setting

  When the SPOER.MTUCH67HIZ bit is set to 1 while the POECR2.MTU6BDZE bit is 1.
- Conditions added by POECR4

  When the ICSR1.POE0F flag is set to 1 while the POECR2.MTU6BDZE and POECR4.IC1ADDMT67ZE bits are 1.

  When the ICSR3.POE8F flag and the ICSR3.POE8E bit are set to 1 while the POECR2.MTU6BDZE and POECR4.IC3ADDMT67ZE bits are 1.

  When the ICSR4.POE10F flag and the ICSR4.POE10E bit are set to 1 while the POECR2.MTU6BDZE and POECR4.IC4ADDMT67ZE bits are 1.

  When the ICSR5.POE11F flag and the ICSR5.POE11E bit are set to 1 while the POECR2.MTU6BDZE and POECR4.IC5ADDMT67ZE bits are 1.
- Detection of stopped oscillation

  When the ICSR6.OSTSTF flag and the ICSR6.OSTSTE bit are set to 1 while the POECR2.MTU6BDZE bit is 1.

(5) MTU7 pins (MTIOC7A, MTIOC7C)

When one of the following conditions is satisfied, the pins are placed in high-impedance state.

- Operation for detection of the POE4# input level

  When the OCSR2.OCE2 bit is set to 1 while the ICSR2.POE4F and OCSR2.OSF2 flags are 1.
- Operation for comparison of the output levels on the MTIOC7A and MTIOC7C pins

  When the OCSR2.OCF2 flag is set to 1 while the POECR2.MTU7ACZE bit is 1.
- SPOER setting

  When the SPOER.MTUCH67HIZ bit is set to 1 while the POECR2.MTU7ACZE bit is 1.
- Conditions added by POECR4

  When the ICSR1.POE0F flag is set to 1 while the POECR2.MTU7ACZE and POECR4.IC1ADDMT67ZE bits are 1.

  When the ICSR3.POE8F flag and the ICSR3.POE8E bit are set to 1 while the POECR2.MTU7ACZE and POECR4.IC3ADDMT67ZE bits are 1.

  When the ICSR4.POE10F flag and the ICSR4.POE10E bit are set to 1 while the POECR2.MTU7ACZE and POECR4.IC4ADDMT67ZE bits are 1.

  When the ICSR5.POE11F flag and the ICSR5.POE11E bit are set to 1 while the POECR2.MTU7ACZE and POECR4.IC5ADDMT67ZE bits are 1.
- Detection of stopped oscillation

  When the ICSR6.OSTSTF flag and the ICSR6.OSTSTE bit are set to 1 while the POECR2.MTU7ACZE bit is 1.

(6) MTU7 pins (MTIOC7B, MTIOC7D)

When one of the following conditions is satisfied, the pins are placed in high-impedance state.

・Operation for detection of the POE4# input level

When the OCSR2.OCE2 bit is set to 1 while the ICSR2.POE4F and OCSR2.OSF2 flags are 1.

・Operation for comparison of the output levels on the MTIOC7B and MTIOC7D pins

When the OCSR2.OSF2 flag is set to 1 while the POECR2.MTU7BDZE bit is 1.

・SPOER setting

When the SPOER.MTUCH67HIZ bit is set to 1 while the POECR2.MTU7BDZE bit is 1.

・Conditions added by POECR4

When the ICSR1.POE0F flag is set to 1 while the POECR2.MTU7BDZE and POECR4.IC1ADDMT67ZE bits are 1.

When the ICSR3.POE8F flag and the ICSR3.POE8E bit are set to 1 while the POECR2.MTU7BDZE and POECR4.IC3ADDMT67ZE bits are 1.

When the ICSR4.POE10F flag and the ICSR4.POE10E bit are set to 1 while the POECR2.MTU7BDZE and POECR4.IC4ADDMT67ZE bits are 1.

When the ICSR5.POE11F flag and the ICSR5.POE11E bit are set to 1 while the POECR2.MTU7BDZE and POECR4.IC5ADDMT67ZE bits are 1.

・Detection of stopped oscillation

When the ICSR6.OSTSTF flag and the ICSR6.OSTSTE bit are set to 1 while the POECR2.MTU7BDZE bit is 1.

(7) MTU0 pin (MTIOC0A)

When one of the following conditions is satisfied, the pins are placed in high-impedance state.

・Operation for detection of the POE8# input level

When the ICSR3.POE8E bit is set to 1 while the ICSR3.POE8F flag is 1.

・SPOER setting

When the SPOER.MTUCH0HIZ bit is set to 1 while the POECR1.MTU0AZE bit is 1.

・Conditions added by POECR5

When the ICSR1.POE0F flag is set to 1 while the POECR1.MTU0AZE and POECR5.IC1ADDMT0ZE bits are 1.

When the ICSR2.POE4F flag is set to 1 while the POECR1.MTU0AZE and POECR5.IC2ADDMT0ZE bits are 1.

When the ICSR4.POE10F flag and the ICSR4.POE10E bit are set to 1 while the POECR1.MTU0AZE and POECR5.IC4ADDMT0ZE bits are 1.

When the ICSR5.POE11F flag and the ICSR5.POE11E bit are set to 1 while the POECR1.MTU0AZE and POECR5.IC5ADDMT0ZE bits are 1.

・Detection of stopped oscillation

When the ICSR6.OSTSTF flag and the ICSR6.OSTSTE bit are set to 1 while the POECR1.MTU0AZE bit is 1.

(8) MTU0 pin (MTIOC0B)

When one of the following conditions is satisfied, the pins are placed in high-impedance state.

・Operation for detection of the POE8# input level

When the ICSR3.POE8E bit is set to 1 while the ICSR3.POE8F flag is 1.

・SPOER setting

When the SPOER.MTUCH0HIZ bit is set to 1 while the POECR1.MTU0BZE bit is 1.

・Conditions added by POECR5

When the ICSR1.POE0F flag is set to 1 while the POECR1.MTU0BZE and POECR5.IC1ADDMT0ZE bits are 1.

When the ICSR2.POE4F flag is set to 1 while the POECR1.MTU0BZE and POECR5.IC2ADDMT0ZE bits are 1.

When the ICSR4.POE10F flag and the ICSR4.POE10E bit are set to 1 while the POECR1.MTU0BZE and POECR5.IC4ADDMT0ZE bits are 1.

When the ICSR5.POE11F flag and the ICSR5.POE11E bit are set to 1 while the POECR1.MTU0BZE and POECR5.IC5ADDMT0ZE bits are 1.

・Detection of stopped oscillation

When the ICSR6.OSTSTF flag and the ICSR6.OSTSTE bit are set to 1 while the POECR1.MTU0BZE bit is 1.

(9) MTU0 pin (MTIOC0C)

When one of the following conditions is satisfied, the pins are placed in high-impedance state.

・Operation for detection of the POE8# input level

When the ICSR3.POE8E bit is set to 1 while the ICSR3.POE8F flag is 1.

・SPOER setting

When the SPOER.MTUCH0HIZ bit is set to 1 while the POECR1.MTU0CZE bit is 1.

・Conditions added by POECR5

When the ICSR1.POE0F flag is set to 1 while the POECR1.MTU0CZE and POECR5.IC1ADDMT0ZE bits are 1.

When the ICSR2.POE4F flag is set to 1 while the POECR1.MTU0CZE and POECR5.IC2ADDMT0ZE bits are 1.

When the ICSR4.POE10F flag and the ICSR4.POE10E bit are set to 1 while the POECR1.MTU0CZE and POECR5.IC4ADDMT0ZE bits are 1.

When the ICSR5.POE11F flag and the ICSR5.POE11E bit are set to 1 while the POECR1.MTU0CZE and POECR5.IC5ADDMT0ZE bits are 1.

・Detection of stopped oscillation

When the ICSR6.OSTSTF flag and the ICSR6.OSTSTE bit are set to 1 while the POECR1.MTU0CZE bit is 1.

(10) MTU0 pin (MTIOC0D)

When one of the following conditions is satisfied, the pins are placed in high-impedance state.

・Operation for detection of the POE8# input level

When the ICSR3.POE8E bit is set to 1 while the ICSR3.POE8F flag is 1.

・SPOER setting

When the SPOER.MTUCH0HIZ bit is set to 1 while the POECR1.MTU0DZE bit is 1.

・Conditions added by POECR5

When the ICSR1.POE0F flag is set to 1 while the POECR1.MTU0DZE and POECR5.IC1ADDMT0ZE bits are 1.

When the ICSR2.POE4F flag is set to 1 while the POECR1.MTU0DZE and POECR5.IC2ADDMT0ZE bits are 1.

When the ICSR4.POE10F flag and the ICSR4.POE10E bit are set to 1 while the POECR1.MTU0DZE and POECR5.IC4ADDMT0ZE bits are 1.

When the ICSR5.POE11F flag and the ICSR5.POE11E bit are set to 1 while the POECR1.MTU0DZE and POECR5.IC5ADDMT0ZE bits are 1.

・Detection of stopped oscillation

When the ICSR6.OSTSTF flag and the ICSR6.OSTSTE bit are set to 1 while the POECR1.MTU0DZE bit is 1.

(11) GPT0 pins (GTIOC0A, GTIOC0B)

When one of the following conditions is satisfied, the pins are placed in high-impedance state.

・Operation for detection of the POE10# input level

When the ICSR4.POE10E bit is set to 1 while the ICSR4.POE10F flag is 1.

・SPOER setting

When the SPOER.GPT01HIZ bit is set to 1 while the POECR3.GPT0ABZE bit is 1.

・Conditions added by POECR6

When the ICSR1.POE0F flag is set to 1 while the POECR3.GPT0ABZE and POECR6.IC1ADDGPT01ZE bits are 1.

When the ICSR2.POE4F flag is set to 1 while the POECR3.GPT0ABZE and POECR6.IC2ADDGPT01ZE bits are 1.

When the ICSR3.POE8F flag and the ICSR3.POE8E bit are set to 1 while the POECR3.GPT0ABZE and POECR6.IC3ADDGPT01ZE bits are 1.

When the ICSR5.POE11F flag and the ICSR5.POE11E bit are set to 1 while the POECR3.GPT0ABZE and POECR6.IC5ADDGPT01ZE bits are 1.

・Detection of stopped oscillation

When the ICSR6.OSTSTF flag and the ICSR6.OSTSTE bit are set to 1 while the POECR3.GPT0ABZE bit is 1.

(12) GPT1 pins (GTIOC1A, GTIOC1B)

When one of the following conditions is satisfied, the pins are placed in high-impedance state.

・Operation for detection of the POE10# input level

When the ICSR4.POE10E bit is set to 1 while the ICSR4.POE10F flag is 1.

・SPOER setting

When the SPOER.GPT01HIZ bit is set to 1 while the POECR3.GPT1ABZE bit is 1.

・Conditions added by POECR6

When the ICSR1.POE0F flag is set to 1 while the POECR3.GPT1ABZE and POECR6.IC1ADDGPT01ZE bits are 1.

When the ICSR2.POE4F flag is set to 1 while the POECR3.GPT1ABZE and POECR6.IC2ADDGPT01ZE bits are 1.

When the ICSR3.POE8F flag and the ICSR3.POE8E bit are set to 1 while the POECR3.GPT1ABZE and POECR6.IC3ADDGPT01ZE bits are 1.

When the ICSR5.POE11F flag and the ICSR5.POE11E bit are set to 1 while the POECR3.GPT1ABZE and POECR6.IC5ADDGPT01ZE bits are 1.

・Detection of stopped oscillation

When the ICSR6.OSTSTF flag and the ICSR6.OSTSTE bit are set to 1 while the POECR3.GPT1ABZE bit is 1.

(13) GPT2 pins (GTIOC2A, GTIOC2B)

When one of the following conditions is satisfied, the pins are placed in high-impedance state.

・Operation for detection of the POE11# input level

When the ICSR5.POE11E bit is set to 1 while the ICSR5.POE11F flag is 1.

・SPOER setting

When the SPOER.GPT23HIZ bit is set to 1 while the POECR3.GPT2ABZE bit is 1.

・Conditions added by POECR6

When the ICSR1.POE0F flag is set to 1 while the POECR3.GPT2ABZE and POECR6.IC1ADDGPT23ZE bits are 1.

When the ICSR2.POE4F flag is set to 1 while the POECR3.GPT2ABZE and POECR6.IC2ADDGPT23ZE bits are 1.

When the ICSR3.POE8F flag and the ICSR3.POE8E bit are set to 1 while the POECR3.GPT2ABZE and POECR6.IC3ADDGPT23ZE bits are 1.

When the ICSR4.POE10F flag and the ICSR4.POE10E bit are set to 1 while the POECR3.GPT2ABZE and POECR6.IC4ADDGPT23ZE bits are 1.

・Detection of stopped oscillation

When the ICSR6.OSTSTF flag and the ICSR6.OSTSTE bit are set to 1 while the POECR3.GPT2ABZE bit is 1.

(14) GPT3 pins (GTIOC3A, GTIOC3B)

When one of the following conditions is satisfied, the pins are placed in high-impedance state.

・Operation for detection of the POE11# input level

When the ICSR5.POE11E bit is set to 1 while the ICSR5.POE11F flag is 1.

・SPOER setting

When the SPOER.GPT23HIZ bit is set to 1 while the POECR3.GPT3ABZE bit is 1.

・Conditions added by POECR6

When the ICSR1.POE0F flag is set to 1 while the POECR3.GPT3ABZE and POECR6.IC1ADDGPT23ZE bits are 1.

When the ICSR2.POE4F flag is set to 1 while the POECR3.GPT3ABZE and POECR6.IC2ADDGPT23ZE bits are 1.

When the ICSR3.POE8F flag and the ICSR3.POE8E bit are set to 1 while the POECR3.GPT3ABZE and POECR6.IC3ADDGPT23ZE bits are 1.

When the ICSR4.POE10F flag and the ICSR4.POE10E bit are set to 1 while the POECR3.GPT3ABZE and POECR6.IC4ADDGPT23ZE bits are 1.

・Detection of stopped oscillation

When the ICSR6.OSTSTF flag and the ICSR6.OSTSTE bit are set to 1 while the POECR3.GPT3ABZE bit is 1.

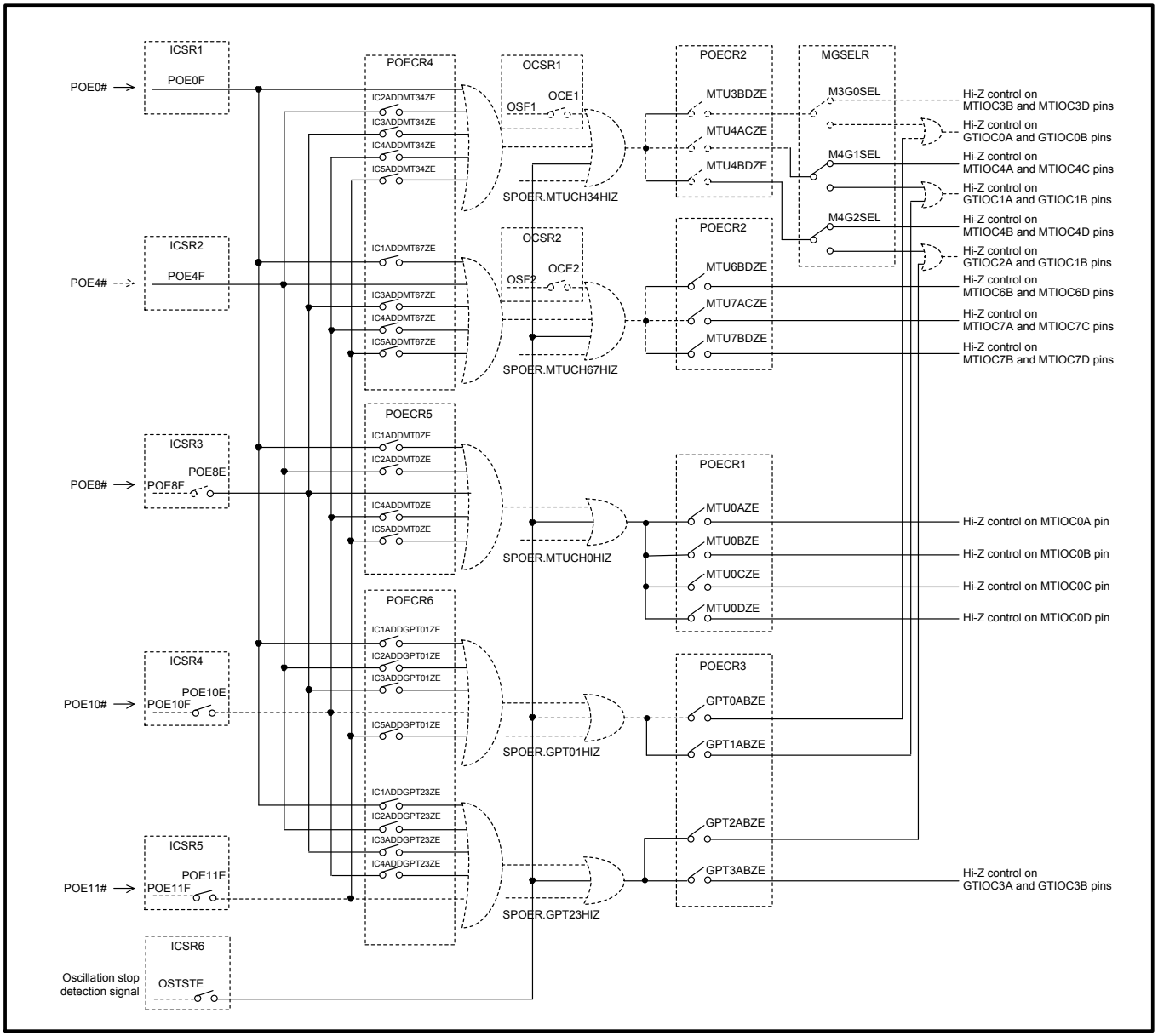

Figure 25.2 Target Pins and Conditions for High-Impedance Control

【After】

25.3 Operation

The following shows the target pins and conditions for high-impedance control.

(1) MTU3 pins or GPT0 pins*1 (MTIOC3B/GTIOC0A, MTIOC3D/GTIOC0B)

When one of the following conditions is satisfied while the POECR2.MTU3BDZE bit is 1, the pins become high-impedance.

- Operation for detection of the POE0# input level

  When the ICSR1.POE0F flag becomes 1.

- Operation for comparison of the output levels on the MTIOC3B and MTIOC3D or GTIOC0A and GTIOC0B pins

  When the OCSR1.OSF1 flag becomes 1 while the OCSR1.OCE1 bit is 1.

- SPOER setting

  When the SPOER.MTUCH34HIZ bit is set to 1.

- Conditions added by POECR4

  When the ICSR2.POE4F flag becomes 1 while the POECR4.IC2ADDMT34ZE bit is 1.

  When the ICSR3.POE8F flag becomes 1 while the POECR4.IC3ADDMT34ZE bit and the ICSR3.POE8E bit are 1.

  When the ICSR4.POE10F flag becomes 1 while the POECR4.IC4ADDMT34ZE bit and the ICSR4.POE10E bit are 1.

  When the ICSR5.POE11F flag becomes 1 while the POECR4.IC5ADDMT34ZE bit and the ICSR5.POE11E bit are 1.

- Detection of oscillation stop

  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

Note 1. The pins selected in the MGSELR.M3G0SEL bit are for the control.

(2) MTU4 pins or GPT1 pins*1 (MTIOC4A/GTIOC1A, MTIOC4C/GTIOC1B)

When one of the following conditions is satisfied while the POECR2.MTU4ACZE bit is 1, the pins become high-impedance.

- Operation for detection of the POE0# input level

  When the ICSR1.POE0F flag becomes 1.

- Operation for comparison of the output levels on the MTIOC4A and MTIOC4C or GTIOC1A and GTIOC1B pins

  When the OCSR1.OSF1 flag becomes 1 while the OCSR1.OCE1 bit is 1.

- SPOER setting

  When the SPOER.MTUCH34HIZ bit is set to 1.

- Conditions added by POECR4

  When the ICSR2.POE4F flag becomes 1 while the POECR4.IC2ADDMT34ZE bit is 1.

  When the ICSR3.POE8F flag becomes 1 while the POECR4.IC3ADDMT34ZE bit and the ICSR3.POE8E bit are 1.

  When the ICSR4.POE10F flag becomes 1 while the POECR4.IC4ADDMT34ZE bit and the ICSR4.POE10E bit are 1.

  When the ICSR5.POE11F flag becomes 1 while the POECR4.IC5ADDMT34ZE bit and the ICSR5.POE11E bit are 1.

- Detection of oscillation stop

  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

Note 1. The pins selected in the MGSELR.M4G1SEL bit are for the control.

(3) MTU4 pins or GPT2 pins*1 (MTIOC4B/GTIOC2A, MTIOC4D/GTIOC2B)

When one of the following conditions is satisfied while the POECR2.MTU4BDZE bit is 1, the pins become high-impedance.

- Operation for detection of the POE0# input level

  When the ICSR1.POE0F flag becomes 1.

- Operation for comparison of the output levels on the MTIOC4B and MTIOC4D or GTIOC2A and GTIOC2B pins

  When the OCSR1.OSF1 flag becomes 1 while the OCSR1.OCE1 bit is 1.

- SPOER setting

  When the SPOER.MTUCH34HIZ bit is set to 1.

- Conditions added by POECR4

  When the ICSR2.POE4F flag becomes 1 while the POECR4.IC2ADDMT34ZE bit is 1.

  When the ICSR3.POE8F flag becomes 1 while the POECR4.IC3ADDMT34ZE bit and the ICSR3.POE8E bit are 1.

  When the ICSR4.POE10F flag becomes 1 while the POECR4.IC4ADDMT34ZE bit and the ICSR4.POE10E bit are 1.

  When the ICSR5.POE11F flag becomes 1 while the POECR4.IC5ADDMT34ZE bit and the ICSR5.POE11E bit are 1.

- Detection of oscillation stop

  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

Note 1. The pins selected in the MGSELR.M4G2SEL bit are for the control.

(4) MTU6 pins (MTIOC6B, MTIOC6D)

When one of the following conditions is satisfied while the POECR2.MTU6BDZE bit is 1, the pins become high-impedance.

- Operation for detection of the POE4# input level

  When the ICSR2.POE4F flag becomes 1.

- Operation for comparison of the output levels on the MTIOC6B and MTIOC6D pins

  When the OCSR2.OSF2 flag becomes 1 while the OCSR2.OCE2 bit is 1.

- SPOER setting

  When the SPOER.MTUCH67HIZ bit is set to 1.

- Conditions added by POECR4

  When the ICSR1.POE0F flag becomes 1 while the POECR4.IC1ADDMT67ZE bit is 1.

  When the ICSR3.POE8F flag becomes 1 while the POECR4.IC3ADDMT67ZE bit and the ICSR3.POE8E bit are 1.

  When the ICSR4.POE10F flag becomes 1 while the POECR4.IC4ADDMT67ZE bit and the ICSR4.POE10E bit are 1.

  When the ICSR5.POE11F flag becomes 1 while the POECR4.IC5ADDMT67ZE bit and the ICSR5.POE11E bit are 1.

- Detection of oscillation stop

  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(5) MTU7 pins (MTIOC7A, MTIOC7C)

When one of the following conditions is satisfied while the POECR2.MTU7ACZE bit is 1, the pins become high-impedance.

- Operation for detection of the POE4# input level

  When the ICSR2.POE4F flag becomes 1.

- Operation for comparison of the output levels on the MTIOC7A and MTIOC7C pins

  When the OCSR2.OSF2 flag becomes 1 while the OCSR2.OCE2 bit is 1.

- SPOER setting

  When the SPOER.MTUCH67HIZ bit is set to 1.

- Conditions added by POECR4

  When the ICSR1.POE0F flag becomes 1 while the POECR4.IC1ADDMT67ZE bit is 1.

  When the ICSR3.POE8F flag becomes 1 while the POECR4.IC3ADDMT67ZE bit and the ICSR3.POE8E bit are 1.

  When the ICSR4.POE10F flag becomes 1 while the POECR4.IC4ADDMT67ZE bit and the ICSR4.POE10E bit are 1.

  When the ICSR5.POE11F flag becomes 1 while the POECR4.IC5ADDMT67ZE bit and the ICSR5.POE11E bit are 1.

- Detection of oscillation stop

  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(6) MTU7 pins (MTIOC7B, MTIOC7D)

When one of the following conditions is satisfied while the POECR2.MTU7BDZE bit is 1, the pins become high-impedance.

- Operation for detection of the POE4# input level

  When the ICSR2.POE4F flag becomes 1.

- Operation for comparison of the output levels on the MTIOC7B and MTIOC7D pins

  When the OCSR2.OSF2 flag becomes 1 while the OCSR2.OCE2 bit is 1.

- SPOER setting

  When the SPOER.MTUCH67HIZ bit is set to 1.

- Conditions added by POECR4

  When the ICSR1.POE0F flag becomes 1 while the POECR4.IC1ADDMT67ZE bit is 1.

  When the ICSR3.POE8F flag becomes 1 while the POECR4.IC3ADDMT67ZE bit and the ICSR3.POE8E bit are 1.

  When the ICSR4.POE10F flag becomes 1 while the POECR4.IC4ADDMT67ZE bit and the ICSR4.POE10E bit are 1.

  When the ICSR5.POE11F flag becomes 1 while the POECR4.IC5ADDMT67ZE bit and the ICSR5.POE11E bit are 1.

- Detection of oscillation stop

  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(7) MTU0 pin (MTIOC0A)

When one of the following conditions is satisfied while the POECR1.MTU0AZE bit is 1, the pin becomes high-impedance.

- Operation for detection of the POE8# input level

  When the ICSR3.POE8F flag becomes 1 while the ICSR3.POE8E bit is 1.

- SPOER setting

  When the SPOER.MTUCH0HIZ bit is set to 1.

・Conditions added by POECR5

When the ICSR1.POE0F flag becomes 1 while the POECR5.IC1ADDMT0ZE bit is 1.

When the ICSR2.POE4F flag becomes 1 while the POECR5.IC2ADDMT0ZE bit is 1.

When the ICSR4.POE10F flag becomes 1 while the POECR5.IC4ADDMT0ZE bit and the ICSR4.POE10E bit are 1.

When the ICSR5.POE11F flag becomes 1 while the POECR5.IC5ADDMT0ZE bit and the ICSR5.POE11E bit are 1.

・Detection of oscillation stop

When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(8) MTU0 pin (MTIOC0B)

When one of the following conditions is satisfied while the POECR1.MTU0BZE bit is 1, the pin becomes high-impedance.

・Operation for detection of the POE8# input level

When the ICSR3.POE8F flag becomes 1 while the ICSR3.POE8E bit is 1.

・SPOER setting

When the SPOER.MTUCH0HIZ bit is set to 1.

・Conditions added by POECR5

When the ICSR1.POE0F flag becomes 1 while the POECR5.IC1ADDMT0ZE bit is 1.

When the ICSR2.POE4F flag becomes 1 while the POECR5.IC2ADDMT0ZE bit is 1.

When the ICSR4.POE10F flag becomes 1 while the POECR5.IC4ADDMT0ZE bit and the ICSR4.POE10E bit are 1.

When the ICSR5.POE11F flag becomes 1 while the POECR5.IC5ADDMT0ZE bit and the ICSR5.POE11E bit are 1.

・Detection of oscillation stop

When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(9) MTU0 pin (MTIOC0C)

When one of the following conditions is satisfied while the POECR1.MTU0CZE bit is 1, the pin becomes high-impedance.

・Operation for detection of the POE8# input level

When the ICSR3.POE8F flag becomes 1 while the ICSR3.POE8E bit is 1.

・SPOER setting

When the SPOER.MTUCH0HIZ bit is set to 1.

・Conditions added by POECR5

When the ICSR1.POE0F flag becomes 1 while the POECR5.IC1ADDMT0ZE bit is 1.

When the ICSR2.POE4F flag becomes 1 while the POECR5.IC2ADDMT0ZE bit is 1.

When the ICSR4.POE10F flag becomes 1 while the POECR5.IC4ADDMT0ZE bit and the ICSR4.POE10E bit are 1.

When the ICSR5.POE11F flag becomes 1 while the POECR5.IC5ADDMT0ZE bit and the ICSR5.POE11E bit are 1.

・Detection of oscillation stop

When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(10) MTU0 pin (MTIOC0D)

When one of the following conditions is satisfied while the POECR1.MTU0DZE bit is 1, the pin becomes high-impedance.

- Operation for detection of the POE8# input level

  When the ICSR3.POE8F flag becomes 1 while the ICSR3.POE8E bit is 1.

- SPOER setting

  When the SPOER.MTUCH0HIZ bit is set to 1.

- Conditions added by POECR5

  When the ICSR1.POE0F flag becomes 1 while the POECR5.IC1ADDMT0ZE bit is 1.

  When the ICSR2.POE4F flag becomes 1 while the POECR5.IC2ADDMT0ZE bit is 1.

  When the ICSR4.POE10F flag becomes 1 while the POECR5.IC4ADDMT0ZE bit and the ICSR4.POE10E bit are 1.

  When the ICSR5.POE11F flag becomes 1 while the POECR5.IC5ADDMT0ZE bit and the ICSR5.POE11E bit are 1.

- Detection of oscillation stop

  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(11) GPT0 pins (GTIOC0A, GTIOC0B)

When one of the following conditions is satisfied while the POECR3.GPT0ABZE bit is 1, the pins become high-impedance.

- Operation for detection of the POE10# input level

  When the ICSR4.POE10F flag becomes 1 while the ICSR4.POE10E bit is 1.

- SPOER setting

  When the SPOER.GPT01HIZ bit is set to 1.

- Conditions added by POECR6

  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT01ZE bit is 1.

  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT01ZE bit is 1.

  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT01ZE bit and the ICSR3.POE8E bit are 1.

  When the ICSR5.POE11F flag becomes 1 while the POECR6.IC5ADDGPT01ZE bit and the ICSR5.POE11E bit are 1.

- Detection of oscillation stop

  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(12) GPT1 pins (GTIOC1A, GTIOC1B)

When one of the following conditions is satisfied while the POECR3.GPT1ABZE bit is 1, the pins become high-impedance.

- Operation for detection of the POE10# input level

  When the ICSR4.POE10F flag becomes 1 while the ICSR4.POE10E bit is 1.

- SPOER setting

  When the SPOER.GPT01HIZ bit is set to 1.

- Conditions added by POECR6

  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT01ZE bit is 1.

  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT01ZE bit is 1.

  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT01ZE bit and the ICSR3.POE8E bit are 1.

  When the ICSR5.POE11F flag becomes 1 while the POECR6.IC5ADDGPT01ZE bit and the ICSR5.POE11E bit are 1.

- Detection of oscillation stop

When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(13) GPT2 pins (GTIOC2A, GTIOC2B)

When one of the following conditions is satisfied while the POECR3.GPT2ABZE bit is 1, the pins become high-impedance.

- Operation for detection of the POE11# input level

  When the ICSR5.POE11F flag becomes 1 while the ICSR5.POE11E bit is 1.

- SPOER setting

  When the SPOER.GPT23HIZ bit is set to 1.

- Conditions added by POECR6

  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT23ZE bit is 1.

  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT23ZE bit is 1.

  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT23ZE bit and the ICSR3.POE8E bit are 1.

  When the ICSR4.POE10F flag becomes 1 while the POECR6.IC4ADDGPT23ZE bit and the ICSR4.POE10E bit are 1.

- Detection of oscillation stop

  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

(14) GPT3 pins (GTIOC3A, GTIOC3B)

When one of the following conditions is satisfied while the POECR3.GPT3ABZE bit is 1, the pins become high-impedance.

- Operation for detection of the POE11# input level

  When the ICSR5.POE11F flag becomes 1 while the ICSR5.POE11E bit is 1.

- SPOER setting

  When the SPOER.GPT23HIZ bit is set to 1.

- Conditions added by POECR6

  When the ICSR1.POE0F flag becomes 1 while the POECR6.IC1ADDGPT23ZE bit is 1.

  When the ICSR2.POE4F flag becomes 1 while the POECR6.IC2ADDGPT23ZE bit is 1.

  When the ICSR3.POE8F flag becomes 1 while the POECR6.IC3ADDGPT23ZE bit and the ICSR3.POE8E bit are 1.

  When the ICSR4.POE10F flag becomes 1 while the POECR6.IC4ADDGPT23ZE bit and the ICSR4.POE10E bit are 1.

- Detection of oscillation stop

  When the ICSR6.OSTSTF flag becomes 1 while the ICSR6.OSTSTE bit is 1.

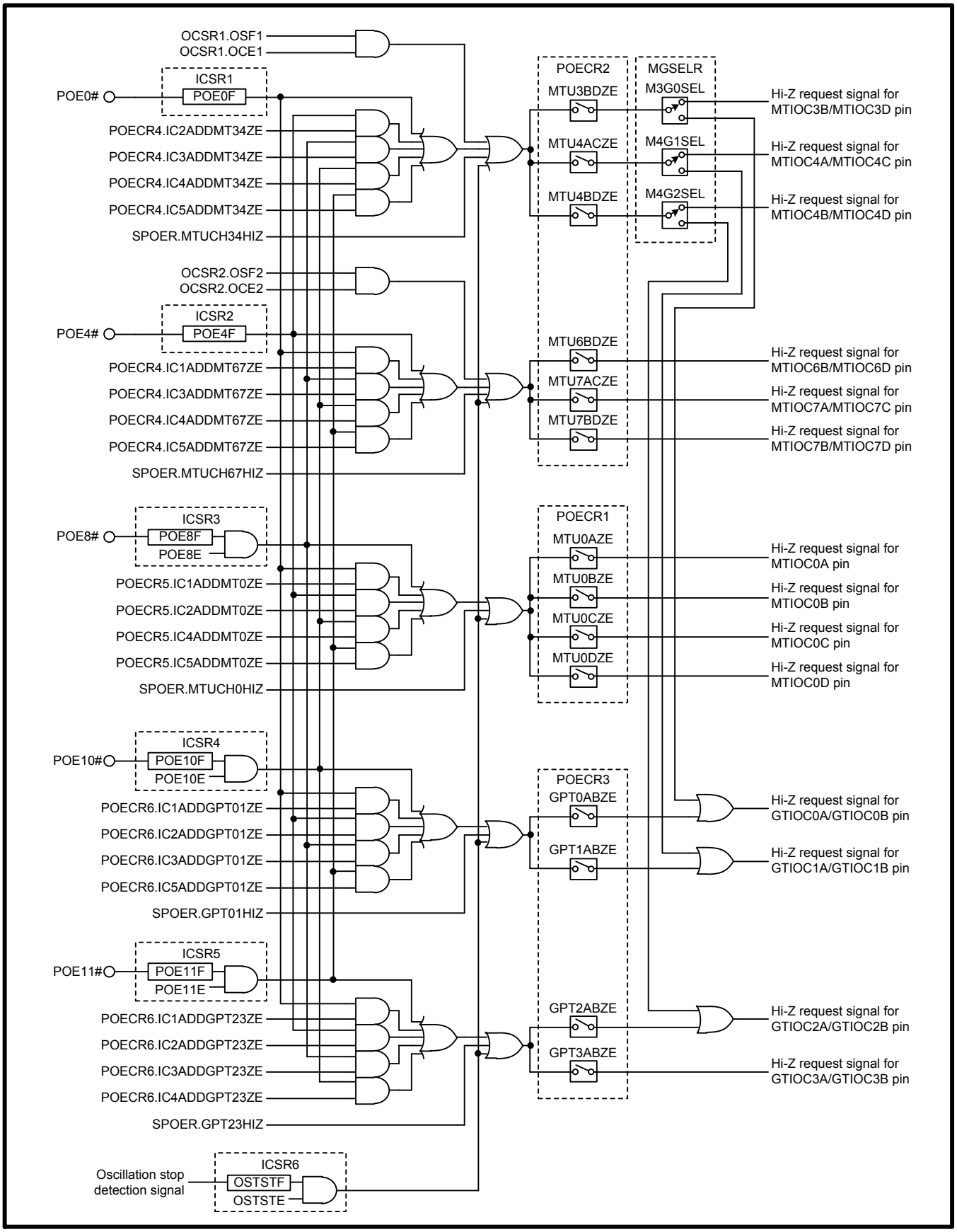

Figure 25.2 Target Pins and Conditions for High-Impedance Control

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