RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU	Document No.	TN-RL*-A0114A/E	Rev.	1.00	
Title	Correction for Incorrect Description Notice RI Descriptions in the User's Manual: Hardware Changed	Information Category	Technical Notification			
		Lot No.				
Applicable Product	RL78/G14 Group	Reference Document	Rev 3 40			

This document describes misstatements found in the RL78/G14 User's Manual: Hardware Rev. 3.40 (R01UH0186EJ0340).

Corrections

Applicable Item	Applicable Page	Contents
10.3.4 Real-time clock control register 1 (RTCC1)	Page 561	Incorrect descriptions revised
Figure 10 - 22. Procedure for Reading Real-time Clock	Page 573	Incorrect descriptions revised
Figure 10 - 23. Procedure for Writing Real-time Clock	Page 574	Incorrect descriptions revised
34.3.2 Supply current characteristics	Page 1171 to Page 1182	Incorrect descriptions revised
35.3.2 Supply current characteristics	Page 1244 to Page 1255	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.



No.		Corrections and Applicable Items				
	Document No.		English	R01UH0186EJ0340	document for corrections	
1	10.3.4	Real-time clock con	trol register 1 (RTCC1)	Page 561	Page 3	
2	Figure Clock	10 - 22. Procedure	for Reading Real-time	Page 573	Page 4	
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4	34.3.2	Supply current char	acteristics	Page 1171 to Page 1182	Page 5 to Page 13	
5	35.3.2	Page 14 to Page 22				

Incorrect: Bold with underline: Correct: Gray hatched

Revision History

RL78/G14 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0114A/E	Jan. 20, 2023	First edition issued
		Corrections No.1 to No.5 revised (this document)



1. 10.3.4 Real-time clock control register 1 (RTCC1) (Page 561)

Incorrect:

Figure 10 - 6. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)

RIFG	Constant-period interrupt status flag						
0	xed-cycle interrupt is not generated.						
1	ixed-cycle interrupt is generated.						
generated, it is	tes the status of generation of the fixed-cycle interrupt. When the fixed-cycle interrupt is set to "1". ared when "0" is written to it. Writing "1" to it is invalid.						

RWST	Wait status flag of real-time clock				
0	Counter is operating.				
1	lode to read or write counter value				
	This status flag indicates whether the setting of the RWAIT bit is valid. Before reading or writing the counter value, confirm that the value of this flag is 1.				

RWAIT	Wait control of real-time clock						
0	Sets counter operation.						
1	Stops SEC to YEAR counters. Mode to read or write counter value						
This bit controls	s the operation of the counter.						
Be sure to write	e "1" to it to read or write the counter value.						
As the internal	counter (16-bit) is continuing to run, complete reading or writing within one second and turn						
back to 0.	back to 0.						
When RWAIT :	When RWAIT = 1, it takes up to one cycle of f_{RTC} until the counter value can be read or written (RWST = 1).						
When the inter	When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT =						
0, then counts	0, then counts up.						
However, when	However, when it wrote a value to second count register, it will not keep the overflow event.						

Correct:

Figure 10 - 6. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)

RIFG	Constant-period interrupt status flag				
0	0 Fixed-cycle interrupt is not generated.				
1 Fixed-cycle interrupt is generated.					
This flag indica generated, it is	ates the status of generation of the fixed-cycle interrupt. When the fixed-cycle interrupt is s set to "1".				
This flag is cleared when "0" is written to it. Writing "1" to it is invalid.					

RWST	Wait status flag of real-time clock				
0	Counter is operating.				
1	Mode to read or write counter value				
This status flag	This status flag indicates whether the setting of the RWAIT bit is valid.				

Before reading or writing the counter value, confirm that the value of this flag is 1.

RWAIT	Wait control of real-time clock						
0 Sets counter operation.							
1	Stops SEC to YEAR counters. Mode to read or write counter value						
This bit contro	Is the operation of the counter.						
Be sure to writ	e "1" to it to read or write the counter value.						
As the internal	counter (16-bit) is continuing to run, complete reading or writing within one second and turn						
back to 0. Whe	en reading or writing to the counter is required while generation of the alarm interrupt is enabled, first						
set the CT2 to 0	CT0 bits to 010B (generating the constant-period interrupt once per 1 second).						
Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.							
Constant-period interrupt. When RWAIT = 1, it takes up to one cycle of frac until the counter value can be read or written (RWST = 1 When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT							

0, then counts up.

However, when it wrote a value to second count register, it will not keep the overflow event.



2. Figure 10 - 22 Procedure for Reading Real-time Clock (Page 573)

Incorrect:

Note Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

Caution Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence. All the registers do not have to read and only some registers may be read.

3. Figure 10 - 23 Procedure for Writing Real-time Clock (Page 574)

Incorrect:

Note Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

- Cautions 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.
- Cautions 2. When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.
- Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence.

All the registers do not have to be set and only some registers may be written.

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Correct:

Note Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

Caution Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When reading to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence. All the registers do not have to read and only some registers may be read.

Correct:

Note Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

- Cautions 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.
- Cautions 2.When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.
- Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence.

All the registers do not have to be set and only some registers may be written.



4. 34.3.2 Supply current characteristics (Page 1171 to Page 1182)

Incorrect:

34.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

 $(T_A = -40 \text{ to } +85^\circ \text{ C}, 1.6 \text{ V} \le \text{EV}_{\text{DD0}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0 \text{ V}) (1/2)$

Parameter	Symbol		Conditions						MAX.	Unit
Supply	IDD1	Operating	HS (high-speed main)	fносо = 64 MHz,	Basic	VDD = 5.0 V		2.4		mA
current Note 1		mode	mode Note 5	fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.4		
Note 1				fносо = 32 MHz,	Basic	VDD = 5.0 V		2.1		
				fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.1		

		fsub = 32.768 kHz Note 4	Normal	Square wave input	4.8	7.5	
		TA = +70°C	operation	Resonator connection	4.8	7.5	
		fsue = 32.768 kHz Note 4	Normal	Square wave input	5.4	8.9]
		TA = +85°C	operation	Resonator connection	5.4	8.9	1

- Notes 1. Total current flowing into V_{DD} and EV_{DDD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DDD} or V_{SS}, EV_{SSD}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D. converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down. resistors and the current flowing during data flash rewrite.
- Notes 2. When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 3. When high-speed system clock and subsystem clock are stopped.
- Notes 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- **Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:	2.7 V \leq V_DD \leq 5.5 V@1 MHz to 32 MHz
	2.4 V \leq V _{DD} \leq 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode:	1.8 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode:	1.6 V \leq V _{DD} \leq 5.5 V@1 MHz to 4 MHz

- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remarks 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- **Remarks 3.** fin: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remarks 4. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remarks 5. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

Correct:

34.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

$(T_A = -40 \text{ to } +85^\circ \text{ C}, 1.6 \text{ V} \le \text{EV}_{DD0} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{V}_{SS} = \text{EV}_{SS0} = 0 \text{ V}) (1/2)$

Parameter	Symbol			Conditions			MIN.	TYP.	MAX.	Unit
Supply	IDD1	Operating	HS (high-speed main)	fносо = 64 MHz,	Basic	VDD = 5.0 V		2.4		mA
current		mode	mode Note 5	fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.4		
Note 1				fносо = 32 MHz,	Basic	VDD = 5.0 V		2.1		1
				fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.1		

		fsus = 32.768 kHz Note 4	Normal	Square wave input	4.8	7.5	
		TA = +70°C	operation	Resonator connection	4.8	7.5	
		fsue = 32.768 kHz Note 4	Normal	Square wave input	5.4	8.9	
		TA = +85°C	operation	Resonator connection	5.4	8.9	

 $T_{\rm rel}$ = $T_{\rm rel}$ =

Notes 1.	То	tal curre	ent flowing into V₀₀ an	d EV _{DD0} , including the input leakage current flowing when the level of						
	the	e input p	in is fixed to VDD, EV	or Vss, EVsso. The following points apply in the HS (high-speed						
	ma	ain), LS	(low-speed main), an	d LV (low-voltage main) modes.						
	• т	he curre	ents in the "TYP." col	umn do not include the operating currents of the peripheral modules.						
	• т	he curre	ents in the "MAX." col	lumn include the operating currents of the peripheral modules, except						
	1	for those	e flowing into the A/D	converter, LVD circuit, I/O port, and on-chip pull-up/pull-down						
	resistors, and those flowing while the data flash memory is being rewritten.									
	In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include									
	the	operati	ing currents of the pe	ripheral modules. However, in HALT mode, including the current						
	flo	wing inte	o the RTC.							
Notes 2.	Wh	en high	-speed on-chip oscilla	ator and subsystem clock are stopped.						
Notes 3.	Wh	ien high	-speed system clock	and subsystem clock are stopped.						
Notes 4.	Wh	en high	-speed on-chip oscill	ator and high-speed system clock are stopped. When AMPHS1 = 1						
	(U	tra-low	power consumption of	oscillation).						
Notes 5.	Re	lationsh	ip between operation	voltage width, operation frequency of CPU and operation mode is as						
	be	low.								
	HS	6 (high-s	peed main) mode:	2.7 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 32 MHz						
			. ,	$2.4 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}_{@}1 \text{ MHz to } 16 \text{ MHz}$						
	LS	(low-sp	eed main) mode:	$1.8 \text{ V} \le V_{DD} \le 5.5 \text{ V} @ 1 \text{ MHz to } 8 \text{ MHz}$						
	LV	(low-vo	ltage main) mode:	$1.6 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}_{\odot}$ 1 MHz to 4 MHz						
Domorko		£.	Link anod avatam	alask fraguenny (V1 alask conjilation fraguency or sytemal main						
Remarks	1.	IMX.	system clock freque	 clock frequency (X1 clock oscillation frequency or external main ency) 						
Remarks	2.	fносо:	High-speed on-chip	oscillator clock frequency (64 MHz max.)						
Remarks	3.	fн:	High-speed on-chip	oscillator clock frequency (32 MHz max.)						
Remarks	4.	fsue:	Subsystem clock fre	equency (XT1 clock oscillation frequency)						
Remarks	5.	Excep	t subsystem clock op	peration, temperature condition of the TYP. value is T_A = 25°C						



(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

$(T_A = -40 \text{ to } +85^\circ \text{ C}, 1.6 \text{ V} \le \text{EV}_{DD0} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{V}_{SS} = \text{EV}_{SS0} = 0 \text{ V})$ (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply current	IDD2	HALT mode	HS (high-speed main)	fHOCO = 64 MHz,	V _{DD} = 5.0 V		0.80	3.09	mA
Note 1	Note 2		mode Note Z	fin = 32 MHz Note 4	V _{DD} = 3.0 V		0.80	3.09	1
				fHOCO = 32 MHz,	VDD = 5.0 V		0.49	2.40	1
				fiH = 32 MHz Note 4	VDD = 3.0 V		0.49	2.40	1
				fносо = 48 MHz,	VDD = 5.0 V		0.62	2.40	1
				fiH = 24 MHz Note 4	VDD = 3.0 V		0.62	2.40	1
				fHOCO = 24 MHz,	VDD = 5.0 V		0.4	1.83	1
				fiH = 24 MHz Note 4	VDD = 3.0 V		0.4	1.83	1
				fHOCO = 16 MHz,	VDD = 5.0 V		0.37	1.38	1
				fiH = 16 MHz Note 4	VDD = 3.0 V		0.37	1.38	1
			LS (low-speed main)	fноco = 8 MHz,	VDD = 3.0 V		260	710	μA
			mode Note Z	fiH = 8 MHz Note 4	VDD = 2.0 V		260	710	1
			_ (· · · · · · · · · · · · · · · · · · ·	'	VDD = 3.0 V		420	700	μA
			mode Note Z	fiH = 4 MHz Note 4	VDD = 2.0 V		420	700	1
			HS (high-speed main) mode Note Z	fmx = 20 MHz Note 3,	Square wave input		0.28	1.55	m/
				V _{DD} = 5.0 V f _{MX} = 20 MHz ^{Note 3} ,	Resonator connection		0.40	1.74	
					Square wave input		0.28	1.55	
				VDD = 3.0 V	Resonator connection		0.40	1.74	1
				fmx = 10 MHz Note 3,	Square wave input		0.19	0.86	1
				VDD = 5.0 V	Resonator connection		0.25	0.93	1
				fmx = 10 MHz Note 3,	Square wave input		0.19	0.86	1
				VDD = 3.0 V	Resonator connection		0.25	0.93	1
			LS (low-speed main)	fmx = 8 MHz Note 3,	Square wave input		95	550	μA
			mode Note Z	VDD = 3.0 V	Resonator connection		140	590	1
				fmx = 8 MHz Note 3,	Square wave input		95	550	1
				VDD = 2.0 V	Resonator connection		140	590	1

_						
	IDD3	STOP mode	T _A = -40°C	0.18	0.51	μA
	Note 6	Note 8	T _A = +25°C	0.24	0.51	
			T _A = +50°C	0.29	1.10	
			T _A = +70°C	0.41	1.90	
			T _A = +85°C	0.90	3.30	

Notes 1. Total current flowing into VDD and EVDDO, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDDO or Vss, EVsso. The values below the MAX, column include the peripheral operation current. However, not including the current flowing into the A/D. converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

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(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

$(T_A = -40 \text{ to } +85^\circ \text{ C}, 1.6 \text{ V} \le \text{EV}_{\text{DD0}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0 \text{ V})$ (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply current	IDD2	HALT mode	HS (high-speed main)	fHoco = 64 MHz,	VDD = 5.0 V		0.80	3.09	mA
Note 1	Note 2		mode Note 6	fiH = 32 MHz Note 4	VDD = 3.0 V		0.80	3.09	1
				fHOCO = 32 MHz,	VDD = 5.0 V		0.49	2.40	1
				fiH = 32 MHz Note 4	VDD = 3.0 V		0.49	2.40	1
				fHOCO = 48 MHz,	VDD = 5.0 V		0.62	2.40	1
				fiH = 24 MHz Note 4	VDD = 3.0 V		0.62	2.40	1
				fHOCO = 24 MHz,	VDD = 5.0 V		0.4	1.83	1
				fiH = 24 MHz Note 4	VDD = 3.0 V		0.4	1.83	1
			fHOCO = 16 MHz,	VDD = 5.0 V		0.37	1.38	1	
			fiH = 16 MHz Note 4	VDD = 3.0 V		0.37	1.38	1	
			LS (low-speed main)	fноco = 8 MHz,	VDD = 3.0 V		260	710	μA
			mode Note 6	fiH = 8 MHz Note 4	VDD = 2.0 V		260	710	1
			LV (low-voltage main)	,	VDD = 3.0 V		420	700	μA
			mode Note 6	fiH = 4 MHz Note 4	VDD = 2.0 V		420	700	1
			HS (high-speed main) mode Note 6	f _{MX} = 20 MHz Note 3,	Square wave input		0.28	1.55	mA
				VDD = 5.0 V	Resonator connection		0.40	1.74	1
				f _{MX} = 20 MHz Note 3,	Square wave input		0.28	1.55	1
				VDD = 3.0 V	Resonator connection		0.40	1.74	1
				f _{MX} = 10 MHz Note 3,	Square wave input		0.19	0.86	1
				VDD = 5.0 V	Resonator connection		0.25	0.93	1
				f _{MX} = 10 MHz Note 3,	Square wave input		0.19	0.86	1
				VDD = 3.0 V	Resonator connection		0.25	0.93	1
			LS (low-speed main)	f _{MX} = 8 MHz Note 3,	Square wave input		95	550	μA
			mode Note 6	V _{DD} = 3.0 V	Resonator connection		140	590	1
				f _{MX} = 8 MHz Note 3,	Square wave input		95	550	1
				VDD = 2.0 V	Resonator connection		140	590	1

IDD3	-	T _A = -40°C	0.18	0.51	μA
	Note 7	T _A = +25°C	0.24	0.51	
		T _A = +50°C	0.29	1.10	
		T _A = +70°C	0.41	1.90	
		Ta = +85°C	0.90	3.30	

Notes 1. Total current flowing into VDD and EVDD, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.

• The currents in the "TYP." column do not include the operating currents of the peripheral modules.

• The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

In the STOP mode, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.



- Notes 2. During HALT instruction execution by flash memory.
- Notes 3. When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 4. When high-speed system clock and subsystem clock are stopped.
- Notes 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and, watchdog timer...

Notes 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Notes 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

 HS (high-speed main) mode:
 $2.7 \vee \leq V_{\infty} \leq 5.5 \vee @1$ MHz to 32 MHz

 $2.4 \vee \leq V_{DD} \leq 5.5 \vee @1$ MHz to 32 MHz

 LS (low-speed main) mode:

 LV (low-voltage main) mode:

 $1.6 \vee \leq V_{DD} \leq 5.5 \vee @1$ MHz to 4 MHz

- Notes.8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remarks 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remarks 3. fin: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remarks 4. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- **Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^{\circ}C$

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Notes 2.	During HA	LT instruction execut	ion by flash memory.						
Notes 3.	When high	n-speed on-chip oscill	lator and subsystem clock are stopped.						
Notes 4.	When high	n-speed system clock	and subsystem clock are stopped.						
Notes 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLP(and setting ultra-low current consumption (AMPHS1 = 1).									
Notes 6.		Relationship between operation voltage width, operation frequency of CPU and operation mode is as							
	HS (high-	speed main) mode:	2.7 V ≤ V _∞ ≤ 5.5 V@1 MHz to 32 MHz						
			2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz						
	LS (low-s	peed main) mode:	$1.8 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}_{@}1 \text{ MHz}$ to 8 MHz						
	LV (low-ve	oltage main) mode:	$1.6 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}_{@}1 \text{ MHz}$ to 4 MHz						
Notes 7.	Regarding mode.	the value for current	to operate the subsystem clock in STOP mode, refer to that in HALT						
Remarks	1. fмx:	High-speed system system	n clock frequency (X1 clock oscillation frequency or external main ency)						
Remarks	2. fносо:	High-speed on-chip	o oscillator clock frequency (64 MHz max.)						
Remarks	3. f⊮:	High-speed on-chip	oscillator clock frequency (32 MHz max.)						
Remarks	4. fsuв:	Subsystem clock fre	equency (XT1 clock oscillation frequency)						
Remarks	5. Except	subsystem clock ope	eration and STOP mode, temperature condition of the TYP. value is $T_A =$						
	25°0	0							



(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

$(T_A = -40 \text{ to } +85^{\circ} \text{ C}, 1.6 \text{ V} \le \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0 \text{ V})$ (1/2)

Parameter	Symbol			Conditions			MIN.	TYP.	MAX.	Unit
Supply	IDD1	Operating	HS (high-speed main)	fносо = 64 MHz,	Basic	VDD = 5.0 V		2.6		mA
current Note 1		mode	mode Note 5	fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.6		1
Note 1				fносо = 32 MHz,	Basic	VDD = 5.0 V		2.3		1
				fin = 32 MHz Note 3	operation	VDD = 3.0 V		2.3		1

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			fsub = 32.768 kHz Note 4	Normal	Square wave input	5.5	10.5	I
			TA = +70°C	operation	Resonator connection	5.5	10.5	I
			fsue = 32.768 kHz Note 4		Square wave input	6.5	14.5	l
			TA = +85°C	operation	Resonator connection	6.5	14.5	l

- Notes 1. Total current flowing into V_{DD}, EV_{DDD}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current. flowing into the A/D converter. D/A converter, comparator, LVD circuit, I/O port, and on-chip. pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Notes 2. When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 3. When high-speed system clock and subsystem clock are stopped.
- Notes 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12bit interval timer and watchdog timer.
- **Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:	2.7 V \leq V _{DD} \leq 5.5 V@1 MHz to 32 MHz
	$2.4 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}$ @1 MHz to 16 MHz
LS (low-speed main) mode:	$1.8 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}$ @1 MHz to 8 MHz
LV (low-voltage main) mode:	$1.6 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}$ @1 MHz to 4 MHz

- **Remarks 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- **Remarks 2.** fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- **Remarks 3.** fin: High-speed on-chip oscillator clock frequency (32 MHz max.)
- **Remarks 4.** fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- **Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^{\circ}C$

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(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

$(T_A = -40 \text{ to } +85^\circ \text{ C}, 1.6 \text{ V} \le \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{ V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0 \text{ V})$ (1/2)

Parameter	Symbol	Conditions M							MAX.	Unit
Supply	IDD1	Operating	HS (high-speed main)	fносо = 64 MHz,	Basic	V _{DD} = 5.0 V		2.6		mA
current Note 1		mode	mode Note 5	fiH = 32 MHz Note 3	operation	V _{DD} = 3.0 V		2.6		1
					Basic	VDD = 5.0 V		2.3		-
					operation	V _{DD} = 3.0 V		2.3		
										1

fsus = 32.768 kHz Note 4 No		Square wave input	5.5	10.5	
TA = +70°C	operation	Resonator connection	5.5	10.5	
fsus = 32.768 kHz Note 4	Normal	Square wave input	6.5	14.5	
TA = +85°C	operation	Resonator connection	6.5	14.5	

Notes 1. Total current flowing into V_{DD}, EV_{DDD}, EV_{DDD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DDD}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.
 The currents in the "TYP." column do not include the operating currents of the peripheral modules.
 The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten. In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.

- Notes 2. When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 3. When high-speed system clock and subsystem clock are stopped.
- **Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).
- **Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:	2.7 V \leq V_DD \leq 5.5 V@1 MHz to 32 MHz
	2.4 V \leq V _{DD} \leq 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode:	1.8 V \leq V _{DD} \leq 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode:	1.6 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 4 MHz

- **Remarks 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remarks 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remarks 3. fin: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remarks 4. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- **Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^{\circ}C$



(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +85° C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, Vss = EVss0 = EVss1 = 0 V) (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply	IDD2	HALT mode	HS (high-speed main)	fHOCO = 64 MHz,	V _{DD} = 5.0 V		0.79	3.32	mA
current Note 1	Note 2		mode Note Z	fin = 32 MHz Note 4	VDD = 3.0 V		0.79	3.32	1
				fHOCO = 32 MHz,	VDD = 5.0 V		0.49	2.63	
				fin = 32 MHz Note 4	VDD = 3.0 V		0.49	2.63	
				fHOCO = 48 MHz,	VDD = 5.0 V		0.62	2.57	1
				fin = 24 MHz Note 4	V _{DD} = 3.0 V		0.62	2.57	Ī
				fносо = 24 MHz,	VDD = 5.0 V		0.4	2.00	
				fiH = 24 MHz Note 4	V _{DD} = 3.0 V		0.4	2.00	
				fHOCO = 16 MHz,	V _{DD} = 5.0 V		0.38	1.49	
				fin = 16 MHz Note 4	V _{DD} = 3.0 V		0.38	1.49	1
			LS (low-speed main)	fносо = 8 MHz,	VDD = 3.0 V		250	800	μA
			mode Note Z	fiH = 8 MHz Note 4	V _{DD} = 2.0 V		250	800	1
			LV (low-voltage main) mode <u>Note.Z</u>		V _{DD} = 3.0 V		420	755	μA
				fiH = 4 MHz Note 4	V _{DD} = 2.0 V		420	755	Î
			HS (high-speed main) mode <u>Note Z</u>	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.30	1.63	mA
					Resonator connection		0.40	1.85	
				fmx = 20 MHz Note 3,	Square wave input		0.30	1.63	
				VDD = 3.0 V	Resonator connection		0.40	1.85	
				f _{MX} = 10 MHz Note 3,	Square wave input		0.20	0.89	1
				VDD = 5.0 V	Resonator connection		0.25	0.97	1
				f _{MX} = 10 MHz Note 3,	Square wave input		0.20	0.89	1
				VDD = 3.0 V	Resonator connection		0.25	0.97	
			LS (low-speed main)	f _{MX} = 8 MHz Note 3,	Square wave input		110	580	μA
			mode Note Z	VDD = 3.0 V	Resonator connection		140	630	1
				f _{MX} = 8 MHz Note 3,	Square wave input		110	580	1
				VDD = 2.0 V	Resonator connection		140	630	1

_							
	IDD3		STOP mode	T _A = -40°C	0.19	0.57	μA
		Note.6	Note 8	T _A = +25°C	0.25	0.57	
				T _A = +50°C	0.33	2.26	
				T _A = +70°C	0.52	3.99	
				TA = +85°C	1.46	8.00	

- Notes 1. Total current flowing into V_{DD}, EV_{DDD}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip. pull-up/pull-down resistors and the current flowing during data flash rewrite.
- **Notes 2.** During HALT instruction execution by flash memory.

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(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +85° C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply	IDD2	HALT mode	HS (high-speed main)	fhoco = 64 MHz,	V _{DD} = 5.0 V		0.79	3.32	mA
current Note 1	Note 2		mode Note 6	fin = 32 MHz Note 4	V _{DD} = 3.0 V		0.79	3.32	
				fhoco = 32 MHz,	V _{DD} = 5.0 V		0.49	2.63	
				fin = 32 MHz Note 4	V _{DD} = 3.0 V		0.49	2.63	
				fhoco = 48 MHz,	V _{DD} = 5.0 V		0.62	2.57	
				fin = 24 MHz Note 4	VDD = 3.0 V		0.62	2.57	1
				fhoco = 24 MHz,	V _{DD} = 5.0 V		0.4	2.00	
				fiH = 24 MHz Note 4	V _{DD} = 3.0 V		0.4	2.00	
				fhoco = 16 MHz,	V _{DD} = 5.0 V		0.38	1.49	1
				fiH = 16 MHz Note 4	V _{DD} = 3.0 V		0.38	1.49	
			LS (low-speed main)		V _{DD} = 3.0 V		250	800	μA
			mode Note 6		V _{DD} = 2.0 V		250	800	
			LV (low-voltage main)	fHOCO = 4 MHz,	V _{DD} = 3.0 V		420	755	μA
			mode Note 6	fiH = 4 MHz Note 4	VDD = 2.0 V		420	755	
			HS (high-speed main) mode Note 6	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.30	1.63	mA
					Resonator connection		0.40	1.85	
				f _{MX} = 20 MHz Note 3,	Square wave input		0.30	1.63	
				V _{DD} = 3.0 V	Resonator connection		0.40	1.85	
				f _{MX} = 10 MHz Note 3,	Square wave input		0.20	0.89	
				VDD = 5.0 V	Resonator connection		0.25	0.97	
				fmx = 10 MHz Note 3,	Square wave input		0.20	0.89	
				VDD = 3.0 V	Resonator connection		0.25	0.97	1
			LS (low-speed main)	f _{MX} = 8 MHz Note 3,	Square wave input		110	580	μA
			mode Note 6	VDD = 3.0 V	Resonator connection		140	630	1
				f _{MX} = 8 MHz Note 3,	Square wave input		110	580	1
				VDD = 2.0 V	Resonator connection		140	630	1

IDD3	STOP mode	TA = -40°C	0.19	0.57	μA
	Note 7	T _A = +25°C	0.25	0.57	
		TA = +50°C	0.33	2.26	
		T _A = +70°C	0.52	3.99	
		Ta = +85°C	1.46	8.00	

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.

• The currents in the "TYP." column do not include the operating currents of the peripheral modules.

 The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and onchip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

In the STOP mode, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.

Notes 2. During HALT instruction execution by flash memory.



- Notes 3. When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 4. When high-speed system clock and subsystem clock are stopped.
- Notes 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer...

Notes 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Notes 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:	2.7 V \leq V _{DD} \leq 5.5 V@1 MHz to 32 MHz
	2.4 V \leq V _{DD} \leq 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode:	1.8 V \leq V _{DD} \leq 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode:	1.6 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 4 MHz

Notes.8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. fmx:	High-speed system clock frequency (X1 clock oscillation frequency or external main
	system clock frequency)

- Remarks 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remarks 3. fin: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remarks 4. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- **Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

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- **Notes 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 4. When high-speed system clock and subsystem clock are stopped.
- **Notes 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).
- Notes 6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:	$2.7 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}_{@}1 \text{ MHz}$ to 32 MHz
	2.4 V \leq V _{DD} \leq 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode:	1.8 V \leq V _{DD} \leq 5.5 V@1 MHz to 8 MHz

- LV (low-voltage main) mode: $1.6 \text{ V} \le V_{DD} \le 5.5 \text{ V}@1 \text{ MHz}$ to 4 MHz
- **Notes 7.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remarks 2. fH000: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remarks 3. fin: High-speed on-chip oscillator clock frequency (32 MHz max.)
- **Remarks 4.** fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remarks 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^{\circ}C$



(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

 $(T_A = -40 \text{ to } +85^{\circ} \text{ C}, 1.6 \text{ V} \le \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0 \text{ V})$ (1/2)

Parameter	Symbol		Conditions						MAX.	Unit
Supply	IDD1	Operating	HS (high-speed main)	fносо = 64 MHz,	Basic	V _{DD} = 5.0 V		2.9		mA
Current Note 1		mode	·····	fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.9		1
					Basic	VDD = 5.0 V	= 5.0 V 2.5		1	
					operation	VDD = 3.0 V		2.5		1
										1

-								
			fsub = 32.768 kHz Note 4		Square wave input	5.9	13.2	
			TA = +70°C	operation	Resonator connection	6.0	13.2	
			fsub = 32.768 kHz Note 4		Square wave input	6.8	17.5	
			TA = +85°C	operation	Resonator connection	6.9	17.5	

Notes 1. Total current flowing into VDD, EVDDD, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDDD, and EVDD1, or VSS, EVSSD, and EVSS1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip. pull-up/pull-down resistors and the current flowing during data flash rewrite.

Notes 2. When high-speed on-chip oscillator and subsystem clock are stopped.

- Notes 3. When high-speed system clock and subsystem clock are stopped.
- Notes 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- **Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:	2.7 V \leq V _{DD} \leq 5.5 V@1 MHz to 32 MHz
	2.4 V \leq V _{DD} \leq 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode:	1.8 V \leq V _{DD} \leq 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode:	1.6 V \leq V _{DD} \leq 5.5 V@1 MHz to 4 MHz

- Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remarks 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- **Remarks 3.** f_H: High-speed on-chip oscillator clock frequency (32 MHz max.)
- **Remarks 4.** fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- **Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^{\circ}C$

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(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

(TA = -40 to +85° C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (1/2)

Symbol			Conditions			MIN.	TYP.	MAX.	Unit
IDD1	Operating	HS (high-speed main)	fносо = 64 MHz,	Basic	VDD = 5.0 V		2.9		mA
	mode	mode Note 5	fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.9		1
			fносо = 32 MHz,	Basic	VDD = 5.0 V		2.5		1
			fin = 32 MHz Note 3	operation	VDD = 3.0 V		2.5		1
	IDD1		mode mode Note 5		mode mode Note 5 fH = 32 MHz Note 3 operation fH core = 32 MHz, Basic	mode mode Note 5 fill = 32 MHz Note 3 operation VDD = 3.0 V fhcore 32 MHz, Basic VDD = 5.0 V	mode mode Note 5 fH = 32 MHz Note 3 operation Von = 3.0 V fH core = 32 MHz, Basic Vbn = 5.0 V Vbn = 5.0 V Vbn = 5.0 V	mode mode Note 5 $\frac{1}{\text{fit} = 32 \text{ MHz}, \text{ Note 3}} \text{operation} \frac{1}{\text{V}_{\text{DD}} = 3.0 \text{ V}} 2.9$ $\frac{1}{\text{fit}_{\text{CO}} = 32 \text{ MHz}, \text{ Basic}} \text{V}_{\text{DD}} = 5.0 \text{ V} 2.5$	mode mode Note 5 fH = 32 MHz Note 3 operation VDD = 3.0 V 2.9 fHoco = 32 MHz, Basic VDD = 5.0 V 2.5

-		 1						1
			fsus = 32.768 kHz Note 4		Square wave input	5.9	13.2	
			TA = +70°C	operation	Resonator connection	6.0	13.2	
			fsus = 32.768 kHz Note 4	Normal	Square wave input	6.8	17.5	
			TA = +85°C	operation	Resonator connection	6.9	17.5	

Notes 1. Total current flowing into V_{DD}, EV_{DDD}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.
The currents in the "TYP." column do not include the operating currents of the peripheral modules.
The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten. In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral flowing the current flowing the peripheral modules.

- Notes 2. When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 3. When high-speed system clock and subsystem clock are stopped.
- **Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).
- **Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:	2.7 V \leq V_DD \leq 5.5 V@1 MHz to 32 MHz
	2.4 V \leq V _{DD} \leq 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode:	1.8 V \leq V _{DD} \leq 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode:	1.6 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 4 MHz

- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remarks 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remarks 3. f_H: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remarks 4. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- **Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^{\circ}C$



(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

$(T_A = -40 \text{ to } +85^{\circ} \text{ C}, 1.6 \text{ V} \le \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{Vss} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0 \text{ V})$ (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Uni
Supply	IDD2	HALT mode	HS (high-speed main)	fhoco = 64 MHz,	VDD = 5.0 V		0.93	3.32	mA
current Note 1	Note 2		mode Nate 7	fin = 32 MHz Note 4	VDD = 3.0 V		0.93	3.32	1
				fHoco = 32 MHz,	VDD = 5.0 V		0.5	2.63	1
				fin = 32 MHz Note 4	V _{DD} = 3.0 V		0.5	2.63	1
				fHOCO = 48 MHz,	VDD = 5.0 V		0.72	2.60	1
				fiH = 24 MHz Note 4	V _{DD} = 3.0 V		0.72	2.60	1
				fносо = 24 MHz,	VDD = 5.0 V		0.42	2.03	1
				fiH = 24 MHz Note 4	V _{DD} = 3.0 V		0.42	2.03	1
				fHOCO = 16 MHz,	V _{DD} = 5.0 V		0.39	1.50	1
				fin = 16 MHz Note 4	V _{DD} = 3.0 V		0.39	1.50	1
			LS (low-speed main)	fносо = 8 MHz,	VDD = 3.0 V		270	800	μA
			mode Note Z	fiH = 8 MHz Note 4	VDD = 2.0 V		270	800	1
		LV (low-voltage main)	fносо = 4 MHz,	V _{DD} = 3.0 V		450	755	μ	
		n	mode Nate Z	fin = 4 MHz Note 4	VDD = 2.0 V		450	755	1
					Square wave input		0.31	1.69	m
				VDD = 5.0 V	Resonator connection		0.41	1.91	1
				fmx = 20 MHz Note 3,	Square wave input		0.31	1.69	1
				VDD = 3.0 V	Resonator connection		0.41	1.91	1
				fmx = 10 MHz Note 3,	Square wave input		0.21	0.94	1
				VDD = 5.0 V	Resonator connection		0.26	1.02	1
				fmx = 10 MHz Note 3,	Square wave input		0.21	0.94	1
				VDD = 3.0 V	Resonator connection		0.26	1.02	1
			LS (low-speed main)	fmx = 8 MHz Note 3,	Square wave input		110	610	μÆ
			mode Note Z	VDD = 3.0 V	Resonator connection		150	660	1
				fmx = 8 MHz Note 3,	Square wave input		110	610	1
]			VDD = 2.0 V	Resonator connection		150	660	1

		STOP mode	TA = -40°C		0.19		μA
	Note_6	Note.8	TA = +25°C		0.30	0.59	
			TA = +50°C		0.41	3.42	
			TA = +70°C		0.80	6.03	
			TA = +85°C		1.53	10.39	

Notes 1. Total current flowing into V_{DD}, EV_{DDD}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

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(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

$(T_A = -40 \text{ to } +85^\circ \text{ C}, 1.6 \text{ V} \le \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{ V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0 \text{ V})$ (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Uni
Supply	IDD2	HALT mode	HS (high-speed main)	fносо = 64 MHz,	VDD = 5.0 V		0.93	3.32	mA
current Note 1	Note 2		mode Note 6	fiH = 32 MHz Note 4	V _{DD} = 3.0 V		0.93	3.32	1
				fHOCO = 32 MHz,	VDD = 5.0 V		0.5	2.63	1
				fin = 32 MHz Note 4	VDD = 3.0 V		0.5	2.63	1
				fносо = 48 MHz,	VDD = 5.0 V		0.72	2.60	1
				fiH = 24 MHz Note 4	V _{DD} = 3.0 V		0.72	2.60	1
				fносо = 24 MHz,	VDD = 5.0 V		0.42	2.03	1
				fiH = 24 MHz Note 4	VDD = 3.0 V		0.42	2.03	1
				fносо = 16 MHz,	VDD = 5.0 V		0.39	1.50	1
				fiH = 16 MHz Note 4	VDD = 3.0 V		0.39	1.50	1
			LS (low-speed main)	fHOCO = 8 MHz,	VDD = 3.0 V		270	800	μ
	LV (low-voltage main)	fiH = 8 MHz Note 4	VDD = 2.0 V		270	800	1		
		fносо = 4 MHz,	VDD = 3.0 V		450	755	μ		
		· · · · · · · · · · · · · · · · · · ·	fiH = 4 MHz Note 4	VDD = 2.0 V		450	755	1	
			HS (high-speed main)	fmx = 20 MHz Note 3,	Square wave input		0.31	1.69	m
			mode Note 6	V _{DD} = 5.0 V	Resonator connection		0.41	1.91	1
				f _{MX} = 20 MHz Note 3,	Square wave input		0.31	1.69	1
				VDD = 3.0 V	Resonator connection		0.41	1.91	1
				fmx = 10 MHz Note 3,	Square wave input		0.21	0.94	1
				V _{DD} = 5.0 V	Resonator connection		0.26	1.02	1
				f _{MX} = 10 MHz Note 3,	Square wave input		0.21	0.94	1
				V _{DD} = 3.0 V	Resonator connection		0.26	1.02	1
			LS (low-speed main)	f _{MX} = 8 MHz Note 3,	Square wave input		110	610	μ
		VDD = 3.0 V	Resonator connection		150	660	1		
			f _{MX} = 8 MHz Note 3,	Square wave input		110	610	1	
				VDD = 2.0 V	Resonator connection		150	660	1

IDD3	STOP mode	T _A = -40°C	0.19		μA
	Note 7	TA = +25°C	0.30	0.59	
		T _A = +50°C	0.41	3.42	
		T _A = +70°C	0.80	6.03	
		Ta = +85°C	1.53	10.39	

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.

The currents in the "TYP." column do not include the operating currents of the peripheral modules.

• The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-

chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten. In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

In the STOP mode, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.



- Notes 2. During HALT instruction execution by flash memory.
- $\label{eq:Notes 3.} When high-speed on-chip oscillator and subsystem clock are stopped.$
- Notes 4. When high-speed system clock and subsystem clock are stopped.
- Notes 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and, watchdog timer...

Notes 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Notes 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

 $\begin{array}{ll} \mbox{HS (high-speed main) mode:} & 2.7 \ \mbox{V} \le \ \mbox{V}_{\text{DD}} \le 5.5 \ \mbox{V@1 MHz to 32 MHz} \\ & 2.4 \ \mbox{V} \le \ \mbox{V}_{\text{DD}} \le 5.5 \ \mbox{V@1 MHz to 16 MHz} \\ \mbox{LS (low-speed main) mode:} & 1.8 \ \mbox{V} \le \ \mbox{V}_{\text{DD}} \le 5.5 \ \mbox{V@1 MHz to 8 MHz} \\ \end{array}$

LV (low-voltage main) mode: $1.6 V \le V_{DD} \le 5.5 V@1 MHz$ to 4 MHz

- **Notes. 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remarks 2. fH000: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remarks 3. fin: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remarks 4. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- **Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^{\circ}C$

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	•	LT instruction executi	
Notes J.	when high		ator and subsystem clock are stopped.
Notes 4.	Whon high		and subsystem clock are stopped.
	•		
Notes 5.	•		ator and high-speed system clock are stopped. When RTCLPC = 1
		0	nsumption (AMPHS1 = 1).
Notes 6.		nip between operation	voltage width, operation frequency of CPU and operation mode is as
	below.		
	HS (high-	speed main) mode:	2.7 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 32 MHz
			2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz
	LS (low-s	peed main) mode:	1.8 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 8 MHz
	LV (low-v	oltage main) mode:	1.6 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 4 MHz
Notes 7.	Regarding	the value for current	to operate the subsystem clock in STOP mode, refer to that in HALT
	mode.		
Remarks <i>′</i>	1. fмx:	High-speed system	n clock frequency (X1 clock oscillation frequency or external main
Remarks 2	2 funco.		o oscillator clock frequency (64 MHz max.)
Remarks :		• • •	oscillator clock frequency (32 MHz max.)
Remarks 4		• • •	equency (XT1 clock oscillation frequency)
Remarks			eration and STOP mode, temperature condition of the TYP. value is T_A =
	25°0	3	



5. 35.3.2 Supply current characteristics (Page 1244 to Page 1255)

Incorrect:

35.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

$(T_A = -40 \text{ to } +105^\circ \text{ C}, 2.4 \text{ V} \le \text{EV}_{\text{DD}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{VSS} = \text{EV}_{\text{SS0}} = 0 \text{ V})$ (1/2)

Parameter	Symbol			Conditions			MIN.	TYP.	MAX.	Unit
Supply	IDD1	Operating	HS (high-speed main)	fносо = 64 MHz,	Basic	V _{DD} = 5.0 V		2.4		mΑ
current		mode	mode Note 5	fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.4		
Note 1				fносо = 32 MHz,	Basic	VDD = 5.0 V		2.1		
				fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.1		

		fsub = 32.768 kHz Note 4	Normal	Square wave input	5.4	8.9	
		TA = +85°C	operation	Resonator connection	5.4	8.9	
		fsus = 32.768 kHz Note 4	Normal	Square wave input	7.2	21.0	1
		TA = +105°C	operation	Resonator connection	7.3	21.1]

- Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Notes 2. When high-speed on-chip oscillator and subsystem clock are stopped.
- **Notes 3.** When high-speed system clock and subsystem clock are stopped.
- Notes 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Notes 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

 $\begin{array}{ll} \text{HS (high-speed main) mode:} & 2.7 \ \text{V} \leq V_{\text{DD}} \leq 5.5 \ \text{V@1 MHz to 32 MHz} \\ & 2.4 \ \text{V} \leq V_{\text{DD}} \leq 5.5 \ \text{V@1 MHz to 16 MHz} \end{array}$

- Remarks 1. flox: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remarks 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remarks 3. fn: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remarks 4. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remarks 5. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

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Correct:

35.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

$(TA = -40 \text{ to } +105^{\circ} \text{ C}, 2.4 \text{ V} \le \text{EV}_{\text{DD0}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{Vss} = \text{EV}_{\text{SS0}} = 0 \text{ V})$ (1/2)

Parameter	Symbol			Conditions			MIN.	TYP.	MAX.	Unit
Supply	IDD1	Operating	HS (high-speed main)	fhoco = 64 MHz,	Basic	VDD = 5.0 V		2.4		mA
current		mode	mode Note 5	fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.4		1
Note 1				fhoco = 32 MHz,	Basic	VDD = 5.0 V		2.1		1
				fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.1		1
										1

		fsus = 32.768 kHz Note 4	Normal	Square wave input	5.4	8.9	
		TA = +85°C	operation	Resonator connection	5.4	8.9	
		fsus = 32.768 kHz Note 4	Normal	Square wave input	7.2	21.0	1
		TA = +105°C	operation	Resonator connection	7.3	21.1	

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main) mode.

The currents in the "TYP." column do not include the operating currents of the peripheral modules.

• The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

- Notes 2. When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 3. When high-speed system clock and subsystem clock are stopped.
- **Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).
- **Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V \leq V_DD \leq 5.5 V@1 MHz to 32 MHz 2.4 V \leq V_DD \leq 5.5 V@1 MHz to 16 MHz

Remarks	1.	fмx:	High-speed system clock frequency (X1 clock oscillation frequency or external main
			system clock frequency)
Remarks	2.	fносо:	High-speed on-chip oscillator clock frequency (64 MHz max.)
Remarks	3.	fн:	High-speed on-chip oscillator clock frequency (32 MHz max.)
Remarks	4.	fsuв:	Subsystem clock frequency (XT1 clock oscillation frequency)
Remarks	5.	Excep	t subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C



(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

$(T_A = -40 \text{ to } +105^\circ \text{ C}, 2.4 \text{ V} \le \text{EV}_{\text{DD}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{VSS} = \text{EV}_{\text{SS0}} = 0 \text{ V})$ (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply current	IDD2	HALT mode	HS (high-speed main)	fHOCO = 64 MHz,	VDD = 5.0 V		0.80	4.36	mA
Note 1	Note 2		mode Nate Z	fiH = 32 MHz Note 4	VDD = 3.0 V		0.80	4.36	1
				fhoco = 32 MHz,	VDD = 5.0 V		0.49	3.67	1
				fiH = 32 MHz Note 4	VDD = 3.0 V		0.49	3.67	1
				fHOCO = 48 MHz,	VDD = 5.0 V		0.62	3.42	1
				fiH = 24 MHz Note 4	VDD = 3.0 V		0.62	3.42	
				fhoco = 24 MHz,	VDD = 5.0 V		0.4	2.85	1
			fiH = 24 MHz Note 4	VDD = 3.0 V		0.4	2.85	1	
			fHOCO = 16 MHz,	VDD = 5.0 V		0.37	2.08	1	
			fiH = 16 MHz Note 4	VDD = 3.0 V		0.37	2.08		
			HS (high-speed main)	f _{MX} = 20 MHz Note 3,	Square wave input		0.28	2.45	mA
			mode Note Z	VDD = 5.0 V	Resonator connection		0.40	2.57	1
				fmx = 20 MHz Note 3,	Square wave input		0.28	2.45	1
			V _{DD} = 3.0 V	Resonator connection		0.40	2.57	1	
			f _{MX} = 10 MHz Note 3,	Square wave input		0.19	1.28	1	
			VDD = 5.0 V	Resonator connection		0.25	1.36	1	
			f _{MX} = 10 MHz Note 3,	Square wave input		0.19	1.28	1	
				VDD = 3.0 V	Resonator connection		0.25	1.36	

IDD3		TA = -40°C		0.18	0.51	μA
Note.6	Note 8	TA = +25°C		0.24	0.51	
		TA = +50°C		0.29	1.10	
		TA = +70°C		0.41	1.90	
		TA = +85°C		0.90	3.30	
		TA = +105°C		3.10	17.00	

- Notes 1. Total current flowing into V_{DD} and EV_{DDD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DDD} or V_{SS}, EV_{SSD}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- **Notes 2.** During HALT instruction execution by flash memory.
- Notes 3. When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 4. When high-speed system clock and subsystem clock are stopped.
- Notes 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is. included. However, not including the current flowing into the 12-bit interval timer and watchdog timer...

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(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

$(T_A = -40 \text{ to } +105^{\circ} \text{ C}, 2.4 \text{ V} \le \text{EV}_{\text{DD}0} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{VSS} = \text{EV}_{\text{SS0}} = 0 \text{ V})$ (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply current		HALT mode	HS (high-speed main)	fhoco = 64 MHz,	VDD = 5.0 V		0.80	4.36	mA
Note 1	Note 2		mode Note 6	fiH = 32 MHz Note 4	VDD = 3.0 V		0.80	4.36	
				fHOCO = 32 MHz,	VDD = 5.0 V		0.49	3.67	
				fin = 32 MHz Note 4	VDD = 3.0 V		0.49	3.67	
				fHOCO = 48 MHz,	VDD = 5.0 V		0.62	3.42	
				fiH = 24 MHz Note 4	VDD = 3.0 V		0.62	3.42	
				fHOCO = 24 MHz,	VDD = 5.0 V		0.4	2.85	
			fho	fiH = 24 MHz Note 4	VDD = 3.0 V		0.4	2.85	
				fHOCO = 16 MHz,	VDD = 5.0 V		0.37	2.08	
				fiH = 16 MHz Note 4	VDD = 3.0 V		0.37	2.08	
			HS (high-speed main)	f _{MX} = 20 MHz Note 3,	Square wave input		0.28	2.45	mA
			mode Note 6	VDD = 5.0 V	Resonator connection		0.40	2.57	
				f _{MX} = 20 MHz Note 3,	Square wave input		0.28	2.45	
				VDD = 3.0 V	Resonator connection		0.40	2.57	
			V _{DD} =	f _{MX} = 10 MHz Note 3,	Square wave input		0.19	1.28	
				VDD = 5.0 V	Resonator connection		0.25	1.36	
				f _{MX} = 10 MHz Note 3,	Square wave input		0.19	1.28	
				VDD = 3.0 V	Resonator connection		0.25	1.36	

т							
	IDD3	STOP mode	TA = -40°C		0.18	0.51	μA
		Note 7	TA = +25°C		0.24	0.51	
			TA = +50°C		0.29	1.10	
			T _A = +70°C		0.41	1.90	
			TA = +85°C		0.90	3.30	
			TA = +105°C		3.10	17.00	

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main) mode.

The currents in the "TYP." column do not include the operating currents of the peripheral modules.

• The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

In the STOP mode, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.

- Notes 2. During HALT instruction execution by flash memory.
- Notes 3. When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 4. When high-speed system clock and subsystem clock are stopped.
- **Notes 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).



Notes 6. Not including the current flowing into the RTC. 12-bit interval timer, and watchdog timer.

Notes 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

 $\begin{array}{ll} \text{HS (high-speed main) mode:} & 2.7 \ \text{V} \leq V_{\text{DD}} \leq 5.5 \ \text{V@1 MHz to } 32 \ \text{MHz} \\ & 2.4 \ \text{V} \leq V_{\text{DD}} \leq 5.5 \ \text{V@1 MHz to } 16 \ \text{MHz} \end{array}$

Notes. 8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remarks 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- **Remarks 3.** f_H: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remarks 4. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- **Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

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Notes 6.		hip between operation voltage width, operation frequency of CPU and operation mode is as
	below.	
	HS (high-	-speed main) mode: $2.7 \text{ V} \le V_{DD} \le 5.5 \text{ V} @1 \text{ MHz}$ to 32 MHz
		2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz
Notes 7.	Regarding	g the value for current operate the subsystem clock in STOP mode, refer to that in HALT
	mode.	
Remarks [•]	1. fмx:	High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
Remarks 2	2. fносо:	High-speed on-chip oscillator clock frequency (64 MHz max.)
Remarks	3. f⊩:	High-speed on-chip oscillator clock frequency (32 MHz max.)
Remarks -	4. fsuв:	Subsystem clock frequency (XT1 clock oscillation frequency)
Remarks	5. Excep	t subsystem clock operation and STOP mode, temperature condition of the TYP. value is T _A =
	25°	C



(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +105° C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (1/2)

Parameter	Symbol			Conditions			MIN.	TYP.	MAX.	Unit
Supply	IDD1	Operating	HS (high-speed main)	fHOCO = 64 MHz,	Basic	VDD = 5.0 V		2.6		mΑ
current		mode	mode Note 5	fiH = 32 MHz Note 3	operation	V _{DD} = 3.0 V		2.6		
Note 1				fносо = 32 MHz,	Basic	VDD = 5.0 V		2.3		1
				fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.3		1
						Resonator connection		6.5	14.5	

_								
			fsub = 32.768 kHz Note 4	Normal	Square wave input	13.0	58.0	
			TA = +105°C	operation	Resonator connection	13.0	58.0	

- Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, J/O port, and on-chip. pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Notes 2. When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 3. When high-speed system clock and subsystem clock are stopped.
- Notes 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12bit interval timer and watchdog timer.
- **Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

 $\begin{array}{ll} \text{HS (high-speed main) mode:} & 2.7 \ \text{V} \le V_{\text{DD}} \le 5.5 \ \text{V@1 MHz to 32 MHz} \\ & 2.4 \ \text{V} \le V_{\text{DD}} \le 5.5 \ \text{V@1 MHz to 16 MHz} \end{array}$

- **Remarks 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remarks 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- **Remarks 3.** fin: High-speed on-chip oscillator clock frequency (32 MHz max.)
- **Remarks 4.** fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- **Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^{\circ}C$

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(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

$(T_A = -40 \text{ to } +105^{\circ} \text{ C}, 2.4 \text{ V} \le \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{Vss} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0 \text{ V})$ (1/2)

Parameter	Symbol			Conditions			MIN.	TYP.	MAX.	Unit
Supply	IDD1	Operating	HS (high-speed main)	fносо = 64 MHz,	Basic	V _{DD} = 5.0 V		2.6		mA
current		mode	mode Note 5	fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.6		
Note 1				fHOCO = 32 MHz,	Basic	VDD = 5.0 V		2.3		
				fin = 32 MHz Note 3	operation	VDD = 3.0 V		2.3		1
						Resonator connection		6.5	14.5	1
										<u> </u>

_								
			fsub = 32.768 kHz Note 4	Normal	Square wave input	13.0	58.0	
			TA = +105°C	operation	Resonator connection	13.0	58.0	

Notes 1. Total current flowing into V_{DD}, EV_{DDD}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The following points apply in the HS (high-speed main) mode.

The currents in the "TYP." column do not include the operating currents of the peripheral modules.

- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and onchip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.
 In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.
- Notes 2. When high-speed on-chip oscillator and subsystem clock are stopped.
- **Notes 3.** When high-speed system clock and subsystem clock are stopped.
- **Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).
- **Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

 HS (high-speed main) mode:
 $2.7 V \le V_{DD} \le 5.5 V@1 MHz$ to 32 MHz

 $2.4 V \le V_{DD} \le 5.5 V@1 MHz$ to 16 MHz

- **Remarks 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remarks 2. fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remarks 3. fin: High-speed on-chip oscillator clock frequency (32 MHz max.)
- **Remarks 4.** fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remarks 5. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C



(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

$(T_{A} = -40 \text{ to } +105^{\circ} \text{ C}, 2.4 \text{ V} \le \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{Vss} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0 \text{ V}) (2/2)$

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply	IDD2	HALT mode	HS (high-speed main)	fhoco = 64 MHz,	VDD = 5.0 V		0.79	4.86	mA
current Note 1	Note 2		mode Note Z	fiH = 32 MHz Note 4	VDD = 3.0 V		0.79	4.86	1
				fhoco = 32 MHz,	VDD = 5.0 V		0.49	4.17	1
				fin = 32 MHz Note 4	VDD = 3.0 V		0.49	4.17	1
				fhoco = 48 MHz,	VDD = 5.0 V		0.62	3.82	1
				fin = 24 MHz Note 4	VDD = 3.0 V		0.62	3.82	1
				fhoco = 24 MHz,	VDD = 5.0 V		0.4	3.25	1
			fin = 24 MHz Note 4	VDD = 3.0 V		0.4	3.25	1	
		fhoco = 16 MHz,	VDD = 5.0 V		0.38	2.28	1		
			fiH = 16 MHz Note 4	V _{DD} = 3.0 V		0.38	2.28	1	
			HS (high-speed main)	f _{MX} = 20 MHz Note 3,	Square wave input		0.30	2.65	mA
			mode Note Z	VDD = 5.0 V	Resonator connection		0.40	2.77	1
				f _{MX} = 20 MHz Note 3,	Square wave input		0.30	2.65	1
				V _{DD} = 3.0 V	Resonator connection		0.40	2.77	1
		f _{MX} = 10 MHz Note 3,	Square wave input		0.20	1.36	1		
		VDD = 5.0 V	Resonator connection		0.25	1.46	1		
		f _{MX} = 10 MHz Note 3,	Square wave input		0.20	1.36	1		
				VDD = 3.0 V	Resonator connection		0.25	1.46	1

	-					
	IDD3	STOP mode	TA = -40°C	0.19	0.57	μA
	Note.6	Note.8	T _A = +25°C	0.25	0.57	
		TA = +50°C TA = +70°C TA = +85°C	T _A = +50°C	0.33	2.26	
			T _A = +70°C	0.52	3.99	
			T _A = +85°C	1.46	8.00	
			T _A = +105°C	5.50	50.00	

- Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip. pull-up/pull-down resistors and the current flowing during data flash rewrite.
- **Notes 2.** During HALT instruction execution by flash memory.
- Notes 3. When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 4. When high-speed system clock and subsystem clock are stopped.
- Notes 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is. included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Notes 6...Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

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(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

$(T_A = -40 \text{ to } +105^{\circ} \text{ C}, 2.4 \text{ V} \le \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{Vss} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0 \text{ V})$ (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply	IDD2	HALT mode	HS (high-speed main)	fHoco = 64 MHz,	V _{DD} = 5.0 V		0.79	4.86	mA
current Note 1	Note 2		mode Note 6	fiH = 32 MHz Note 4	VDD = 3.0 V		0.79	4.86	1
				fhoco = 32 MHz,	V _{DD} = 5.0 V		0.49	4.17	1
				fiH = 32 MHz Note 4	VDD = 3.0 V		0.49	4.17	1
				fhoco = 48 MHz,	V _{DD} = 5.0 V		0.62	3.82	1
				fiH = 24 MHz Note 4	VDD = 3.0 V		0.62	3.82	1
				fhoco = 24 MHz,	V _{DD} = 5.0 V		0.4	3.25	
		fiH = 24 MHz Note 4	V _{DD} = 3.0 V		0.4	3.25			
	fносо = 16 MHz, fiн = 16 MHz Note 4	fносо = 16 MHz,	VDD = 5.0 V		0.38	2.28			
		V _{DD} = 3.0 V		0.38	2.28	1			
			HS (high-speed main)	f _{MX} = 20 MHz Note 3,	Square wave input		0.30	2.65	mA
			mode Note 6	VDD = 5.0 V	Resonator connection		0.40	2.77	
				f _{MX} = 20 MHz Note 3,	Square wave input		0.30	2.65	
				VDD = 3.0 V	Resonator connection		0.40	2.77	1
		f _{MX} = 10 MHz Note 3,	Square wave input		0.20	1.36			
		VDD = 5.0 V	Resonator connection		0.25	1.46	1		
				f _{MX} = 10 MHz Note 3,	Square wave input		0.20	1.36	1
				VDD = 3.0 V	Resonator connection		0.25	1.46	1

T			1							1
I		IDD3	STOP mode	TA = -40°C			0.19	0.57	μA	
I			Note 7	Ta = +25°C			0.25	0.57		ĺ
I			TA = +50°C			0.33	2.26		ĺ	
		TA = +70°C TA = +85°C	TA = +70°C			0.52	3.99			
I				1.46	8.00					
				TA = +105°C			5.50	50.00		

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The following points apply in the HS (high-speed main) mode.

The currents in the "TYP." column do not include the operating currents of the peripheral modules.

 The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and onchip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.
 In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

In the STOP mode, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.

- **Notes 2.** During HALT instruction execution by flash memory.
- Notes 3. When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 4. When high-speed system clock and subsystem clock are stopped.
- **Notes 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).



Notes.7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

 HS (high-speed main) mode:
 $2.7 V \le V_{DD} \le 5.5 V@1 MHz$ to 32 MHz

 $2.4 V \le V_{DD} \le 5.5 V@1 MHz$ to 16 MHz

Notes.8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. fmx:	High-speed system clock frequency (X1 clock oscillation frequency or external main
	system clock frequency)

- Remarks 2. fHoco: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remarks 3. fin: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remarks 4. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- **Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^{\circ}C$

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Notes 6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below. HS (high-speed main) mode: $2.7 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}$ @1 MHz to 32 MHz $2.4 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}@1 \text{ MHz}$ to 16 MHz Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT Notes 7. mode. Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency) High-speed on-chip oscillator clock frequency (64 MHz max.) Remarks 2. fHOCO: Remarks 3. fil: High-speed on-chip oscillator clock frequency (32 MHz max.) Remarks 4. fsuB: Subsystem clock frequency (XT1 clock oscillation frequency) Remarks 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C



(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

$(T_A = -40 \text{ to } +105^{\circ} \text{ C}, 2.4 \text{ V} \le \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{Vss} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0 \text{ V})$ (1/2)

Parameter	Symbol			MIN.	TYP.	MAX.	Unit			
Supply	IDD1	Operating	HS (high-speed main)	fносо = 64 MHz,	Basic	VDD = 5.0 V		2.9		mA
current Note 1		mode	mode Note 5	fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.9		1
NOLE I				fносо = 32 MHz,	Basic	VDD = 5.0 V		2.5		1
				fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.5]

		fsub = 32.768 kHz Note 4	Normal	Square wave input	6.8	17.5	
		TA = +85°C	operation	Resonator connection	6.9	17.5	
		fsus = 32.768 kHz Note 4	Normal	Square wave input	15.5	77.8	
		TA = +105°C	operation	Resonator connection	15.5	77.8	

- Notes 1. Total current flowing into V_{DD}, EV_{DDD}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current. flowing into the A/D converter. D/A converter, comparator, LVD circuit, I/O port, and on-chip. pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Notes 2. When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 3. When high-speed system clock and subsystem clock are stopped.
- Notes 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12bit interval timer and watchdog timer.
- **Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V \leq V_{DD} \leq 5.5 V@1 MHz to 32 MHz 2.4 V \leq V_{DD} \leq 5.5 V@1 MHz to 16 MHz

- Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- **Remarks 2.** fHOCO: High-speed on-chip oscillator clock frequency (64 MHz max.)
- **Remarks 3.** f_H: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remarks 4. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- **Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

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(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

$(T_A = -40 \text{ to } +105^{\circ} \text{ C}, 2.4 \text{ V} \le \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{Vss} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0 \text{ V})$ (1/2)

Parameter	Symbol		Conditions						MAX.	Unit
Supply	IDD1	Operating	HS (high-speed main)	fHoco = 64 MHz,	Basic	VDD = 5.0 V		2.9		mA
current		mode	mode Note 5	fiH = 32 MHz Note 3	operation	VDD = 3.0 V		2.9		1
Note 1					Basic	VDD = 5.0 V		2.5		1
					operation	VDD = 3.0 V		2.5		1
										1

	fsub = 32.768 kHz Note 4	Normal	Square wave input	6.8	17.5	
	TA = +85°C	operation	Resonator connection	6.9	17.5	
	fsus = 32.768 kHz Note 4	Normal	Square wave input	15.5	77.8	
	TA = +105°C	operation	Resonator connection	15.5	77.8	

Notes 1. Total current flowing into V_{DD}, EV_{DDD}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The following points apply in the HS (high-speed main) mode.

The currents in the "TYP." column do not include the operating currents of the peripheral modules.

- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and onchip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.
 In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.
- Notes 2. When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 3. When high-speed system clock and subsystem clock are stopped.
- **Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).
- **Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

 HS (high-speed main) mode:
 $2.7 V \le V_{DD} \le 5.5 V@1 MHz$ to 32 MHz

 $2.4 V \le V_{DD} \le 5.5 V@1 MHz$ to 16 MHz

- Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remarks 2. fH000: High-speed on-chip oscillator clock frequency (64 MHz max.)
- **Remarks 3.** fin: High-speed on-chip oscillator clock frequency (32 MHz max.)
- **Remarks 4.** fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- **Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^{\circ}C$



(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

$(T_A = -40 \text{ to } +105^{\circ} \text{ C}, 2.4 \text{ V} \le \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{Vss} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0 \text{ V})$ (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply	IDD2	HALT mode	HS (high-speed main)	fhoco = 64 MHz,	VDD = 5.0 V		0.93	5.16	mA
current Note 1	Note 2		mode Note 7	fiH = 32 MHz Note 4	VDD = 3.0 V		0.93	5.16	1
				fhoco = 32 MHz,	VDD = 5.0 V		0.5	4.47	1
				fiH = 32 MHz Note 4	VDD = 3.0 V		0.5	4.47	1
				fHOCO = 48 MHz,	VDD = 5.0 V		0.72	4.08	1
				fiH = 24 MHz Note 4	VDD = 3.0 V		0.72	4.08	1
				fHOCO = 24 MHz,	V _{DD} = 5.0 V		0.42	3.51	1
			fHOCO =		VDD = 3.0 V		0.42	3.51	1
				fносо = 16 MHz,	VDD = 5.0 V		0.39	2.38	1
				fin = 16 MHz Note 4	V _{DD} = 3.0 V		0.39	2.38	1
			HS (high-speed main)				0.31	2.83	mA
			mode Note.Z	VDD = 5.0 V	Resonator connection		0.41	2.92	1
				f _{MX} = 20 MHz Note 3,	Square wave input		0.31	2.83	1
				VDD = 3.0 V	Resonator connection		0.41	2.92	1
				f _{MX} = 10 MHz Note 3,	Square wave input		0.21	1.46	1
				VDD = 5.0 V	Resonator connection		0.26	1.57	1
				f _{MX} = 10 MHz Note 3,	Square wave input		0.21	1.46	1
				VDD = 3.0 V	Resonator connection		0.26	1.57	1

	IDD3	STOP mode	TA = -40°C			0.19	0.63	μA
	Note.6	Note.8	TA = +25°C			0.30	0.63	
			TA = +50°C			0.41	3.47	
		TA = +70°C TA = +85°C	0.80	6.08				
				1.53	10.44			
			TA = +105°C			6.50	67.14	

- Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip. pull-up/pull-down resistors and the current flowing during data flash rewrite.
- **Notes 2.** During HALT instruction execution by flash memory.
- Notes 3. When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 4. When high-speed system clock and subsystem clock are stopped.
- Notes 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Notes 6...Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

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(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

$(T_A = -40 \text{ to } +105^{\circ} \text{ C}, 2.4 \text{ V} \le \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{Vss} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0 \text{ V})$ (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply	IDD2	HALT mode	HS (high-speed main)	fносо = 64 MHz,	V _{DD} = 5.0 V		0.93	5.16	mA
current Note 1	Note 2		mode Note 6	fiH = 32 MHz Note 4	V _{DD} = 3.0 V		0.93	5.16	
				fноco = 32 MHz,	V _{DD} = 5.0 V		0.5	4.47	
				fin = 32 MHz Note 4	VDD = 3.0 V		0.5	4.47	
				fноco = 48 MHz,	V _{DD} = 5.0 V		0.72	4.08	
				fiH = 24 MHz Note 4	V _{DD} = 3.0 V		0.72	4.08	
				fноco = 24 MHz,	V _{DD} = 5.0 V		0.42	3.51	
			fiH = 24 MHz Note 4	fiH = 24 MHz Note 4	V _{DD} = 3.0 V		0.42	3.51	
				fHoco = 16 MHz,	V _{DD} = 5.0 V		0.39	2.38	
				fiH = 16 MHz Note 4	VDD = 3.0 V		0.39	2.38	
		fmx = 20 MHz Note 3,	Square wave input		0.31	2.83	mA		
			mode Note 6	VDD = 5.0 V	Resonator connection		0.41	2.92	
				f _{MX} = 20 MHz Note 3,	Square wave input		0.31	2.83	
				V _{DD} = 3.0 V	Resonator connection		0.41	2.92	
				fmx = 10 MHz Note 3,	Square wave input		0.21	1.46	
				VDD = 5.0 V	Resonator connection		0.26	1.57	
		f _{MX} = 10 MHz Note 3,	Square wave input		0.21	1.46			
		VDD = 3.0 V	Resonator connection		0.26	1.57			

	IDD3	STOP mode	TA = -40°C	0.19	0.63	μA	1
		Note 7	TA = +25°C	0.30	0.63		1
			T _A = +50°C	0.41	3.47		1
			T _A = +70°C	0.80	6.08		1
	TA = +85°C	T _A = +85°C	1.53	10.44		1	
			T _A = +105°C	6.50	67.14		ì

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The following points apply in the HS (high-speed main) mode.

The currents in the "TYP." column do not include the operating currents of the peripheral modules.

 The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and onchip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.
 In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

In the STOP mode, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.

- **Notes 2.** During HALT instruction execution by flash memory.
- Notes 3. When high-speed on-chip oscillator and subsystem clock are stopped.
- Notes 4. When high-speed system clock and subsystem clock are stopped.
- **Notes 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).



Notes.7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

 HS (high-speed main) mode:
 $2.7 V \le V_{DD} \le 5.5 V@1 MHz$ to 32 MHz

 $2.4 V \le V_{DD} \le 5.5 V@1 MHz$ to 16 MHz

Notes.8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. fmx:	High-speed system clock frequency (X1 clock oscillation frequency or external main
	system clock frequency)

- Remarks 2. fHoco: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remarks 3. fin: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remarks 4. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
- **Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^{\circ}C$

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Notes 6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below. HS (high-speed main) mode: $2.7 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}$ @1 MHz to 32 MHz $2.4 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}@1 \text{ MHz}$ to 16 MHz Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT Notes 7. mode. Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency) High-speed on-chip oscillator clock frequency (64 MHz max.) Remarks 2. fHOCO: Remarks 3. fil: High-speed on-chip oscillator clock frequency (32 MHz max.) Remarks 4. fsuB: Subsystem clock frequency (XT1 clock oscillation frequency) Remarks 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

