RENESAS TECHNICAL UPDATE

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Title RH850 RLIN3 timeout error Information Category Technical Notification Applicable Product See "Table 1". Lot No. All Iot Reference Document See "Table 1". The limitations of RLIN3 timeout error are added as follows: Reference Document See "Table 1". Red character: Added Product and Reference Document User's Manual RH850/C1M-A1, C1M-A2 Product User's Manual RH850/C1M-A1, C1M-A2 R01UH0607EJ0120 R1H850/C1M-A1, C1M-A2 RH850/F1H Product User's Manual RH850/F1H R01UH0451EJ0220 R1H850/F1H RH850/F1H R01UH045EJ0112 R01UH045EJ0112 RH850/F1H R01UH045EJ0112 R01UH045EJ0112 RH850/F1H, R7F701501AXX/R7F701502AXX/R7F701506AXX/R7F701507AXX) R01UH045EJ0112 RH850/F1K R01UH0452L0110 R01UH0452L0110 RH850/F1K R01UH0452L0110 R01UH052EJ0110 RH850/	Product Category	MPU/MCU Document No.			TN-RH8-B0352A/E	TN-RH8-B0352A/E Rev.			
Applicable Product See "Table 1". Reference Document See "Table 1". All lot Reference Document See "Table 1". Added See "Table 1". See "Table 1". Product User's Manual See "Table 1". Product User's Manual See "Table 1".	Title	RH850 RLIN3 timeout error			Technical Notification				
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RH850/P1x-C R01UH0517EJ0130 RH850/P1L-C R01UH0592EJ0110 RH850/P1x R01UH0436EJ0140 RH850/P1M-E R01UH0585EJ0120 RH850/E2x-FCC1, E2M R01UH0641EJ0130 RH850/E2x-FCC2, E2UH, E2H R01UH0770EJ0110	Table 1 RH850, RH850, RH850, RH850,	Applicable Product and Reference Document Product /C1M-A1, C1M-A2 /D1x /F1M /F1H (R7F701501AXX/R7F701502AXX/R7F70		7F701507AXX)	R01UH0607EJ012 R01UH0451EJ022 R01UH0518EJ010 R01UH0445EJ011	20 20 03 12			
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RH850/P1x R01UH0436EJ0140 RH850/P1M-E R01UH0585EJ0120 RH850/E2x-FCC1, E2M R01UH0641EJ0130 RH850/E2x-FCC2, E2UH, E2H R01UH0770EJ0110	Table 1 RH850/ RH850/ RH850/ RH850/ RH850/ RH850/ RH850/	Applicable Product and Reference Document Product /C1M-A1, C1M-A2 /D1x /F1M /F1H (R7F701501AXX/R7F701502AXX/R7F70 /F1H-100 /F1K /F1KH, F1KM		87F701507AXX)	R01UH0607EJ012 R01UH0607EJ012 R01UH0451EJ022 R01UH0518EJ010 R01UH0445EJ011 R01UH0631EJ010 R01UH0631EJ010 R01UH0562EJ011	20 20 03 12 00 10			
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RH850/E2x-FCC1, E2M R01UH0641EJ0130 RH850/E2x-FCC2, E2UH, E2H R01UH0770EJ0110	Table 1 RH850/ RH850/ RH850/ RH850/ RH850/ RH850/ RH850/ RH850/ RH850/	Applicable Product and Reference Document Product /C1M-A1, C1M-A2 /D1x /F1M /F1H (R7F701501AXX/R7F701502AXX/R7F70) /F1H-100 /F1K /F1KH, F1KM /P1L-C		87F701507AXX)	R01UH0607EJ012 R01UH0607EJ012 R01UH0451EJ022 R01UH0518EJ010 R01UH0631EJ010 R01UH0631EJ010 R01UH0562EJ011 R01UH0684EJ012 R01UH0517EJ013 R01UH0592EJ011	20 20 03 12 00 10 20 30 10			
RH850/E2x-FCC2, E2UH, E2H R01UH0770EJ0110	Table 1 RH850/ RH850/ RH850/ RH850/ RH850/ RH850/ RH850/ RH850/ RH850/ RH850/	Applicable Product and Reference Document Product /C1M-A1, C1M-A2 /D1x /F1M /F1H (R7F701501AXX/R7F701502AXX/R7F70 /F1H-100 /F1K /F1KH, F1KM /P1x-C /P1L-C /P1x		27F701507AXX)	R01UH0607EJ012 R01UH0607EJ012 R01UH0451EJ022 R01UH0518EJ010 R01UH0631EJ010 R01UH0631EJ010 R01UH0631EJ010 R01UH0634EJ012 R01UH0517EJ013 R01UH0592EJ011 R01UH0592EJ011 R01UH0436EJ014	20 20 20 12 20 10 20 20 20 30 10 40			
	Table 1 RH850/ RH850/ RH850/ RH850/ RH850/ RH850/ RH850/ RH850/ RH850/ RH850/ RH850/	Applicable Product and Reference Document Product /C1M-A1, C1M-A2 /D1x /F1M /F1H (R7F701501AXX/R7F701502AXX/R7F70) /F1H-100 /F1K /F1KK /F1KH, F1KM /P1x-C /P1x-C /P1x-E		87F701507AXX)	R01UH0607EJ012 R01UH0607EJ012 R01UH0451EJ022 R01UH0518EJ010 R01UH0631EJ010 R01UH0631EJ010 R01UH0631EJ010 R01UH0631EJ010 R01UH0631EJ010 R01UH0631EJ011 R01UH0562EJ011 R01UH0517EJ013 R01UH0517EJ014 R01UH0532EJ014 R01UH0436EJ014 R01UH0585EJ012	20 20 20 12 20 10 20 30 10 40 20			
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2. User's Manual Update: C1M-A1, C1M-A2

Section 13 LIN/UART Interface (RLIN3)

13.3 Registers

13.3.2 LIN Master Related Registers

13.3.2.10 RLN3nLEDE – LIN Error Detection Enable Register

FTERE Bit (Timeout Error Detection Enable)

The FTERE bit enables or disables detection of the frame timeout error or the response timeout error. With 0 set, the frame timeout error or response timeout error is not detected. With 1 set, the frame timeout error or response timeout error is detected. When this bit is set to 1, the detection result is indicated in the FTER flag in the RLN3nLEST register. With the LTES bit, either the frame timeout error or response timeout error can be selected. Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received. For details on the timeout error, see **Section 13.7.7, Error Status**.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 13.4**.

13.3.2.11 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode. With 0 set, LIN reset mode is caused. With 1 set, LIN reset mode is canceled.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 13.4**.



13.3.3 LIN Slave Related Registers

13.3.3.9 RLN3nLEDE – LIN Error Detection Enable Register

TERE Bit (Timeout Error Detection Enable)

The TERE bit enables or disables detection of the frame timeout error or the response timeout error. With 0 set, the frame timeout error or response timeout error is not detected. With 1 set, the frame timeout error or response timeout error is detected. When this bit is set to 1, the detection result is indicated in the TER flag in the RLN3nLEST register. With the LTES bit, either the frame timeout error or response timeout error can be selected. The timeout error should not be used in LIN slave mode [auto baud rate] (when the LMD[1:0] bits in the RLN3nLMD register are "10_B"). Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received. For details on the timeout error, see **Section 13.7.7, Error Status**. If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 13.4**.

13.3.3.10 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode. With 0 set, LIN reset mode is caused.

With 1 set, LIN reset mode is canceled.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 13.4**.



Table 13.76 Transition Condition for Operation Mode

13.7 LIN Mode

	Operation Mode Transition			Transition Condition
(1)	LIN reset mode	→	LIN mode • LIN operation mode	LMD bit in RLN3nLMD register = 00_B or 10_B or 11_B and OM1 and OM0 bits in RLN3nLCUC register = 11_B
(2)	LIN reset mode	→	LIN mode • LIN wake-up mode	LMD bit in RLN3nLMD register = 00_{B} or 10_{B} or 11_{B} and OM1 and OM0 bits in RLN3nLCUC register = 01_{B}
(3) *2	LIN mode • LIN operation mode • LIN wake-up mode	→	LIN reset mode	OM0 bit in RLN3nLCUC register = 0 ₈
(4)* ¹	LIN mode	→	LIN mode • LIN wake-up mode	OM1 and OM0 bits in RLN3nLCUC register = 01_B
(5)*1	LIN mode • LIN wake-up mode	→	LIN mode • LIN operation mode	OM1 and OM0 bits in RLN3nLCUC register = 11_B

Note 1. Transition between LIN operation mode and LIN wake-up mode cannot be made when communication is going on (when the FTS bit in the RLN3nLTRC register is 1).

Note 2. In LIN mode, if RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1 or RLN3nLEDE.TERE =1), users should take the procedure shown in **Figure 13.4**. The procedure is to protect a RLIN3 error interrupt and clear a RLIN3 error interrupt request.





Figure 13.4 LIN reset sequence by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used

Note 1. This "n" value means interrupt number. See Section 13.1.4, Interrupt Requests and confirm interrupt numbers of RLIN3n status interrupt (n = 0 to 2) in Table 13.6. For EICn, refer to Section 6, Interrupts.



13.7.7 Error Status

13.7.7.1 LIN Master Mode

Table 13.86	Types of Error Statuses in LIN Master Mode
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Status		Error Detection Condition	Operation Mode Capable of Error Detection	Communication	Enable/ Disable Detection	Corresponding Bit
Bit error	r	The transmitted data and the data on the LIN bus monitored by the receive pin do not match *1*2	LIN operation mode	Cancel	1	BER flag in RLN3nLEST
			 LIN wake-up mode 			register
Physical bus error		 LIN bus is detected to be high level when sending a break 	 LIN operation mode 	Cancel	1	PBER flag in RLN3nLEST
		 LIN bus is detected to be low level when sending a break delimiter 	 LIN wake-up mode 			register
		LIN bus is detected to be high level when sending a wake-up				
Timeout	t error	A frame or response transmission/reception does not terminate within a given time*3*4	LIN operation mode	Cancel	1	FTER flag in RLN3nLEST register
Framing	g error	In response field reception, a stop bit of each data byte is low level	LIN operation mode	Cancel	1	FER flag in RLN3nLEST register
Checksi error	um	In response field reception, the result of checksum test gives an error	LIN operation mode	-	×	CSER flag in RLN3nLEST register
Respon: preparat error		One of the following conditions occurs in frame separate mode during a multi-byte response reception:	LIN operation mode	Cancel	×	RPER flag in RLN3nLEST register
		The first reception data byte is received after completion of header transmission but before a				
		response transmission/reception request is set				
		 The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set. 				
Note 1.	lf a bi	 The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data 		or is detected in a	non-dataar	rea, such as ar
Note 1.		 The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set. 	bit is sent. If a bit en			
Note 1.	inter-	The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set. it error is detected, processing is stopped after a stop to	bit is sent. If a bit en y after the bit which	had the error is se	ent. If a bit e	error is detected
	inter- during	The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set. it error is detected, processing is stopped after a stop to byte space, the transmission is suspended immediated	bit is sent. If a bit en y after the bit which wake-up is cance	had the error is se led after the error-	ent. If a bit e	error is detected
Note 2.	inter-l during In a n The t	The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set. it error is detected, processing is stopped after a stop to byte space, the transmission is suspended immediated g the transmission of a wake-up, the transmission of the multi-byte response transmission, bit errors are detected imeout time depends on the response field data length.	bit is sent. If a bit en y after the bit which e wake-up is cance d also between dat (the RFDL [3:0] bit	had the error is se led after the error- a groups. s in the RLN3nLDI	ent. If a bit e causing bit FC register)	error is detected is sent. and the
Note 1. Note 2. Note 3.	inter- during In a n The ti check	The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set. it error is detected, processing is stopped after a stop to byte space, the transmission is suspended immediatel g the transmission of a wake-up, the transmission of the multi-byte response transmission, bit errors are detected imeout time depends on the response field data length ksum selection (the CSM bit in the RLN3nLDFC register	oit is sent. If a bit en y after the bit which e wake-up is cance d also between dat (the RFDL [3:0] bit er), and can be calc	had the error is se led after the error- a groups. s in the RLN3nLD ulated from the fol	ent. If a bit e causing bit FC register) lowing form	error is detecte is sent. and the ula.
Note 2.	inter-I during In a n The ti check Wher eight	The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set. it error is detected, processing is stopped after a stop to byte space, the transmission is suspended immediated g the transmission of a wake-up, the transmission of the multi-byte response transmission, bit errors are detected imeout time depends on the response field data length.	it is sent. If a bit en y after the bit which e wake-up is cance d also between dat (the RFDL [3:0] bit er), and can be calc is 1 (i.e., frame se tet. Once the RTS b	had the error is so led after the error- a groups. s in the RLN3nLDI ulated from the fol paration mode), the it is set, the timeo	ent. If a bit e causing bit FC register) lowing form e timeout tin	and the ula. ne is that for
Note 2.	inter- during In a n The ti check Wher eight based	The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set. it error is detected, processing is stopped after a stop to byte space, the transmission is suspended immediatel g the transmission of a wake-up, the transmission of the multi-byte response transmission, bit errors are detected imeout time depends on the response field data length ksum selection (the CSM bit in the RLN3nLDFC register in the setting of the FSM bit in the RLN3nLTRC register is set bytes until the RTS bit of the RLN3nLTRC register is set.	it is sent. If a bit en y after the bit which e wake-up is cance d also between dat (the RFDL [3:0] bit er), and can be calc is 1 (i.e., frame se tet. Once the RTS b	had the error is so led after the error- a groups. s in the RLN3nLDI ulated from the fol paration mode), the it is set, the timeo	ent. If a bit e causing bit FC register) lowing form e timeout tin	and the ula. ne is that for
Note 2.	inter- during In a n The ti check Wher eight based [Fran On cl	 The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set. it error is detected, processing is stopped after a stop to byte space, the transmission is suspended immediatel g the transmission of a wake-up, the transmission of the multi-byte response transmission, bit errors are detected imeout time depends on the response field data length ksum selection (the CSM bit in the RLN3nLDFC register in the setting of the FSM bit in the RLN3nLDFC register bytes until the RTS bit of the RLN3nLTRC register is s d on the response field data length (the RFDL[3:0] bits me timeout] 	bit is sent. If a bit en y after the bit which ie wake-up is cance d also between dat (the RFDL [3:0] bit er), and can be calc is 1 (i.e., frame sep tet. Once the RTS b in the RLN3nLDFC	had the error is so led after the error- a groups. s in the RLN3nLDI ulated from the fol paration mode), the it is set, the timeo register). + (number of data	ent. If a bit e causing bit FC register) lowing form e timeout tin ut time is re	and the ula. ne is that for -set to the time × 14 [Tbit]
Note 2.	inter- during In a n The ti check Wher eight based [Fran On ck On ck	 The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set. it error is detected, processing is stopped after a stop to byte space, the transmission is suspended immediatel g the transmission of a wake-up, the transmission of the multi-byte response transmission, bit errors are detected imeout time depends on the response field data length ksum selection (the CSM bit in the RLN3nLDFC register in the setting of the FSM bit in the RLN3nLDFC register bytes until the RTS bit of the RLN3nLTRC register is s d on the response field data length (the RFDL[3:0] bits me timeout] assic selection (when the LCS bit in RLN3nLDFC is 0) nhanced selection (when the LCS bit in RLN3nLDFC is 0) 	bit is sent. If a bit en y after the bit which e wake-up is cance d also between dat (the RFDL [3:0] bit er), and can be calc is 1 (i.e., frame sep tet. Once the RTS b in the RLN3nLDFC : Timeout time = 49 5 1): Timeout time =	had the error is se led after the error- a groups. s in the RLN3nLDI ulated from the fol paration mode), the it is set, the timeo register). + (number of data 48 + (number of d	ent. If a bit e causing bit FC register) lowing form e timeout tin ut time is re bytes + 1) lata bytes +	and the ula. ne is that for -set to the time × 14 [Tbit] 1) × 14 [Tbit]
lote 2.	inter- during In a n The ti check Wher eight based [Fran On cl On er The a	 The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set. it error is detected, processing is stopped after a stop to byte space, the transmission is suspended immediatel g the transmission of a wake-up, the transmission of the multi-byte response transmission, bit errors are detected imeout time depends on the response field data length ksum selection (the CSM bit in the RLN3nLDFC register in the setting of the FSM bit in the RLN3nLDFC register bytes until the RTS bit of the RLN3nLTRC register is s d on the response field data length (the RFDL[3:0] bits me timeout] assic selection (when the LCS bit in RLN3nLDFC is 0) infanced selection (when the LCS bit in RLN3nLDFC is aforementioned timeout time is a time greater than the 	bit is sent. If a bit en y after the bit which e wake-up is cance d also between dat (the RFDL [3:0] bit er), and can be calc is 1 (i.e., frame sep tet. Once the RTS b in the RLN3nLDFC : Timeout time = 49 s 1): Timeout time = TFRAME_MAX of L	had the error is se led after the error- a groups. s in the RLN3nLDI ulated from the fol paration mode), the it is set, the timeor register). + (number of data 48 + (number of d	ent. If a bit e -causing bit FC register) lowing form e timeout tin ut time is re bytes + 1) lata bytes + ackage Rev	and the ula. ne is that for -set to the time × 14 [Tbit] 1) × 14 [Tbit]
Note 2.	inter-l during In a n The ti check Wher eight based (Fran On cl On er The a classi	The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set. it error is detected, processing is stopped after a stop the byte space, the transmission is suspended immediatel g the transmission of a wake-up, the transmission of the multi-byte response transmission, bit errors are detected imeout time depends on the response field data length ksum selection (the CSM bit in the RLN3nLDFC register in the setting of the FSM bit in the RLN3nLDFC register bytes until the RTS bit of the RLN3nLTRC register is so d on the response field data length (the RFDL[3:0] bits me timeout] assic selection (when the LCS bit in RLN3nLDFC is 0) inhanced selection (when the LCS bit in RLN3nLDFC is aforementioned timeout time is a time greater than the ic selection, or the TFRAME_MAX of LIN Specification	bit is sent. If a bit en y after the bit which e wake-up is cance d also between dat (the RFDL [3:0] bit er), and can be calc is 1 (i.e., frame sep tet. Once the RTS b in the RLN3nLDFC : Timeout time = 49 s 1): Timeout time = TFRAME_MAX of L	had the error is se led after the error- a groups. s in the RLN3nLDI ulated from the fol paration mode), the it is set, the timeor register). + (number of data 48 + (number of d	ent. If a bit e -causing bit FC register) lowing form e timeout tin ut time is re bytes + 1) lata bytes + ackage Rev	and the ula. ne is that for -set to the time × 14 [Tbit] 1) × 14 [Tbit]
Note 2.	inter-l during In a n The ti check When eight based (Fran On cl On er The a classi (Res)	 The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set. it error is detected, processing is stopped after a stop to byte space, the transmission is suspended immediatel g the transmission of a wake-up, the transmission of the multi-byte response transmission, bit errors are detected imeout time depends on the response field data length ksum selection (the CSM bit in the RLN3nLDFC register in the setting of the FSM bit in the RLN3nLDFC register bytes until the RTS bit of the RLN3nLTRC register is s d on the response field data length (the RFDL[3:0] bits me timeout] assic selection (when the LCS bit in RLN3nLDFC is 0) infanced selection (when the LCS bit in RLN3nLDFC is aforementioned timeout time is a time greater than the 	bit is sent. If a bit en y after the bit which e wake-up is cance d also between dat (the RFDL [3:0] bit er), and can be calc is 1 (i.e., frame sep tet. Once the RTS b in the RLN3nLDFC : Timeout time = 49 s 1): Timeout time = TFRAME_MAX of L	had the error is se led after the error- a groups. s in the RLN3nLDI ulated from the fol paration mode), the it is set, the timeor register). + (number of data 48 + (number of d	ent. If a bit e -causing bit FC register) lowing form e timeout tin ut time is re bytes + 1) lata bytes + ackage Rev	and the ula. ne is that for -set to the time × 14 [Tbit] 1) × 14 [Tbit]
Note 2.	inter- during In a n The ti check Wher eight based (Fran On ch On ch On ch On ch Check (Fran Check (Fran Check (Fran Check (Fran Check (Fran Check (Fran Check) (Fran) (Fran Check) (Fran (Fran) (Fr	 The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set. it error is detected, processing is stopped after a stop I byte space, the transmission is suspended immediatel g the transmission of a wake-up, the transmission of th multi-byte response transmission, bit errors are detected imeout time depends on the response field data length ksum selection (the CSM bit in the RLN3nLDFC register in the setting of the FSM bit in the RLN3nLDFC register bytes until the RTS bit of the RLN3nLTRC register is s d on the response field data length (the RFDL[3:0] bits me timeout] assic selection (when the LCS bit in RLN3nLDFC is aforementioned timeout time is a time greater than the ic selection, or the TFRAME_MAX of LIN Specification ponse timeout] 	bit is sent. If a bit en y after the bit which e wake-up is cance d also between dat (the RFDL [3:0] bit er), and can be calc is 1 (i.e., frame sep et. Once the RTS b in the RLN3nLDFC : Timeout time = 49 5 1): Timeout time = TFRAME_MAX of L Package Revision	had the error is se led after the error- a groups. s in the RLN3nLDI ulated from the fol paration mode), the it is set, the timeor register). + (number of data 48 + (number of d	ent. If a bit e -causing bit FC register) lowing form e timeout tin ut time is re bytes + 1) lata bytes + ackage Rev	and the ula. ne is that for -set to the time × 14 [Tbit] 1) × 14 [Tbit]
Note 2.	inter- during In a n The ti check Wher eight based [Fran On cl On er The a classi [Resj Timed Wher If RL	 The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set. it error is detected, processing is stopped after a stop I byte space, the transmission is suspended immediatel g the transmission of a wake-up, the transmission of th multi-byte response transmission, bit errors are detected inneout time depends on the response field data length ksum selection (the CSM bit in the RLN3nLDFC register h the setting of the FSM bit in the RLN3nLDFC register bytes until the RTS bit of the RLN3nLTRC register is s d on the response field data length (the RFDL[3:0] bits me timeout] assic selection (when the LCS bit in RLN3nLDFC is 0) nhanced selection (when the LCS bit in RLN3nLDFC is aforementioned timeout time is a time greater than the ic selection, or the TFRAME_MAX of LIN Specification ponse timeout] out time = (number of data bytes + 1) × 14 [Tbit] 	bit is sent. If a bit en y after the bit which e wake-up is cance d also between dat (the RFDL [3:0] bit er), and can be calc is 1 (i.e., frame sep et. Once the RTS b in the RLN3nLDFC : Timeout time = 49 5 1): Timeout time = TFRAME_MAX of L Package Revision stops. CUC.OM0 to 0 whe	had the error is so led after the error- a groups. s in the RLN3nLDI ulated from the fol baration mode), the it is set, the timeour register). + (number of data 48 + (number of data 48 + (number of data 1N Specification P 2.x on enhanced s	ent. If a bit e causing bit FC register) lowing form e timeout tin ut time is re bytes + 1) lata bytes + ackage Rev election.	and the ula. ne is that for -set to the time × 14 [Tbit] 1) × 14 [Tbit] rision 1.3 on



13.7.7.2 LIN Slave Mode

Bit error Timeout error		Operation Mode Capable of Error Detection	Communication	Enable/ Disable Detection	Corresponding Bit				
error	The transmitted data and the data on the LIN bus monitored by the receive pin do not match *1*2	LIN operation mode LIN wake-up mode	Cancel	1	BER flag in RLN3nLEST register				
Framina	A frame or response transmission/reception does not terminate within a given time*3 *6	LIN operation mode	Cancel	1	TER flag in RLN3nLEST register				
Framing error	In response field reception, a stop bit of each data byte is low level	LIN operation mode		1	FER flag in RLN3nLEST register				
Sync field error	If the width of the break low level is greater than the width set by the LBLT bit in the RLN3nLBFC register and the sync field is not $55_{\rm H}$	LIN operation mode	Cancel	√* ⁴	SFER flag in RLN3nLEST register				
Checksun error	In response field reception, the result of checksum test gives an error	LIN operation mode	*5	×	CSER flag in RLN3nLEST register				
ID parity error	If the received ID parity bit does not match the value that is automatically calculated by the LIN/UART interface	LIN operation mode	Cancel	1	IPER flag in RLN3nLEST register				
Response preparatio error		LIN operation mode	Cancel	×	RPER flag in RLN3nLEST register				
ote 1. I	f a bit error is detected, processing is stopped after a s	stop bit is sent. If a bit er	ror is detected in a	non-data ar	ea, such as an				
i	nter-byte space, the transmission is suspended immed	diately after the bit which	had the error is se	ent. If a bit e	rror is detected				
c	during the transmission of a wake-up, the transmission	of the wake-up is cance	eled after the error-	causing bit i	s sent.				
ote 2. I	n a multi-byte response transmission, bit error can be	detected between data	groups.						
ote 3. 1	The timeout time depends on the response field data le	ength (the RFDL [3:0] bit	s in the RLN3nLD	FC register)	and the				
c	checksum selection (the LCS bit in the RLN3nLDFC re	gister), and this can be	calculated accordir	ng to the folk	owing formula.				
7	The time-out period until the RTS or LNRR bit of the R	LN3nLTRC register is se	et is 8 data bytes. \	When the RT	S bit is set, the				
t	imeout time is reset to the time based on the response	e field data length (RFDL	[3:0] bit of the RLM	3nLDFC reg	gister). When				
t	he LNRR bit is set, the timeout function stops.								
[Frame timeout]								
C	On classic selection (when the LCS bit in RLN3nLDFC is 0):								
	Timeout time = 49 + (number of data bytes + 1)×	14 [Tbit]							
	On enhanced selection (when the LCS bit in RLN3nLD								
C	Timeout time = 48 + (number of data bytes + 1) ×								
	The aforementioned timeout time is a time greater thar	_	-	ackage Rev	ision 1.3 on				
١	classic selection, or the TFRAME_MAX of LIN Specific	ation Package Revision	2.x on enhanced s	selection.					
T	-	alion Package Revision	2.x on enhanced s	election.					
1 0	classic selection, or the TFRAME_MAX of LIN Specific	allon Package Revision	2.x on enhanced s	election.					
ר כ ו	classic selection, or the TFRAME_MAX of LIN Specific Response timeout]	-	2.x on ennanced s	election.					
ר כ נ ר ע	classic selection, or the TFRAME_MAX of LIN Specific Response timeout] Fimeout time = (number of data bytes + 1) × 14 [Tbit]	ction stops.							
1 (1 v ote 4. (ote 5. (classic selection, or the TFRAME_MAX of LIN Specific Response timeout] Fimeout time = (number of data bytes + 1) × 14 [Tbit] When en error is detected, time-out error detection fun	ction stops. abled/disabled. Error de	tection cannot be	enabled/disa	bled.				
I I Iote 4. C Iote 5. C is	classic selection, or the TFRAME_MAX of LIN Specific Response timeout] Fimeout time = (number of data bytes + 1) × 14 [Tbit] When en error is detected, time-out error detection fun Only reflection of the result to the SFER flag can be en Checksum judgment is performed upon completion of r	ction stops. abled/disabled. Error de response frame receptio	tection cannot be n. In case of an er	enabled/disa ror, thereceiv	bled.				



3. User's Manual Update: D1x

Section 20 LIN/UART Interface (RLIN3)

20.3 Registers

20.3.2 LIN Master Related Registers

20.3.2.10 RLN3nLEDE – LIN Error Detection Enable Register

FTERE Bit (Timeout Error Detection Enable)

The FTERE bit enables or disables detection of the frame timeout error or the response timeout error.

With 0 set, the frame timeout error or response timeout error is not detected.

With 1 set, the frame timeout error or response timeout error is detected.

When this bit is set to 1, the detection result is indicated in the FTER flag in the RLN3nLEST register.

With the LTES bit, either the frame timeout error or response timeout error can be selected.

Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received.

For details on the timeout error, see Section 20.7.6, Error Status.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 20.4**.

20.3.2.11 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode.

With 0 set, LIN reset mode is caused.

With 1 set, LIN reset mode is canceled.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 20.4**.



20.7 LIN Mode

	Operation Mode Transition		Transition Condition
(1)	LIN reset mode	 → LIN mode ◆ LIN operation mode 	LMD[1:0] bit in RLN3nLMD register = 00 _B and OM1 and OM0 bits in RLN3nLCUC register = 11 _B
(2)	LIN reset mode	 → LIN mode ◆ LIN wake-up mode 	LMD[1:0] bit in RLN3nLMD register = 00_B and OM1 and OM0 bits in RLN3nLCUC register = 01_B
(3) *2	LIN mode LIN operation mode LIN wake-up mode 	→ LIN reset mode	OM0 bit in RLN3nLCUC register = 0 _B
(4) *1	LIN mode LIN operation mode 	 → LIN mode ◆ LIN wake-up mode 	OM1 and OM0 bits in RLN3nLCUC register = 01_{B}
(5) ∗1	LIN mode LIN wake-up mode 	 → LIN mode ◆ LIN operation mode 	OM1 and OM0 bits in RLN3nLCUC register = 11_{B}

 Table 20.58
 Transition Condition for Operation Mode

Note 1. Transition between LIN operation mode and LIN wake-up mode cannot be made when communication

is going on (when the FTS bit in the RLN3nLTRC register is 1).

Note 2. In LIN mode, if RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1 or RLN3nLEDE.TERE =1), users should take the procedure shown in **Figure 20.4**. The procedure is to protect a RLIN3 error interrupt and clear a RLIN3 error interrupt request.





- Figure 20.4 SW reset sequence when the timeout function is used
- Note 1. This "n" value means interrupt number. See Section 20.1.4, Interrupt Requests and confirm interrupt numbers of RLIN3n status interrupt (n = 0 to 3) in Table 20.7. For EICn, refer to Section 7, Interrupt.



20.7.6 Error Status

Status	Error Detecti	ion Condition	Operation Mode Capable of Error Detection	Commu nication	Enable/Di sable Detection	Corresponding Bit	
Biterror	The transmitt	ed data and the data on the LIN	LIN operation mode	Cancel	Enabled	BER flag in	
		d by the receive pin do not match	LIN wake-up mode			RLN3nLEST register	
Physical bus error	 LIN bus is sending a 	s detected to be high level when I break	LIN operation mode LIN wake-up mode	Cancel	Enabled	PBER flag in RLN3nLEST	
		s detected to be low level when break delimiter				register	
	 LIN bus is detected to be high level when sending a wake-up 						
Timeout error	A frame or response transmission/reception does not terminate within a given time ^{*3} ^{'4}		LIN operation mode	Cancel	Enabled	FTER flag in RLN3nLEST register	
Framing error	In response fi data byte is lo	ield reception, a stop bit of each ow level	LIN operation mode	Cancel	Enabled	FER flag in RLN3nLEST register	
Checksum error		ield reception, the result of st gives an error	LIN operation mode	-	Disabled	CSER flag in RLN3nLEST register	
Response preparation error		llowing conditions occurs in frame le during a multi-byte response	LIN operation mode	Cancel	Disabled	RPER flag in RLN3nLEST register	
	completio	eception data byte is received after n of header transmission but response transmission/reception s set					
	The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set.						
	Note 1.	If a bit error is detected, the proce data area, such as an inter-byte sp is detected during the transmissio error-causing bit is sent.	bace, the transmission is can	eled immedi	iately after th	at area. If a bit en	
	Note 2.	In a multi-byte response transmis	sion, bit errors are detected	also betweer	n data groups	5.	
	Note 3.	The timeout time depends on the r and the checksum selection (the C to the following formula: When the FSM bit in the RLN3nL0 the 8 data bytes until the RTS bit time is changed to the time based register).	CSM bit in the RLN3nLDFC re DFC register is set to 1 (fram of the RLN3nLTRC register i	egister), and e separate m is set. Once	this can be ca node), the tim the RTS bit is	alculated accordin neout time is that s set, the timeout	
		[Frame timeout] On classic selection (when the CS bytes + 1) × 14 [Tbit] On enhanced selection (when the					
		bytes + 1) × 14 [Tbit] The aforementioned timeout time Revision 1.3 on classic selection, enhanced selection. [Response timeout]	-	_		-	
		Transit Keep a farmh an ef data b	ytes + 1) × 14 [Tbit]				
		Timeout time = (number of data b					
	Note 4.	When an error is detected, time-o		-			



4. User's Manual Update:

F1M,

F1H (R7F701501AXX/R7F701502AXX/R7F701506AXX/R7F701507AXX), F1H-100, F1K, F1KH, F1KM

Regarding the target chapter, R01UH0518EJ0103 (F1M) is 18, R01UH0445EJ0112 (F1H) is 18,

R01UH0631EJ0100 (F1H-100) is 18, R01UH0562EJ0110 (F1K) is 19 and R01UH0684EJ0120 (F1KH, F1KM) is 22.

The following descriptions show based on RH850/F1KH, RH850/F1KM User's manual.

Section 22 LIN/UART Interface (RLIN3)

22.3 Registers

- 22.3.2 LIN Master Related Registers
- 22.3.2.10 RLN3nLEDE LIN Error Detection Enable Register

FTERE Bit (Timeout Error Detection Enable)

The FTERE bit enables or disables detection of the frame timeout error or the response timeout error. With 0 set, the frame timeout error or response timeout error is not detected. With 1 set, the frame timeout error or response timeout error is detected. When this bit is set to 1, the detection result is reflected in the FTER flag of the RLN3nLEST register. With the LTES bit, either the frame timeout error or response timeout error can be selected. Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received. For details on the timeout error, see **Section 22.7.7, Error Statuses**.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 22.4**.

21.3.2.11 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode. With 0 set, LIN reset mode.

With 1 set, LIN reset mode is canceled.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 22.4**.



22.3.3 LIN Slave Related Registers

22.3.3.9 RLN3nLEDE – LIN Error Detection Enable Register

TERE Bit (Timeout Error Detection Enable)

The TERE bit enables or disables detection of the frame timeout error or the response timeout error. With 0 set, the frame timeout error or response timeout error is not detected. With 1 set, the frame timeout error or response timeout error is detected. When this bit is set to 1, the detection result is reflected in the TER flag of the RLN3nLEST register. With the LTES bit, either the frame timeout error or response timeout error can be selected. The timeout error should not be used in LIN slave mode [auto baud rate] (when the LMD[1:0] bits in the RLN3nLMD register are "10_B"). Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received. For details on the timeout error, see **Section 22.7.7, Error Statuses**. If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 22.4**.

21.3.3.10 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode. With 0 set, LIN/UART interface enters LIN reset mode. With 1 set, LIN reset mode of LIN/UART interface is canceled. If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in Figure 22.4.



22.7 LIN Mode

Table 22.91 Transition Conditions for Operating Modes

	Operation Mode Transition		Transition Condition
(1)	LIN reset mode	→ LIN mode	LMD bits in RLN3nLMD register = 00 _B or 10 _B or 11 _B
		 LIN operation mode 	and
			OM1 and OM0 bits in RLN3nLCUC register = 11 _B
(2)	LIN reset mode	→ LIN mode	LMD bits in RLN3nLMD register = 00 _B or 10 _B or 11 _B
		 LIN wake-up mode 	and
			OM1 and OM0 bits in RLN3nLCUC register = 01 _B
(3)*2	LIN mode	→ LIN reset mode	OM0 bit in RLN3nLCUC register = 0 _B
	 LIN operation mode 		
	 LIN wake-up mode 		
(4)* ¹	LIN mode	→ LIN mode	OM1 and OM0 bits in RLN3nLCUC register = 01 _B
	 LIN operation mode 	 LIN wake-up mode 	
(5)* ¹	LIN mode	→ LIN mode	OM1 and OM0 bits in RLN3nLCUC register = 11 ₈
	 LIN wake-up mode 	 LIN operation mode 	

Note 1. Transition between LIN operation mode and LIN wake-up mode cannot be made when communication is in progress (when the FTS bit in the RLN3nLTRC register is 1).

Note 2. In LIN mode, if RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1 or RLN3nLEDE.TERE =1), users should take the procedure shown in **Figure 22.4**. The procedure is to protect a RLIN3 error interrupt and clear a RLIN3 error interrupt request.





Figure 22.4 LIN reset sequence by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used



Note 1. This "xxx" value means interrupt name. See Section 22.1.4, Interrupt Requests and confirm interrupt numbers of RLIN3n interrupt or RLIN3n status interrupt (n = 0 to 7) in Table 22.17, Table 22.18 and Table 22.19 in accordance with the value of RLN3nLMD.LIOS. For ICxxx, refer to Section 7A Exception/Interrupts of RH850/F1KH-D8 and Section 7BC Exception/Interrupts of RH850/F1KM.

22.7.7 Error Statuses

22.7.7.1 LIN Master Mode

Table 22.101 Types of Error Statuses in LIN Master Mode

		·	•		•	
Status		Error Detection Condition	Operating Mode Capable of Error Detection	Communi cation	Enable/ Disable Detection	Corresponding Bit
Bit error		The transmitted data and the data on the LIN bus monitored by the receive pin do not match *1.*2	LIN operation mode LIN wake-up mode	Aborted	Enabled	BER flag in RLN3nLEST register
Physical bus error		 LIN bus is detected to be high level when transmitting a break LIN bus is detected to be low level when transmitting a break delimiter LIN bus is detected to be high level when transmitting a wake-up 	 LIN operation mode LIN wake-up mode 	Aborted	Enabled	PBER flag in RLN3nLEST register
Timeout	error	A frame or response transmission/reception does not terminate within a given time*3·4	LIN operation mode	Aborted	Enabled	FTER flag in RLN3nLEST register
Framing	error	In response field reception, the stop bit of each data byte is low level	LIN operation mode	Aborted	Enabled	FER flag in RLN3nLEST register
Checksu error	ım	In response field reception, checksum test results in an error	LIN operation mode	-	Disabled	CSER flag in RLN3nLEST register
Respons preparat error		 One of the following conditions occurs in frame separate mode during a multi-byte response reception: The first reception data byte is received after completion of header transmission but before a response transmission/reception request is specified The first reception data byte is received after the completion of previous data group reception but before a transmission/reception request for the next data group is specified. 		Aborted	Disabled	RPER flag in RLN3nLEST register
Note 1.	inter- detec	t error is detected, processing is aborted after a stop byte space, the transmission is aborted immediately ted during the transmission of a wake-up, the transmitted.	after the bit that caused the	error is tra	nsmitted. If a	a bit error is
Note 2.	In a n	nulti-byte response transmission, bit errors are also	detected between data grou	ips.		
Note 3.			ster), and can be calculated (frame separate mode), the the RTS bit is set, the timed	l using the fo	ollowing form e is that of th	nula. ne 8 data bytes
	When bytes When bytes The a check select [Res] Time	timeout] classic checksum is selected (when the CSM bit i + 1) × 14 [Tbit] enhanced checksum is selected (when the CSM bit + 1) × 14 [Tbit] forementioned timeout time is longer than the TFR sum is selected, or the TFRAME_MAX of LIN Spe ted. ponse timeout] put time = (number of data bytes + 1) × 14 [Tbit] an error is detected, time-out error detection function	bit in RLN3nLDFC is 1): Tin AME_MAX of LIN Specification Package Revision	neout time = ation Packa	= 48 + (num) ge Revision	ber of data 1.3 when class
Note 4.		I3 transitions to LIN reset mode by clearing RLN3nLCUC.OI RLN3nLEDE.FTERE = 1), users should take the procedure s		n is		



22.7.7.2 LIN Slave Mode

Table 22.102	Types of Error Statuses in LIN Slave Mode
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Status	Error Detection Condition	Operating Mode Capable of Error Detection	Communication	Enable/Disable Detection	Corresponding Bit
Biterror	The transmitted data and the data on the LIN bus monitored by the receive pin do not match*1*2	LIN operation mode LIN wake-up mode	Aborted	Enabled	BER flag in RLN3nLEST register
Timeout error	A frame or response transmission/reception does not terminate within a given time*3 *6	LIN operation mode	Aborted	Enabled	TER flag in RLN3nLEST register
Framing error	In frame reception, the stop bit of each data byte is low level	LIN operation mode	Aborted	Enabled	FER flag in RLN3nLEST register
Sync field error	If the width of the break low level is greater than the width set by the LBLT bit in the RLN3nLBFC register and the sync field is not $\rm 55_H$	LIN operation mode	Aborted	Enabled*4	SFER flag in RLN3nLEST register
Checksum error	In response field reception, the checksum test results in an error	LIN operation mode	*5	Disabled	CSER flag in RLN3nLEST register
ID parity error	If the received ID parity bit does not match the value that is automatically calculated by the LIN/UART interface	LIN operation mode	Aborted	Enabled	IPER flag in RLN3nLEST register
Response preparation error	 After the reception of a header, if the response is not prepared before the first reception data byte is received 	LIN operation mode	Aborted	Disabled	RPER flag in RLN3nLEST register
	 In a multi-byte response reception, if the preparation for the reception of next data group does not complete before the first reception data byte for the next data group is received 				

inter-byte space, the transmission is aborted immediately after the bit that caused the error is transmitted. If a bit error is detected during the transmission of a wake-up, the transmission of the wake-up is aborted after the bit that caused the error is transmitted.

Note 2. In a multi-byte response transmission, bit errors are also detected between data groups.

Note 3. The timeout time depends on the response field data length (the RFDL [3:0] bits in the RLN3nLDFC register) and the checksum selection (the LCS bit in the RLN3nLDFC register), and this can be calculated according to the following formula. The timeout time is that of 8 data bytes until the RTS bit or the LNRR bit of the RLN3nLTRC register is set. When the RTS bit is set, the timeout time is changed to the time based on the response field data length (RFDL[3:0] bit of the RLN3nLDFC register). When the LNRR bit is set, the timeout function stops.

[Frame timeout]

When classic checksum is selected (when the CSM bit in RLN3nLDFC is 0): Timeout time = 49 + (number of data bytes + 1) × 14 [Tbit]

When enhanced checksum is selected (when the CSM bit in RLN3nLDFC is 1): Timeout time = 48 + (number of data bytes + 1) × 14 [Tbit]

The aforementioned timeout time is longer than the TFRAME_MAX of LIN Specification Package Revision 1.3 when classic checksum is selected, or the TFRAME_MAX of LIN Specification Package Revision 2.x when enhanced checksum is selected.

[Response timeout]

Timeout time = (number of data bytes + 1) × 14 [Tbit] When en error is detected, time-out error detection function stops.

- Note 4. Only reflection of the result to the SFER flag can be enabled/disabled. Error detection cannot be enabled/disabled.
- Note 5. Checksum determination is performed upon completion of response frame reception. In case of an error, the successful reception flag is not set to 1.
- Note 6. If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 22.4**.



5. User's Manual Update: P1x-C

Section 18 LIN/UART Interface (RLIN3)

18.3 Registers

18.3.2 LIN Master Related Registers

18.3.2.10 RLN3nLEDE – LIN Error Detection Enable Register

FTERE Bit (Timeout Error Detection Enable)

The FTERE bit enables or disables detection of the frame timeout error or the response timeout error. With 0 set, the frame timeout error or response timeout error is not detected. With 1 set, the frame timeout error or response timeout error is detected. When this bit is set to 1, the detection result is indicated in the FTER flag in the RLN3nLEST register. With the LTES bit, either the frame timeout error or response timeout error can be selected. Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received. For details on the timeout error, see **Section 18.5.3.7, Error Status**. Timeout error should be disabled for data group communication.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 18.4**.

18.3.2.11 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode. With 0 set, LIN reset mode is caused. With 1 set, LIN reset mode is canceled. If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 18.4**.



18.3.3 LIN Slave Related Registers

18.3.3.9 RLN3nLEDE – LIN Error Detection Enable Register

TERE Bit (Timeout Error Detection Enable)

The TERE bit enables or disables detection of the frame timeout error or the response timeout error. With 0 set, the frame timeout error or response timeout error is not detected.

With 1 set, the frame timeout error or response timeout error is detected.

When this bit is set to 1, the detection result is indicated in the TER flag in the RLN3nLEST register. With the LTES bit, either the frame timeout error or response timeout error can be selected.

The timeout error should not be used in LIN slave mode [auto baud rate] (when the LMD[1:0] bits in the RLN3nLMD register are "10_B").

Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received. For details on the timeout error, see **Section 18.5.3.7**, **Error Status**.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 18.4**.

18.3.3.10 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode. With 0 set, LIN reset mode.

With 1 set, LIN reset mode is canceled.

It takes 3 peripheral clock cycles + 4 communication clock cycles, until the OMM0 bit in the RLN3nLMST register reflects the OM0 bit setting in the RLN3nLCUC register.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 18.4**.



18.5 Operation

18.5.3 LIN Mode

Table 18.74 Transition condition for Operation Mode	4 Transition condition for C	Operation Mode
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	Operation mode transition		Transition condition
(1)	LIN reset mode	→ LIN mode - LIN operation mode	LMD bit in RLN3nLMD register = 00_B or 10_B or 11_B and OM1 and OM0 bits in RLN3nLCUC register = 11_B
(2)	LIN reset mode	→ LIN mode - LIN wake-up mode	LMD bit in RLN3nLMD register = 00_B or 10_B or 11_B and OM1 and OM0 bits in RLN3nLCUC register = 01_B
(3) *2	LIN mode - LIN operation mode - LIN wake-up mode	→ LIN reset mode	OM0 bit in LCUC register = 0 _B
(4) *1	LIN mode - LIN operation mode	→ LIN mode - LIN wake-up mode	OM1 and OM0 bits in RLN3nLCUC register = 01B
(5) *1	LIN mode - LIN wake-up mode	→ LIN mode - LIN operation mode	OM1 and OM0 bits in RLN3nLCUC register = 11 _B

Note 1. Transition between LIN operation mode and LIN wake-up mode cannot be made when communication is going on (when the FTS bit in the RLN3nLTRC register is 1).

Note 2. In LIN mode, if RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1 or RLN3nLEDE.TERE =1), users should take the procedure shown in **Figure 18.4**. The procedure is to protect a RLIN3 error interrupt and clear a RLIN3 error interrupt request.





Figure 18.4 LIN reset sequence by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used

Note 1. This "n" value means interrupt number. See Section 18.1.4, Interrupt Requests and confirm interrupt numbers of RLIN3n status interrupt (n = 0 to 5) in Table 18.6. For EICn, refer to Section 6, Interrupts.



18.5.3.7 Error Status

(1) LIN Master Mode

Status	Error detection	on condition	Operation mode capable of error detection	Commu nication	Enable/ disable detection	Correspondin bit
Bit error		ed data and the data on the LIN d by the receive pin do not match	LIN operation modeLIN wake-up mode	Cancel	Enabled	BER flag in RLN3nLEST register
Physical bus error	sending a	detected to be high level when break detected to be low level when	LIN operation modeLIN wake-up mode	Cancel	Enabled	PBER flag in RLN3nLEST register
	sending a	break delimiter detected to be high level when				5
	sending a	wake-up				
Timeout error		sponse transmission/reception inate within a given time ^{*3} *4	LIN operation mode	Cancel	Enabled	FTER flag in RLN3nLEST register
Framing error	In response fi data byte is lo	eld reception, a stop bit of each w level	LIN operation mode	Cancel	Enabled	FER flag in RLN3nLEST register
Checksum error		eld reception, the result of t gives an error	LIN operation mode	-	Disabled	CSER flag in RLN3nLEST register
Response preparation error		lowing conditions occurs in frame de during a multi-byte response	LIN operation mode	Cancel	Disabled	RPER flag in RLN3nLEST register
	completion	eception data byte is received after n of header transmission but esponse transmission/reception set				
	The first re the complete	eception data byte is received after etion of previous data group before a transmission/reception				
		r another data group is set.				
	Note 1. Note 2. Note 3.	If a bit error is detected, the proce data area, such as an inter-byte sp is detected during the transmission error-causing bit is sent. In a multi-byte response transmiss The timeout time depends on the prior and the checksum selection (the of to the following formula: [Frame timeout] On classic selection (when the Cr + 1) × 14 [Tbit] On enhanced selection (when the bytes + 1) × 14 [Tbit] The aforementioned timeout time	pace, the transmission is cance on of a wake-up, the transmiss asion, bit errors are detected a response field data length (the CSM bit in the RLN3nLDFC reg SM bit in RLN3nLDFC is 0): T e CSM bit in RLN3nLDFC is 1	eled immedi sion of the v Iso between RFDL [3:0] gister), and t imeout time): Timeout t	ately after th vake-up is ca n data group: bits in the RL this can be ca e = 49 + (nun ime = 48 + (r	at area. If a bit en anceled after the s. N3nLDFC regist alculated accordi nber of data byte number of data
		Revision 1.3 on classic selection enhanced selection.	-	-	-	-
		[Response timeout] Timeout time = (number of data	bytes + 1) × 14 [Tbit]			
	Note 4.	If RLIN3 transitions to LIN reset i (RLN3nLEDE.FTERE = 1), users	· · · ·			eout function is us



(2) LIN Slave Mode

Chata	Email 4 1		Operation mode capable of error		Enable/ disable	
Status	Error detection		detection	Communication	detection	Corresponding bit
Bit error		data and the data on the LIN the receive pin do not match ^{*1}	LIN operation mode LIN wake-up mode	Cancel	Enabled	BER flag in RLN3nLEST register
Timeout error		nse transmission/reception te within a given time ^{3*6}	LIN operation mode	Cancel	Enabled	TER flag in RLN3nLEST register
Framing error	In response field data byte is low le	reception, a stop bit of each evel	LIN operation mode	Cancel	Enabled	FER flag in RLN3nLEST register
Sync field error	the width set by t	break low level is greater than he LBLT bit in the RLN3nLBFC sync field is not 55 _H	LIN operation mode	Cancel	Enabled ^{*4}	SFER flag in RLN3nLEST register
Checksum error	In response field checksum test gi	reception, the result of ves an error	LIN operation mode	'5	Disabled	CSER flag in RLN3nLEST register
ID parity error		parity bit does not match the matically calculated by the LIN/	LIN operation mode	Cancel	Enabled	IPER flag in RLN3nLEST register
Response preparation error	first reception response pre Before the con- reception dation in a multi-bytion for the con- reception dation of the con- reception dation of the con- reception dation of the con- reception dation of the con- reception of	eption of a header, before the n data byte is received, eparation is not made in time. completion of receiving the first ta byte for the next data group te response reception, eparation for the next group is time	LIN operation mode	Cancel	Disabled	RPER flag in RLN3nLEST register
	Note 1.	If a bit error is detected, th data area, such as an inter- is detected during the tran- error-causing bit is sent.	byte space, the transmis	sion is canceled im	mediately after	that area. If a bit erro
	Note 1. Note 2. Note 3.	data area, such as an inter- is detected during the trans	-byte space, the transmis smission of a wake-up, f ansmission, bit error car on the response field dat n (the LCS bit in the RLM re time-out period until th S bit is set, the timeout t	ssion is canceled im the transmission of a be detected betwe a length (the RFDL I3nLDFC register), ne RTS or LNRR bi ime is reset to the ti	mediately after the wake-up is een data group (3:0) bits in the l and this can be t of the RLN3nL me based on th	that area. If a bit error canceled after the s. RLN3nLDFC register e calculated according TRC register is set is ne response field data
	Note 2.	data area, such as an inter- is detected during the trans error-causing bit is sent. In a multi-byte response trans The timeout time depends of and the checksum selection to the following formula. The 8 data bytes. When the RT	byte space, the transmis smission of a wake-up, t ansmission, bit error car on the response field dat n (the LCS bit in the RLM he time-out period until the S bit is set, the timeout t e RLN3nLDFC register).	ssion is canceled im the transmission of a be detected betwe a length (the RFDL I3nLDFC register), he RTS or LNRR bi ime is reset to the ti When the LNRR b DFC is 0): Timeout	mediately after the wake-up is een data group [3:0] bits in the l and this can be t of the RLN3nL me based on th it is set, the tim time = 49 + (no	that area. If a bit error canceled after the s. RLN3nLDFC register calculated according TRC register is set in the response field data beout function stops.
	Note 2.	data area, such as an inter- is detected during the tran- error-causing bit is sent. In a multi-byte response tr. The timeout time depends of and the checksum selection to the following formula. Th 8 data bytes. When the RT length (RFDL[3:0] bit of the [Frame timeout] On classic selection (when 1) × 14 [Tbit] On enhanced selection (wh	byte space, the transmis smission of a wake-up, t ansmission, bit error car on the response field dat n (the LCS bit in the RLN ne time-out period until the S bit is set, the timeout t e RLN3nLDFC register). In the CSM bit in RLN3nL hen the CSM bit in RLN3 ut time is a time greater	ssion is canceled im the transmission of the detected betwe a length (the RFDL I3nLDFC register), the RTS or LNRR bi- ime is reset to the ti When the LNRR bi- DFC is 0): Timeout nLDFC is 1): Timeout than the TFRAME_	mediately after the wake-up is een data group [3:0] bits in the l and this can be t of the RLN3nL me based on th it is set, the tim time = 49 + (nu but time = 48 + (that area. If a bit error canceled after the s. RLN3nLDFC register calculated according TRC register is set is ne response field data neout function stops. umber of data bytes (number of data bytes pecification Package
	Note 2.	data area, such as an inter- is detected during the tran- error-causing bit is sent. In a multi-byte response tr. The timeout time depends of and the checksum selection to the following formula. Th 8 data bytes. When the RT length (RFDL[3:0] bit of the [Frame timeout] On classic selection (when 1) × 14 [Tbit] On enhanced selection (wh + 1) × 14 [Tbit] The aforementioned timeo Revision 1.3 on classic selection	byte space, the transmis smission of a wake-up, t ansmission, bit error car on the response field dat n (the LCS bit in the RLN he time-out period until the S bit is set, the timeout the RLN3nLDFC register). In the CSM bit in RLN3nL hen the CSM bit in RLN3nL hen the CSM bit in RLN3 ut time is a time greater lection, or the TFRAME_	ssion is canceled im the transmission of the detected betwe a length (the RFDL I3nLDFC register), the RTS or LNRR bi- ime is reset to the ti When the LNRR bi- DFC is 0): Timeout nLDFC is 1): Timeout than the TFRAME_ MAX of LIN Specif	mediately after the wake-up is een data group [3:0] bits in the l and this can be t of the RLN3nL me based on th it is set, the tim time = 49 + (nu but time = 48 + (_MAX of LIN Sp ication Packag	that area. If a bit error canceled after the s. RLN3nLDFC register calculated according TRC register is set is ne response field dat neout function stops. umber of data bytes (number of data bytes pecification Package e Revision 2.x on
	Note 2. Note 3.	data area, such as an inter- is detected during the tran- error-causing bit is sent. In a multi-byte response tr. The timeout time depends of and the checksum selection to the following formula. Th 8 data bytes. When the RT length (RFDL[3:0] bit of the [Frame timeout] On classic selection (when 1) × 14 [Tbit] On enhanced selection (when + 1) × 14 [Tbit] The aforementioned timeo Revision 1.3 on classic sele enhanced selection. [Response timeout] Timeout time = (number of Only reflection of the result disabled.	byte space, the transmis smission of a wake-up, t ansmission, bit error car on the response field dat n (the LCS bit in the RLM he time-out period until ti S bit is set, the timeout t e RLN3nLDFC register). In the CSM bit in RLN3nL hen the CSM bit in RLN3nL hen the CSM bit in RLN3 dut time is a time greater lection, or the TFRAME_ f data bytes + 1) × 14 [Th t to the SFER flag can b performed upon comple	asion is canceled im the transmission of the detected betwe a length (the RFDL I3nLDFC register), the RTS or LNRR bi- ime is reset to the ti When the LNRR bi- DFC is 0): Timeout nLDFC is 1): Timeout than the TFRAME_ MAX of LIN Specif bit] e enabled/disabled	mediately after the wake-up is een data group: [3:0] bits in the l and this can be t of the RLN3nL me based on th it is set, the tim time = 49 + (nu but time = 49 + (nu but time = 48 + (_MAX of LIN Sp ication Packag	that area. If a bit error canceled after the s. RLN3nLDFC register e calculated according TRC register is set is ne response field dat neout function stops. umber of data bytes (number of data bytes pecification Package e Revision 2.x on n cannot be enabled



6. User's Manual Update: P1L-C

Section 16 LIN/UART Interface (RLIN3)

16.3 Registers

16.3.2 LIN Master Related Registers

16.3.2.10 RLN3nLEDE – LIN Error Detection Enable Register

FTERE Bit (Timeout Error Detection Enable)

The FTERE bit enables or disables detection of the frame timeout error or the response timeout error. With 0 set, the frame timeout error or response timeout error is not detected. With 1 set, the frame timeout error or response timeout error is detected. When this bit is set to 1, the detection result is indicated in the FTER flag in the RLN3nLEST register. With the LTES bit, either the frame timeout error or response timeout error can be selected. Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received. For details on the timeout error, see **Section 16.5.3.7**, **Error Status**. Timeout error should be disabled for data group communication.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 16.4**

16.3.2.11 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode. With 0 set, LIN reset mode is caused. With 1 set, LIN reset mode is canceled. If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 16.4**.



16.3.3 LIN Slave Related Registers

16.3.3.9 RLN3nLEDE – LIN Error Detection Enable Register

TERE Bit (Timeout Error Detection Enable)

The TERE bit enables or disables detection of the frame timeout error or the response timeout error. With 0 set, the frame timeout error or response timeout error is not detected.

With 1 set, the frame timeout error or response timeout error is detected.

When this bit is set to 1, the detection result is indicated in the TER flag in the RLN3nLEST register. With the LTES bit, either the frame timeout error or response timeout error can be selected.

The timeout error should not be used in LIN slave mode [auto baud rate] (when the LMD[1:0] bits in the RLN3nLMD register are "10_B").

Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received. For details on the timeout error, see **Section 16.5.3.7**, **Error Status**.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 16.4**.

16.3.3.10 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode. With 0 set, LIN reset mode.

With 1 set, LIN reset mode is canceled.

It takes 3 peripheral clock cycles + 4 communication clock cycles, until the OMM0 bit in the RLN3nLMST register reflects the OM0 bit setting in the RLN3nLCUC register.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 16.4**



16.5 Operation

16.5.3 LIN Mode

Table 16.74	Transition	condition	for	Operation	Mode
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	Operation mode transition		Transition condition
(1)	LIN reset mode	→ LIN mode - LIN operation mode	LMD bit in RLN3nLMD register = 00_B or 10_B or 11_B and OM1 and OM0 bits in RLN3nLCUC register = 11_B
(2)	LIN reset mode	→ LIN mode - LIN wake-up mode	LMD bit in RLN3nLMD register = 00_B or 10_B or 11_B and OM1 and OM0 bits in RLN3nLCUC register = 01_B
(3) *2	LIN mode - LIN operation mode - LIN wake-up mode	→ LIN reset mode	OM0 bit in LCUC register = 0 _B
(4) *1	LIN mode - LIN operation mode	→ LIN mode - LIN wake-up mode	OM1 and OM0 bits in RLN3nLCUC register = 01B
(5) *1	LIN mode - LIN wake-up mode	→ LIN mode - LIN operation mode	OM1 and OM0 bits in RLN3nLCUC register = 11 _B

Note 1. Transition between LIN operation mode and LIN wake-up mode cannot be made when communication is going on (when the FTS bit in the RLN3nLTRC register is 1).

Note 2. In LIN mode, if RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1 or RLN3nLEDE.TERE =1), users should take the procedure shown in **Figure 16.4**. The procedure is to protect a RLIN3 error interrupt and clear a RLIN3 error interrupt request.





Figure 16.4 LIN reset sequence by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used

Note 1. This "n" value means interrupt number. See Section 16.1.4, Interrupt Requests and confirm interrupt numbers of RLIN3n status interrupt (n = 0 to 5) in Table 16.6. For EICn, refer to Section 6, Interrupts.



16.5.3.7 Error Status

(1) LIN Master Mode

Table 16.84	Types	of Error	Statuses	in LIN	Master	Mode
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Status	Error detecti	on condition	Operation mode capable of error detection	Commu nication	Enable/ disable detection	Corresponding bit
Bit error		ed data and the data on the LIN d by the receive pin do not match	LIN operation modeLIN wake-up mode	Cancel	Enabled	BER flag in RLN3nLEST register
Physical bus error	sending a		LIN operation modeLIN wake-up mode	Cancel	Enabled	PBER flag in RLN3nLEST register
	sending a	s detected to be low level when break delimiter s detected to be high level when				
	sending a	-				
Timeout error		sponse transmission/reception ninate within a given time ^{*3} *4	LIN operation mode	Cancel	Enabled	FTER flag in RLN3nLEST register
Framing error	In response fi data byte is lo	ield reception, a stop bit of each ow level	LIN operation mode	Cancel	Enabled	FER flag in RLN3nLEST register
Checksum error		ield reception, the result of st gives an error	LIN operation mode	_	Disabled	CSER flag in RLN3nLEST register
Response preparation error		llowing conditions occurs in frame de during a multi-byte response	LIN operation mode	Cancel	Disabled	RPER flag in RLN3nLEST register
	completio before a r request is • The first r the compl reception	eception data byte is received after n of header transmission but response transmission/reception a set eception data byte is received after letion of previous data group before a transmission/reception or another data group is set.				
	Note 1. Note 2.	If a bit error is detected, the proce data area, such as an inter-byte sp is detected during the transmission error-causing bit is sent. In a multi-byte response transmis	pace, the transmission is cance on of a wake-up, the transmiss	eled immedi sion of the v	iately after th vake-up is ca	at area. If a bit en anceled after the
	Note 3.	The timeout time depends on the i and the checksum selection (the (to the following formula: [Frame timeout] On classic selection (when the C + 1) × 14 [Tbit] On enhanced selection (when the bytes + 1) × 14 [Tbit]	CSM bit in the RLN3nLDFC reg	gister), and t	this can be ca e = 49 + (nun	alculated accordin
		The aforementioned timeout time	is a time greater than the TFI	RAME_MAX	X of LIN Spe	cification Package
		Revision 1.3 on classic selection enhanced selection.	n, or the TFRAME_MAX of LI	N Specifica	ation Packag	e Revision 2.x o
		[Response timeout] Timeout time = (number of data	bytes + 1) × 14 [Tbit]			
	Note 4.	If RLIN3 transitions to LIN reset ((RLN3nLEDE.FTERE = 1), users	· · · ·			eout function is us



(2) LIN Slave Mode

Table 16.85	Types of Error \$	Statuses in	LIN	Slave Mode

Status	Error data stim	condition	Operation mode capable of error	Communication	Enable/ disable	Corrosponding
Status Bit error	Error detection The transmitted of	data and the data on the LIN	LIN operation mode	Cancel	detection Enabled	Corresponding bit BER flag in BLN2-LECT
	-2	the receive pin do not match*1	 LIN wake-up mode 			RLN3nLEST register
Fimeout error		nse transmission/reception te within a given time ^{*3*6}	LIN operation mode	Cancel	Enabled	TER flag in RLN3nLEST register
Framing error	In response field data byte is low l	reception, a stop bit of each evel	LIN operation mode	Cancel	Enabled	FER flag in RLN3nLEST register
Sync field error	the width set by t	break low level is greater than he LBLT bit in the RLN3nLBFC sync field is not 55 _H	LIN operation mode	Cancel	Enabled ^{*4}	SFER flag in RLN3nLEST register
Checksum error	In response field checksum test gi	reception, the result of ves an error	LIN operation mode	*5	Disabled	CSER flag in RLN3nLEST register
ID parity error		parity bit does not match the matically calculated by the LIN/	LIN operation mode	Cancel	Enabled	IPER flag in RLN3nLEST register
Response preparation error	first reception response pre Before the co reception dat in a multi-byt	eption of a header, before the n data byte is received, eparation is not made in time. ompletion of receiving the first ta byte for the next data group is response reception, eparation for the next group is time	LIN operation mode	Cancel	Disabled	RPER flag in RLN3nLEST register
	Note 1.	If a bit error is detected, th data area, such as an inter-	byte space, the transmis	ssion is canceled im	mediately after	
	Note 2.	is detected during the tran error-causing bit is sent. In a multi-byte response tr	ansmission, bit error car	n be detected betw	een data group	S.
	Note 2. Note 3.	error-causing bit is sent.	ansmission, bit error car on the response field dat n (the LCS bit in the RLM ne time-out period until to S bit is set, the timeout t	n be detected betw a length (the RFDL V3nLDFC register), he RTS or LNRR bi ime is reset to the ti	een data group [3:0] bits in the and this can be t of the RLN3nl me based on th	s. RLN3nLDFC register e calculated according LTRC register is set is he response field data
		error-causing bit is sent. In a multi-byte response to The timeout time depends and the checksum selection to the following formula. The 8 data bytes. When the RT	ansmission, bit error car on the response field dat n (the LCS bit in the RLM ne time-out period until ti S bit is set, the timeout t e RLN3nLDFC register).	n be detected betw a length (the RFDL V3nLDFC register), he RTS or LNRR bi ime is reset to the t When the LNRR b DFC is 0): Timeout	een data group [3:0] bits in the and this can be t of the RLN3nl me based on th it is set, the tim time = 49 + (no	s. RLN3nLDFC register e calculated according LTRC register is set is he response field data neout function stops.
		error-causing bit is sent. In a multi-byte response tr The timeout time depends and the checksum selection to the following formula. Th 8 data bytes. When the RT length (RFDL[3:0] bit of the [Frame timeout] On classic selection (when 1) × 14 [Tbit] On enhanced selection (when	ansmission, bit error car on the response field dat n (the LCS bit in the RLN re time-out period until the S bit is set, the timeout the RLN3nLDFC register). In the CSM bit in RLN3nL hen the CSM bit in RLN3 ut time is a time greater	n be detected betw a length (the RFDL J3nLDFC register), he RTS or LNRR bi ime is reset to the t When the LNRR b DFC is 0): Timeout InLDFC is 1): Timeout than the TFRAME	een data group [3:0] bits in the and this can be t of the RLN3nl me based on th it is set, the tim time = 49 + (no but time = 48 + (_MAX of LIN S	s. RLN3nLDFC register e calculated according LTRC register is set is he response field data neout function stops. umber of data bytes (number of data bytes pecification Package
		error-causing bit is sent. In a multi-byte response tr The timeout time depends and the checksum selectio to the following formula. Th 8 data bytes. When the RT length (RFDL[3:0] bit of the [Frame timeout] On classic selection (when 1) × 14 [Tbit] On enhanced selection (wh + 1) × 14 [Tbit] The aforementioned timeo Revision 1.3 on classic sel	ansmission, bit error car on the response field dat n (the LCS bit in the RLN re time-out period until ti S bit is set, the timeout t e RLN3nLDFC register). In the CSM bit in RLN3nL hen the CSM bit in RLN3 ut time is a time greater lection, or the TFRAME_	h be detected betw a length (the RFDL I3nLDFC register), he RTS or LNRR bi ime is reset to the t When the LNRR b DFC is 0): Timeout InLDFC is 1): Timeout than the TFRAME _MAX of LIN Specif bit]	een data group [3:0] bits in the and this can be t of the RLN3nl me based on th it is set, the tim time = 49 + (no but time = 48 + (_MAX of LIN Spi ication Packag	s. RLN3nLDFC register e calculated according LTRC register is set is he response field data neout function stops. umber of data bytes (number of data bytes pecification Package e Revision 2.x on
	Note 3.	error-causing bit is sent. In a multi-byte response tr The timeout time depends and the checksum selectio to the following formula. Th 8 data bytes. When the RT length (RFDL[3:0] bit of the [Frame timeout] On classic selection (when 1) × 14 [Tbit] On enhanced selection (when + 1) × 14 [Tbit] The aforementioned timeo Revision 1.3 on classic sele enhanced selection. [Response timeout] Timeout time = (number of Only reflection of the result disabled.	ansmission, bit error car on the response field dat n (the LCS bit in the RLN the time-out period until the S bit is set, the timeout the RLN3nLDFC register). In the CSM bit in RLN3nL then the CSM bit in RLN3 out time is a time greater findata bytes + 1) × 14 [The t to the SFER flag can be performed upon complet	h be detected betwi a length (the RFDL I3nLDFC register), he RTS or LNRR bi ime is reset to the ti When the LNRR b DFC is 0): Timeout anLDFC is 1): Timeout than the TFRAME, MAX of LIN Specif bit] he enabled/disabled	een data group [3:0] bits in the and this can be t of the RLN3nl me based on th it is set, the tim time = 49 + (no but time = 48 + (_MAX of LIN S) ication Packag	s. RLN3nLDFC register e calculated according LTRC register is set is he response field data neout function stops. umber of data bytes - (number of data bytes pecification Package le Revision 2.x on



7. User's Manual Update: P1x

Section 16 LIN/UART Interface (RLIN3)

16.3 Registers

16.3.2.10 RLN3nLEDE – LIN Error Detection Enable Register

FTERE Bit (Timeout Error Detection Enable)

The FTERE bit enables or disables detection of the frame timeout error or the response timeout error. With 0 set, the frame timeout error or response timeout error is not detected. With 1 set, the frame timeout error or response timeout error is detected. When this bit is set to 1, the detection result is indicated in the FTER flag in the RLN3nLEST register. With the LTES bit, either the frame timeout error or response timeout error can be selected. Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received.

For details on the timeout error, see Section 16.7.6, Error Status.

Timeout error should be disabled for data group communication.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 16.4**.

16.3.2.11 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode. With 0 set, LIN reset mode is caused.

With 1 set, LIN reset mode is canceled.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 16.4**.



16.7 LIN Mode

Table 16.58 Transition Condition for Operation Mode

	Operation mode transition		Transition condition
(1)	LIN reset mode	→ LIN mode - LIN operation mode	LMD bit in RLN3nLMD register = 00_B or 10_B or 11_B and OM1 and OM0 bits in RLN3nLCUC register = 11_B
(2)	LIN reset mode	→ LIN mode - LIN wake-up mode	LMD bit in RLN3nLMD register = 00_B or 10_B or 11_B and OM1 and OM0 bits in RLN3nLCUC register = 01_B
(3) *2	LIN mode - LIN operation mode - LIN wake-up mode	→ LIN reset mode	OM0 bit in LCUC register = 0 _B
(4) *1	LIN mode - LIN operation mode	→ LIN mode - LIN wake-up mode	OM1 and OM0 bits in RLN3nLCUC register = 01 _B
(5) *1	LIN mode - LIN wake-up mode	→ LIN mode - LIN operation mode	OM1 and OM0 bits in RLN3nLCUC register = 11 _B

Note 1. Transition between LIN operation mode and LIN wake-up mode cannot be made when communication is going on (when the FTS bit in the RLN3nLTRC register is 1).

Note 2. In LIN mode, if RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1 or RLN3nLEDE.TERE =1), users should take the procedure shown in **Figure 16.4**. The procedure is to protect a RLIN3 error interrupt and clear a RLIN3 error interrupt request.





Figure 16.4 LIN reset sequence by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used

Note 1. This "n" value means interrupt number. See Section 16.1.4, Interrupt Requests and confirm interrupt numbers of RLIN3n status interrupt (n = 0 to 5) in Table 16.6. For EICn, refer to Section 6, Interrupts.



16.7.6 Error Status

16.7.6.1 LIN Master Mode

	_					
Table 16.63	Types	of Error	Statuses	IN LIN	Master	Mode

and the data on the LIN receive pin do not match d to be high level when elimiter d to be high level when p ransmission/reception thin a given time ^{*3*4} ption, a stop bit of each	LIN operation mode LIN wake-up mode LIN operation mode LIN wake-up mode LIN wake-up mode	Cancel	Enabled	BER flag in RLN3nLEST register PBER flag in RLN3nLEST register	
d to be low level when elimiter d to be high level when p ransmission/reception thin a given time ^{*3 *4}	LIN wake-up mode		Enabled	RLN3nLEST	
elimiter d to be high level when p ransmission/reception thin a given time ^{*3 *4}	LIN operation mode	Ormani		register	
p ransmission/reception thin a given time ^{*3} *4	LIN operation mode	Onest			
thin a given time ^{*3} * ⁴	LIN operation mode	0			
otion, a stop bit of each		Cancel	Enabled	FTER flag in RLN3nLEST register	
	LIN operation mode	Cancel	Enabled	FER flag in RLN3nLEST register	
ption, the result of an error	LIN operation mode	-	Disabled	CSER flag in RLN3nLEST register	
onditions occurs in frame g a multi-byte response	LIN operation mode	Cancel	Disabled	RPER flag in RLN3nLEST register	
data byte is received after der transmission but transmission/reception					
request is set • The first reception data byte is received after the completion of previous data group reception before a transmission/reception request for another data group is set.					
te 1. If a bit error is detected, the process is canceled after a stop bit is sent. If a bit error is detected in a non- data area, such as an inter-byte space, the transmission is canceled immediately after that area. If a bit error is detected during the transmission of a wake-up, the transmission of the wake-up is canceled after the space protected in the space.					
error-causing bit is sent. In a multi-byte response transmission, bit errors are detected also between data groups. The timeout time depends on the response field data length (the RFDL [3:0] bits in the RLN3nLDFC register and the checksum selection (the CSM bit in the RLN3nLDFC register), and this can be calculated according to the following formula: [Frame timeout] On classic selection (when the CSM bit in RLN3nLDFC is 0): Timeout time = 49 + (number of data bytes + 1) × 14 [Tbit] On enhanced selection (when the CSM bit in RLN3nLDFC is 1): Timeout time = 48 + (number of data bytes + 1) × 14 [Tbit]					
prementioned timeout time	e is a time greater than the TF n, or the TFRAME_MAX of L	-		-	
on 1.3 on classic selectior ced selection.					
ced selection. onse timeout]	bytes + 1) × 14 [Tbit]		vhen the time	out function is	
	onse timeout]	ut time = (number of data bytes + 1) × 14 [Tbit]	ut time = (number of data bytes + 1) × 14 [Tbit]	-	



8. User's Manual Update: P1M-E

Section 16 LIN/UART Interface (RLIN3)

16.3 Registers

16.3.2.10 RLN3nLEDE – LIN Error Detection Enable Register

FTERE Bit (Timeout Error Detection Enable)

The FTERE bit enables or disables detection of the frame timeout error or the response timeout error. With 0 set, the frame timeout error or response timeout error is not detected. With 1 set, the frame timeout error or response timeout error is detected. When this bit is set to 1, the detection result is indicated in the FTER flag in the RLN3nLEST register. With the LTES bit, either the frame timeout error or response timeout error can be selected. Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received. For details on the timeout error, see **Section 16.7.6**, **Error Status**.

Timeout error should be disabled for data group communication.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 16.4**.

16.3.2.11 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode. With 0 set, LIN reset mode is caused. With 1 set, LIN reset mode is canceled.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 16.4**.



16.7 LIN Mode

• Table 16.59 Transition Condition for Operation Mode

	Operation mode transition		Transition condition
(1)	LIN reset mode	→ LIN mode - LIN operation mode	LMD bit in RLN3nLMD register = 00_B or 10_B or 11_B and OM1 and OM0 bits in RLN3nLCUC register = 11_B
(2)	LIN reset mode	→ LIN mode - LIN wake-up mode	LMD bit in RLN3nLMD register = 00_B or 10_B or 11_B and OM1 and OM0 bits in RLN3nLCUC register = 01_B
(3) *2	LIN mode - LIN operation mode - LIN wake-up mode	→ LIN reset mode	OM0 bit in LCUC register = 0 _B
(4) *1	LIN mode - LIN operation mode	→ LIN mode - LIN wake-up mode	OM1 and OM0 bits in RLN3nLCUC register = 01 _B
(5) *1	LIN mode - LIN wake-up mode	→ LIN mode - LIN operation mode	OM1 and OM0 bits in RLN3nLCUC register = 11 _B

Note 1. Transition between LIN operation mode and LIN wake-up mode cannot be made when communication is going on (when the FTS bit in the RLN3nLTRC register is 1).

Note 2. In LIN mode, if RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1 or RLN3nLEDE.TERE =1), users should take the procedure shown in **Figure 16.4**. The procedure is to protect a RLIN3 error interrupt and clear a RLIN3 error interrupt request.





Note 1. This "n" value means interrupt number. See Section 16.1.4, Interrupt Requests and confirm interrupt numbers of

RLIN3n status interrupt (n = 0 to 5) in Table 16.7. For EICn, refer to Section 6, Interrupts.


16.7.6 Error Status

16.7.6.1 LIN Master Mode

Status	Error detection	on condition	Operation mode capable of error detection	Commu nication	Enable/ disable detection	Corresponding bit		
Bit error		ed data and the data on the LIN I by the receive pin do not match	LIN operation modeLIN wake-up mode	Cancel	Enabled	BER flag in RLN3nLEST register		
Physical bus error	sending a LIN bus is sending a 	detected to be high level when break detected to be low level when break delimiter detected to be high level when	LIN operation mode Cancel Enabled PB LIN wake-up mode RLI reg					
Timeout	sending a	wake-up sponse transmission/reception	LIN operation mode	Cancel	Enabled	FTER flag in		
error		inate within a given time ^{*3} *4	Lint operation mode	Gancer	Enabled	RLN3nLEST register		
Framing error	In response fi data byte is lo	eld reception, a stop bit of each w level	LIN operation mode	Cancel	Enabled	FER flag in RLN3nLEST register		
Checksum error		eld reception, the result of t gives an error	LIN operation mode	_	Disabled	CSER flag in RLN3nLEST register		
Response preparation error	combined more reception: • The first re completion before a re request is • The first re the comple reception	lowing conditions occurs in frame de during a multi-byte response ecception data byte is received after n of header transmission but esponse transmission/reception set ecception data byte is received after etion of previous data group before a transmission/reception r another data group is set.	LIN operation mode	Cancel	Disabled	RPER flag in RLN3nLEST register		
	Note 1. Note 2. Note 3.	is detected during the transmissionerror-causing bit is sent. In a multi-byte response transmiss The timeout time depends on the mand the checksum selection (the C to the following formula: [Frame timeout] On classic selection (when the Cs + 1) × 14 [Tbit] On enhanced selection (when the bytes + 1) × 14 [Tbit]	space, the transmission is canceled immediately after that area. If a bit sion of a wake-up, the transmission of the wake-up is canceled after t nission, bit errors are detected also between data groups. e response field data length (the RFDL [3:0] bits in the RLN3nLDFC reg e CSM bit in the RLN3nLDFC register), and this can be calculated acco CSM bit in RLN3nLDFC is 0): Timeout time = 49 + (number of data by he CSM bit in RLN3nLDFC is 1): Timeout time = 48 + (number of data ne is a time greater than the TFRAME_MAX of LIN Specification Pack					
		Revision 1.3 on classic selection enhanced selection. [Response timeout] Timeout time = (number of data		N Specifica	ition Packag	e Revision 2.x o		
	Note 4.	If RLIN3 transitions to LIN reset r (RLN3nLEDE.FTERE = 1), users	node by clearing RLN3nLCUC			out function is us		



9. User's Manual Update: E2x-FCC1, E2M

Section 19 LIN/UART Interface (RLIN3)

19.3 Registers

19.3.2 LIN Master Related Registers

19.3.2.10 RLN3nLEDE – LIN Error Detection Enable Register

FTERE Bit (Timeout Error Detection Enable)

The FTERE bit enables or disables detection of the frame timeout error or the response timeout error. With 0 set, the frame timeout error or response timeout error is not detected.

With 1 set, the frame timeout error or response timeout error is detected.

When this bit is set to 1, the detection result is indicated in the FTER flag in the RLN3nLEST register. With the LTES bit, either the frame timeout error or response timeout error can be selected.

Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received. For details on the timeout error, see **Section 19.5.3.7**, **Error Status**.

Timeout error should be disabled for data group communication.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 19.4**.

19.3.2.11 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode. With 0 set, LIN reset mode is caused. With 1 set, LIN reset mode is canceled. If RLIN3 transitions to LIN reset mode by clearing RLN3pl CLIC OM0 to 0 when the timeout function i

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 19.4**.



19.3.3 LIN Slave Related Registers

19.3.3.9 RLN3nLEDE – LIN Error Detection Enable Register

TERE Bit (Timeout Error Detection Enable)

The TERE bit enables or disables detection of the frame timeout error or the response timeout error. With 0 set, the frame timeout error or response timeout error is not detected. With 1 set, the frame timeout error or response timeout error is detected. When this bit is set to 1, the detection result is reflected in the TER flag in the RLN3nLEST register. With the LTES bit, either the frame timeout error or response timeout error can be selected. The timeout error should not be used in LIN slave mode [auto baud rate] (when the LMD[1:0] bits in the RLN3nLMD register are "10_B"). Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received. For details on the timeout error, see **Section 19.5.3.7, Error Status**. If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 19.4**.

19.3.3.10 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode. With 0 set, LIN reset mode. With 1 set, LIN reset mode is canceled.

It takes 3 peripheral clock cycles + 4 communication clock cycles, until the OMM0 bit in the RLN3nLMST register reflects the OM0 bit setting in the RLN3nLCUC register.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 19.4**.



19.5 Operation

19.5.3 LIN Mode

Table 19.76 Transition Condition for Operation Mode

	Operation Mode Transition			Transition Condition
(1)	LIN reset mode	→	LIN mode LIN operation mode	LMD bits in RLN3nLMD register = 00_B or 10_B or 11_B and OM1 and OM0 bits in RLN3nLCUC register = 11_B
(2)	LIN reset mode	→	LIN mode LIN wake-up mode 	LMD bits in RLN3nLMD register = 00_B or 10_B or 11_B and OM1 and OM0 bits in RLN3nLCUC register = 01_B
(3) *2	LIN mode LIN operation mode LIN wake-up mode	→	LIN reset mode	OM0 bit in RLN3nLCUC register = 0 ₈
(4) *1	LIN mode LIN operation mode	→	LIN mode • LIN wake-up mode	OM1 and OM0 bits in RLN3nLCUC register = 01_B
(5) *1	LIN mode LIN wake-up mode 	→	LIN mode LIN operation mode	OM1 and OM0 bits in RLN3nLCUC register = 11_B

Note 1. Transition between LIN operation mode and LIN wake-up mode cannot be made when communication is in progress (when the FTS bit in the RLN3nLTRC register is 1).

Note 2. In LIN mode, if RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1 or RLN3nLEDE.TERE =1), users should take the procedure shown in **Figure 19.4**. The procedure is to protect a RLIN3 error interrupt and clear a RLIN3 error interrupt request.





Figure 19.4 LIN reset sequence by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used

Note 1. This "n" value means interrupt number. See Section 19.1.4, Interrupt Requests and confirm interrupt numbers of RLIN3n status interrupt (n = 0 to 5) in Table 19.6. For EICn, refer to Section 6, Interrupts.



19.5.3.7 Error Status

(1) LIN Master Mode

Table 19.86 Types of Error Statuses in LIN Master Mode

Status	Error Detection Condition	Operation Mode Capable of Error Detection	Commun ication	Enable/ Disable Detection	Corresponding Bit						
Bit error	The transmitted data and the data on the LIN bus monitored by the receive pin do not match *1.42	LIN operation mode LIN wake-up mode	Cancel	Enabled	BER flag in RLN3nLEST register						
Physical bus erro	 break LIN bus detected a low level when sending a break delimiter LIN bus detected a high level when sending 	 LIN wake-up mode 	Cancel	Enabled	PBER flag in RLN3nLEST register						
Timeout error	wake-up t A frame or response transmission/reception is not completed within a given time* ^{3*4}	LIN operation mode	Cancel	Enabled	FTER flag in RLN3nLEST register						
Framing error	In response field reception, a stop bit of each data byte is low level	LIN operation mode	Cancel	Enabled	FER flag in RLN3nLEST register						
Checksu error	In response field reception, the result of checksum indicates an error	LIN operation mode	_	Disabled	CSER flag in RLN3nLEST register						
Respons preparat error			Cancel	Disabled	RPER flag in RLN3nLEST register						
Note 1.	If a bit error is detected, processing is stopped after										
	inter-byte space, the transmission is suspended imm during the transmission of a wake-up, the transmiss	-									
Note 2	In a multi-byte response transmission, bit errors are	-		i on outdoining i							
Note 2.		-		LDFC registe	er) and the						
Note 3.	The timeout time depends on the response field data length (the RFDL [3:0] bits in the RLN3nLDFC register) and the checksum selection (the CSM bit in the RLN3nLDFC register), and can be calculated from the following formula.										
Note 3.	checksum selection (the CSM bit in the RLN3nLDF(C register), and can be calculat		following for	rmula.						
Note 3.	checksum selection (the CSM bit in the RLN3nLDF(When the FSM bit in the RLN3nLDFC registers is 1		ed from the	-							
Note 3.	When the FSM bit in the RLN3nLDFC registers is 1 RTS bit of the RLN3nLTRC register is set. Once the response field data length (the RFDL[3:0] bits in the	(frame separation mode), the t RTS bit is set, the timeout time	ed from the imeout time	is that for ei	ight bytes until th						
Note 3.	When the FSM bit in the RLN3nLDFC registers is 1 RTS bit of the RLN3nLTRC register is set. Once the	(frame separation mode), the t e RTS bit is set, the timeout time RLN3nLDFC register). 3nLDFC is 0): Timeout time = 4	ed from the imeout time e is re-set to 19 + (numbe	is that for eitor the time ba	ight bytes until th ised on the tes + 1) × 14 [Tbi						
Note 3.	When the FSM bit in the RLN3nLDFC registers is 1 RTS bit of the RLN3nLTRC register is set. Once the response field data length (the RFDL[3:0] bits in the [Frame timeout] When classic is selected (when the CSM bit in RLN When enhanced is selected (when the CSM bit in R [Tbit] The aforementioned timeout time is a time longer th classic is selected, or the TFRAME_MAX of LIN Sp [Response timeout]	(frame separation mode), the t RTS bit is set, the timeout time RLN3nLDFC register). 3nLDFC is 0): Timeout time = 4 LN3nLDFC is 1): Timeout time han the TFRAME_MAX of LIN 3 recification Package Revision 2	ed from the imeout time e is re-set to 49 + (numbe = 48 + (nur Specification	is that for ei o the time ba er of data byt mber of data n Package R	ight bytes until th ised on the tes + 1) × 14 [Tbi bytes + 1) × 14 Revision 1.3 wher						
Note 3.	When the FSM bit in the RLN3nLDFC registers is 1 RTS bit of the RLN3nLTRC register is set. Once the response field data length (the RFDL[3:0] bits in the [Frame timeout] When classic is selected (when the CSM bit in RLN When enhanced is selected (when the CSM bit in R [Tbit] The aforementioned timeout time is a time longer th classic is selected, or the TFRAME_MAX of LIN Sp	(frame separation mode), the t RTS bit is set, the timeout time RLN3nLDFC register). 3nLDFC is 0): Timeout time = 4 LN3nLDFC is 1): Timeout time han the TFRAME_MAX of LIN 9 ecification Package Revision 2	ed from the imeout time e is re-set to 49 + (numbe = 48 + (nur Specification	is that for ei o the time ba er of data byt mber of data n Package R	ight bytes until th ised on the tes + 1) × 14 [Tbi bytes + 1) × 14 Revision 1.3 wher						
Note 3.	When the FSM bit in the RLN3nLDFC registers is 1 RTS bit of the RLN3nLTRC register is set. Once the response field data length (the RFDL[3:0] bits in the [Frame timeout] When classic is selected (when the CSM bit in RLN When enhanced is selected (when the CSM bit in RLN The aforementioned timeout time is a time longer the classic is selected, or the TFRAME_MAX of LIN Sp [Response timeout] Timeout time = (number of data bytes + 1) × 14 [Tb When an error is detected, the timeout error detection	(frame separation mode), the t RTS bit is set, the timeout time RLN3nLDFC register). 3nLDFC is 0): Timeout time = 4 LN3nLDFC is 1): Timeout time han the TFRAME_MAX of LIN 3 ecification Package Revision 2 it] on function stops.	ed from the imeout time e is re-set to 49 + (numbe = 48 + (num Specification 2.x when enl	is that for ei o the time ba er of data byt mber of data n Package R hanced is se	ight bytes until th ised on the tes + 1) × 14 [Tbi bytes + 1) × 14 levision 1.3 when lected.						



(2) LIN Slave Mode

Table 19.87	Types	of Error	Statuses i	n L IN	Slave	Mode
Table 13.07	i ypes		Statuses I		Jave	would

Status	Error Detection Condition	Operation Mode Capable of Error Detection	Communication	Enable/Disable Detection	Corresponding Bit
Bit error	The transmitted data and the data on the LIN bus monitored by the receive pin do not match* ¹⁺²	LIN operation mode LIN wake-up mode	Cancel	Enabled	BER flag in RLN3nLEST register
Timeout error	A frame or response transmission/reception is not completed within a given time*3 '6	LIN operation mode	Cancel	Enabled	TER flag in RLN3nLEST register
Framing error	In frame reception, a stop bit of each data byte is low level	LIN operation mode	Cancel	Enabled	FER flag in RLN3nLEST register
Sync field error	If the width of the break low level is greater than the width set by the LBLT bit in the RLN3nLBFC register and the sync field is not $55_{\rm H}$	LIN operation mode	Cancel	Enabled ¹⁴	SFER flag in RLN3nLEST register
Checksum error	In response field reception, the result of checksum indicates an error	LIN operation mode	*5	Disabled	CSER flag in RLN3nLEST register
ID parity error	If the received ID parity bit does not match the value that is automatically calculated by the LIN/UART interface	LIN operation mode	Cancel	Enabled	IPER flag in RLN3nLEST register
Response preparation error	 After the reception of a header, response preparation is not completed in time before the first byte of reception data is received 	LIN operation mode	Cancel	Disabled	RPER flag in RLN3nLEST register
	 In multi-byte response reception, the reception preparation for the next data group is not completed in time before the first byte of the next data group reception data is received. 				

Note 1. If a bit error is detected, processing is stopped after a stop bit is sent. If a bit error is detected in a non-data area, such as an inter-byte space, the transmission is suspended immediately after the bit which had the error is sent. If a bit error is detected during the transmission of a wake-up, the transmission of the wake-up is canceled after the error-causing bit is sent.

Note 2. In a multi-byte response transmission, bit errors are also detected between data groups.

Note 3. The timeout time depends on the response field data length (the RFDL [3:0] bits in the RLN3nLDFC register) and the checksum selection (the LCS bit in the RLN3nLDFC register), and this can be calculated according to the following formula. The timeout period until the RTS or LNRR bit of the RLN3nLTRC register is set is 8 data bytes. When the RTS bit is set, the timeout time is reset to the time based on the response field data length (RFDL[3:0] bits of the RLN3nLDFC register). When the LNRR bit is set, the timeout function stops.

[Frame timeout]

When classic is selected (when the LCS bit in RLN3nLDFC is 0): Timeout time = 49 + (number of data bytes + 1) × 14 [Tbit] When enhance is selected (when the LCS bit in RLN3nLDFC is 1): Timeout time = 48 + (number of data bytes + 1) × 14 [Tbit] The aforementioned timeout time is a time longer than the TFRAME_MAX of LIN Specification Package Revision 1.3 when classic is selected, or the TFRAME_MAX of LIN Specification Package Revision 2.x when enhanced is selected.

[Response timeout]

Timeout time = (number of data bytes + 1) × 14 [Tbit]

When an error is detected, timeout error detection function stops.

- Note 4. Only reflection of the result to the SFER flag can be enabled/disabled. Error detection cannot be enabled/disabled.
- Note 5. Checksum judgment is performed upon completion of response frame reception. In case of an error, the successful reception flag is not set to 1.

Note 6. If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 19.4**.



10. User's Manual Update: E2x-FCC2, E2UH, E2H

Section 20 LIN/UART Interface (RLIN3)

20.3 Registers

20.3.2 LIN Master Related Registers

20.3.2.10 RLN3nLEDE – LIN Error Detection Enable Register

FTERE Bit (Timeout Error Detection Enable)

The FTERE bit enables or disables detection of the frame timeout error or the response timeout error. With 0 set, the frame timeout error or response timeout error is not detected. With 1 set, the frame timeout error or response timeout error is detected.

When this bit is set to 1, the detection result is indicated in the FTER flag in the RLN3nLEST register. With the LTES bit, either the frame timeout error or response timeout error can be selected.

Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received. For details on the timeout error, see Section 20.5.3.7, Error Status.

Timeout error should be disabled for data group communication.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 20.4**.

20.3.2.11 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode. With 0 set, LIN reset mode is caused. With 1 set, LIN reset mode is canceled. If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in Figure 20.4.



20.3.3 LIN Slave Related Registers

20.3.3.9 RLN3nLEDE – LIN Error Detection Enable Register

TERE Bit (Timeout Error Detection Enable)

The TERE bit enables or disables detection of the frame timeout error or the response timeout error. With 0 set, the frame timeout error or response timeout error is not detected. With 1 set, the frame timeout error or response timeout error is detected. When this bit is set to 1, the detection result is reflected in the TER flag in the RLN3nLEST register. With the LTES bit, either the frame timeout error or response timeout error can be selected. The timeout error should not be used in LIN slave mode [auto baud rate] (when the LMD[1:0] bits in the RLN3nLMD register are "10_B"). Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received.

For details on the timeout error, see Section 20.5.3.7, Error Status.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 20.4**.

20.3.3.10 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode.

With 0 set, LIN reset mode.

With 1 set, LIN reset mode is canceled.

It takes 3 peripheral clock cycles + 4 communication clock cycles, until the OMM0 bit in the RLN3nLMST register reflects the OM0 bit setting in the RLN3nLCUC register.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 20.4**.



20.5 Operation

20.5.3 LIN Mode

Table 20.77 Transition Condition for Operation Mode

	Operation Mode Transition	,		Transition Condition
(1)	LIN reset mode	→	LIN mode LIN operation mode 	LMD bits in RLN3nLMD register = 00_{B} or 10_{B} or 11_{B} and OM1 and OM0 bits in RLN3nLCUC register = 11_{B}
(2)	LIN reset mode	→	LIN mode • LIN wake-up mode	LMD bits in RLN3nLMD register = 00_B or 10_B or 11_B and OM1 and OM0 bits in RLN3nLCUC register = 01_B
(3) *2	LIN mode LIN operation mode LIN wake-up mode 	→	LIN reset mode	OM0 bit in RLN3nLCUC register = 0 ₈
(4) *1	LIN mode LIN operation mode 	→	LIN mode • LIN wake-up mode	OM1 and OM0 bits in RLN3nLCUC register = 01_{B}
(5) *1	LIN mode LIN wake-up mode	→	LIN mode • LIN operation mode	OM1 and OM0 bits in RLN3nLCUC register = 11 ₈

Note 1. Transition between LIN operation mode and LIN wake-up mode cannot be made when communication is in progress (when the FTS bit in the RLN3nLTRC register is 1).

Note 2. In LIN mode, if RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1 or RLN3nLEDE.TERE =1), users should take the procedure shown in **Figure 20.4**. The procedure is to protect a RLIN3 error interrupt and clear a RLIN3 error interrupt request.





Figure 20.4 LIN reset sequence by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used

Note 1. This "n" value means interrupt number. See Section 20.1.4, Interrupt Requests and confirm interrupt numbers of RLIN3n status interrupt (n = 0 to 7) in Table 20.7. For EICn, refer to Section 6, Interrupts.



20.5.3.7 Error Status

(1) LIN Master Mode

Table 20.87 Types of Error Statuses in LIN Master Mode

Status		Error Detection Condition	Operation Mode Capable of Error Detection	Commun ication	Enable/ Disable Detection	Corresponding Bit
Bit error	r	The transmitted data and the data on the LIN bus monitored by the receive pin do not match *1,*2	LIN operation mode LIN wake-up mode	Cancel	Enabled	BER flag in RLN3nLEST register
Physical bus error		 LIN bus detected a high level when sending a break LIN bus detected a low level when sending a break delimiter LIN bus detected a high level when sending a 	 LIN wake-up mode 	Cancel	Enabled	PBER flag in RLN3nLEST register
Timeout error	t	wake-up A frame or response transmission/reception is not completed within a given time*3 '4	LIN operation mode	Cancel	Enabled	FTER flag in RLN3nLEST register
Framing error]	In response field reception, a stop bit of each data byte is low level	LIN operation mode	Cancel	Enabled	FER flag in RLN3nLEST register
Checksum error		In response field reception, the result of checksum indicates an error	LIN operation mode	-	Disabled	CSER flag in RLN3nLEST register
Respon: preparat error		 One of the following conditions occurs in frame separate mode during a multi-byte response reception: After header transmission is complete, the first byte of receive data is received before a response transmission/reception request is set. After the previous data group reception is complete, the first byte of receive data is received before a transmission/reception request for the next data group is set. 	LIN operation mode	Cancel	Disabled	RPER flag in RLN3nLEST register
lote 1.	inte	bit error is detected, processing is stopped after a r-byte space, the transmission is suspended imme	ediately after the bit which ha	d the error is	s sent. If a bi	t error is detecte
Note 2.		ing the transmission of a wake-up, the transmissio a multi-byte response transmission, bit errors are a	-		ror-causing t	oit is sent.
Note 3.	che Wh RT: res [Fr: Wh	e timeout time depends on the response field data tecksum selection (the CSM bit in the RLN3nLDFC i en the FSM bit in the RLN3nLDFC registers is 1 (f S bit of the RLN3nLTRC register is set. Once the F ponse field data length (the RFDL[3:0] bits in the R ame timeout] en classic is selected (when the CSM bit in RLN3r en enhanced is selected (when the CSM bit in RLN it]	register), and can be calculat rame separation mode), the t RTS bit is set, the timeout tim RLN3nLDFC register).	ed from the imeout time e is re-set to 19 + (numbe	following for is that for ei o the time ba	mula. ght bytes until the sed on the es + 1) × 14 [Tbit
	clas [Re Tim	e aforementioned timeout time is a time longer than ssic is selected, or the TFRAME_MAX of LIN Spec sponse timeout] eout time = (number of data bytes + 1) × 14 [Tbit] en an error is detected, the timeout error detection	fication Package Revision 2.		-	
		LIN3 transitions to LIN reset mode by clearing RLN	I3nLCUC.OM0 to 0 when the	timeout fun	ction is used	



(2) LIN Slave Mode

Table 20.88	Types of Error Statuses in LIN Slave Mode
10010 20.00	Types of Enor otatuses in Env olave mode

Status	Error Detection Condition	Operation Mode Capable of Error Detection	Communication	Enable/Disable Detection	Corresponding Bit
Bit error	The transmitted data and the data on the LIN bus monitored by the receive pin do not match*1*2	LIN operation mode LIN wake-up mode	Cancel	Enabled	BER flag in RLN3nLEST register
Timeout error	A frame or response transmission/reception is not completed within a given time* ³ '6	LIN operation mode	Cancel	Enabled	TER flag in RLN3nLEST register
Framing error	In frame reception, a stop bit of each data byte is low level	LIN operation mode	Cancel	Enabled	FER flag in RLN3nLEST register
Sync field error	If the width of the break low level is greater than the width set by the LBLT bit in the RLN3nLBFC register and the sync field is not $55_{\rm H}$	LIN operation mode	Cancel	Enabled ¹⁴	SFER flag in RLN3nLEST register
Checksum error	In response field reception, the result of checksum indicates an error	LIN operation mode	*5	Disabled	CSER flag in RLN3nLEST register
ID parity error	If the received ID parity bit does not match the value that is automatically calculated by the LIN/UART interface	LIN operation mode	Cancel	Enabled	IPER flag in RLN3nLEST register
Response preparation error	 After the reception of a header, response preparation is not completed in time before the first byte of reception data is received In multi-byte response reception, the reception preparation for the next data group is not completed in time before the first byte of the next data group reception data is received. 	LIN operation mode	Cancel	Disabled	RPER flag in RLN3nLEST register

Note 1. If a bit error is detected, processing is stopped after a stop bit is sent. If a bit error is detected in a non-data area, such as an inter-byte space, the transmission is suspended immediately after the bit which had the error is sent. If a bit error is detected during the transmission of a wake-up, the transmission of the wake-up is canceled after the error-causing bit is sent.

Note 2. In a multi-byte response transmission, bit errors are also detected between data groups.

Note 3. The timeout time depends on the response field data length (the RFDL [3:0] bits in the RLN3nLDFC register) and the checksum selection (the LCS bit in the RLN3nLDFC register), and this can be calculated according to the following formula. The timeout period until the RTS or LNRR bit of the RLN3nLTRC register is set is 8 data bytes. When the RTS bit is set, the timeout time is reset to the time based on the response field data length (RFDL[3:0] bits of the RLN3nLDFC register). When the LNRR bit is set, the timeout function stops.

[Frame timeout]

When classic is selected (when the LCS bit in RLN3nLDFC is 0): Timeout time = 49 + (number of data bytes + 1) × 14 [Tbit] When enhance is selected (when the LCS bit in RLN3nLDFC is 1): Timeout time = 48 + (number of data bytes + 1) × 14 [Tbit] The aforementioned timeout time is a time longer than the TFRAME_MAX of LIN Specification Package Revision 1.3 when classic is selected, or the TFRAME_MAX of LIN Specification Package Revision 2.x when enhanced is selected.

[Response timeout]

Timeout time = (number of data bytes + 1) × 14 [Tbit]

When an error is detected, timeout error detection function stops.

- Note 4. Only reflection of the result to the SFER flag can be enabled/disabled. Error detection cannot be enabled/disabled.
- Note 5. Checksum judgment is performed upon completion of response frame reception. In case of an error, the successful reception flag is not set to 1.
- Note 6. If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 20.4**.



11. User's Manual Update: U2A-EVA, U2A16, U2A8, U2A6

Section 21 LIN/UART Interface (RLIN3)

21.3 Registers

21.3.2 LIN Master Related Registers

21.3.2.10 RLN3nLEDE – LIN Error Detection Enable Register

FTERE Bit (Timeout Error Detection Enable)

The FTERE bit enables or disables detection of the frame timeout error or the response timeout error. With 0 set, the frame timeout error or response timeout error is not detected. With 1 set, the frame timeout error or response timeout error is detected.

When this bit is set to 1, the detection result is indicated in the FTER flag in the RLN3nLEST register. With the LTES bit, either the frame timeout error or response timeout error can be selected. Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received. For details on the timeout error, see **Section 21.4.4.7**, **Error Status**.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 21.4**.

21.3.2.11 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode. With 0 set, LIN reset mode. With 1 set, LIN reset mode is canceled. If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1), users should take the procedure shown in **Figure 21.4**.



21.3.3 LIN Slave Related Registers

21.3.3.9 RLN3nLEDE – LIN Error Detection Enable Register

TERE Bit (Timeout Error Detection Enable)

The TERE bit enables or disables detection of the frame timeout error or the response timeout error. With 0 set, the frame timeout error or response timeout error is not detected. With 1 set, the frame timeout error or response timeout error is detected. When this bit is set to 1, the detection result is reflected in the TER flag in the RLN3nLEST register. With the LTES bit, either the frame timeout error or response timeout error can be selected. The timeout error should not be used in LIN slave mode [auto baud rate] (when the LMD[1:0] bits in the RLN3nLMD register are "10_B"). Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received.

Do not use the timeout error if response data of 9 bytes or more is to be transmitted or received. For details on the timeout error, see **Section 21.4.4.7**, **Error Status**.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 21.4**.

21.3.3.10 RLN3nLCUC – LIN Control Register

OM0 Bit (LIN Reset)

The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode. With 0 set, LIN/UART interface enters LIN reset mode. With 1 set, LIN reset mode of LIN/UART interface is canceled.

If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 21.4**.



21.4 Operation

21.4.4 LIN Mode

	Operation Mode Transition			Transition Condition
(1)	LIN reset mode	→	LIN mode LIN operation mode 	LMD bits in RLN3nLMD register = 00 _B or 10 _B or 11 _B and OM1 and OM0 bits in RLN3nLCUC register = 11 _B
(2)	LIN reset mode	→	LIN mode LIN wake-up mode 	LMD bits in RLN3nLMD register = 00 _B or 10 _B or 11 _B and OM1 and OM0 bits in RLN3nLCUC register = 01 _B
(3) *2	LIN mode LIN operation mode LIN wake-up mode 	→	LIN reset mode	OM0 bit in RLN3nLCUC register = 0 _B
(4) *1	LIN mode LIN operation mode 	→	LIN mode • LIN wake-up mode	OM1 and OM0 bits in RLN3nLCUC register = 01 _B
(5) *1	LIN mode • LIN wake-up mode	→	LIN mode LIN operation mode 	OM1 and OM0 bits in RLN3nLCUC register = 11 _B

Table 21.79 Transition Condition for Operation Mode

Note 1. Transition between LIN operation mode and LIN wake-up mode cannot be made when communication is in progress (when the FTS bit in the RLN3nLTRC register is 1).

Note 2. In LIN mode, if RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.FTERE = 1 or RLN3nLEDE.TERE =1), users should take the procedure shown in **Figure 21.4**. The procedure is to protect a RLIN3 error interrupt and clear a RLIN3 error interrupt request.





Figure 21.4 LIN reset sequence by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used

Note 1. This "n" value means interrupt number. See Section 21.1.4, Interrupt Requests and Error Notifications and confirm interrupt numbers of RLIN3n interrupt or RLIN3n status interrupt (n = 0 to 23) in Table 21.7 in accordance with the value of RLN3nLMD.LIOS. For EICn, refer to Section 6, Interrupts.



21.4.4.7 Error Status

(1) LIN Master Mode

Status	Error Detecti	ion Condition	Operation Mode Capable of Error Detection	Commu	Enable/ Disable Detection	Corresponding Bit		
				-				
Bit error		ed data and the data on the LIN d by the receive pin do not match	 LIN operation mode LIN wake-up mode 	Cancel	Enabled	BER flag in RLN3nLEST register		
Physical bus error	a break LIN bus de break deli 	etected a high level when sending	LIN operation mode LIN wake-up mode	Cancel	Enabled	PBER flag in RLN3nLEST register		
Timeout error	A frame or res	sponse transmission/reception is d within a given time* ^{3'4}	LIN operation mode	Cancel	Enabled	FTER flag in RLN3nLEST register		
Framing error	In response fi data byte is lo	eld reception, a stop bit of each w level	LIN operation mode	Cancel	Enabled	FER flag in RLN3nLEST register		
Checksum error		eld reception, the result of licates an error	LIN operation mode	-	Disabled	CSER flag in RLN3nLEST register		
Response preparation error	 separate mod reception: After head first byte of response set. After the p complete, received b 	lowing conditions occurs in frame le during a multi-byte response der transmission is complete, the of receive data is received before a transmission/reception request is previous data group reception is the first byte of receive data is pefore a transmission/reception or the next data group is set.	LIN operation mode	Cancel	Disabled	RPER flag in RLN3nLEST register		
	Note 2. Note 3.	area, such as an inter-byte space, error is sent. If a bit error is detecte is canceled after the error-causing In a multi-byte response transmiss The timeout time depends on the re and the checksum selection (the C following formula. When the FSM bit in the RLN3nLD bytes until the RTS bit of the RLN3 to the time based on the response [Frame timeout] When classic checksum is selected of data bytes + 1) × 14 [Tbit]	ed during the transmission of bit is sent. sion, bit errors are also detect esponse field data length (the CSM bit in the RLN3nLDFC r FC register is 1 (frame separ BnLTRC register is set. Once field data length (the RFDL)	a wake-up, i ted between RFDL [3:0] register), and ation mode), the RTS bit [3:0] bits in t	the transmiss In data groups bits in the RL d can be calc the timeout t is set, the tim he RLN3nLD	sion of the wake-u s. N3nLDFC registe ulated from the ime is that for eigh neout time is re-se FC register).		
		When enhanced checksum is selected (when the CSM bit in RLN3nLDFC is 1): Timeout time = 48 + (number of data bytes + 1) × 14 [Tbit] The aforementioned timeout time is a time longer than the TFRAME_MAX of LIN Specification Package Revision 1.3 when classic checksum is selected, or the TFRAME_MAX of LIN Specification Package Revision 2.x when enhanced checksum is selected. [Response timeout] Timeout time = (number of data bytes + 1) × 14 [Tbit] When an error is detected, the timeout error detection function stops.						



Date: Sep. 08, 2021

(2) LIN Slave Mode

Status	Error Detection Condition	Operation Mode Capable of Error Detection	Communication	Enable/ Disable Detection	Corresponding Bit
Bit error	The transmitted data and the data on the LIN bus monitored by the receive pin do not match*1 *2	LIN operation mode LIN wake-up mode	Cancel	Enabled	BER flag in RLN3nLEST register
Timeout error	A frame or response transmission/reception is not completed within a given time*3 *6	LIN operation mode	Cancel	Enabled	TER flag in RLN3nLEST register
Framing error	In frame reception, a stop bit of each data byte is low level	LIN operation mode	Cancel	Enabled	FER flag in RLN3nLEST register
Sync field error	If the width of the break low level is greater than the width set by the LBLT bit in the RLN3nLBFC register and the sync field is not $55_{\rm H}$	LIN operation mode	Cancel	Enabled ^{"4}	SFER flag in RLN3nLEST register
Checksum error	In response field reception, the result of checksum indicates an error	LIN operation mode	_ ^{*5}	Disabled	CSER flag in RLN3nLEST register
ID parity error	If the received ID parity bit does not match the value that is automatically calculated by the LIN/ UART interface	LIN operation mode	Cancel	Enabled	IPER flag in RLN3nLEST register
Response preparation error	 After the reception of a header, response preparation is not completed in time before the first byte of reception data is received. In multi-byte response reception, the reception preparation for the next data group is not completed in time before the first byte of the next data group reception data is received. 	LIN operation mode	Cancel	Disabled	RPER flag in RLN3nLEST register
	Note 1. If a bit error is detected, processing is stopped after a stop bit is sent. If a bit error is detected in a non-data area, such as an inter-byte space, the transmission is suspended immediately after the bit which had the error is sent. If a bit error is detected during the transmission of a wake-up, the transmission of the wake-up is canceled after the error-causing bit is sent.				
	Note 2. In a multi-byte response transmission, bit errors are also detected between data groups. Note 3. The timeout time depends on the response field data length (the REDI (3:0) bits in the RI N3nI DEC register				

Table 21.90 Types of Error Statuses in LIN Slave Mode

Note 3. The timeout time depends on the response field data length (the RFDL [3:0] bits in the RLN3nLDFC register) and the checksum selection (the LCS bit in the RLN3nLDFC register), and this can be calculated according to the following formula. The timeout period until the RTS or LNRR bit of the RLN3nLTRC register is set is 8 data bytes. When the RTS bit is set, the timeout time is reset to the time based on the response field data length (RFDL[3:0] bits of the RLN3nLDFC register). When the LNRR bit is set, the timeout function stops.

[Frame timeout]

When classic is selected (when the CSM bit in RLN3nLDFC is 0): Timeout time = 49 + (number of data bytes + 1) × 14 [Tbit]

When enhanced is selected (when the CSM bit in RLN3nLDFC is 1): Timeout time = 48 + (number of data bytes + 1) × 14 [Tbit]

The aforementioned timeout time is a time longer than the TFRAME_MAX of LIN Specification Package Revision 1.3 when classic is selected, or the TFRAME_MAX of LIN Specification Package Revision 2.x when enhanced is selected.

[Response timeout]

Timeout time = (number of data bytes + 1) × 14 [Tbit] When an error is detected, timeout error detection function stops.

Note 4. Only reflection of the result to the SFER flag can be enabled/disabled. Error detection cannot be enabled/ disabled.

Note 5. Checksum judgment is performed upon completion of response frame reception. In case of an error, the successful reception flag is not set to 1.

Note 6. If RLIN3 transitions to LIN reset mode by clearing RLN3nLCUC.OM0 to 0 when the timeout function is used (RLN3nLEDE.TERE = 1), users should take the procedure shown in **Figure 21.4**.



12. Judgement Flow



