To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
RenesasTechnology Corp.

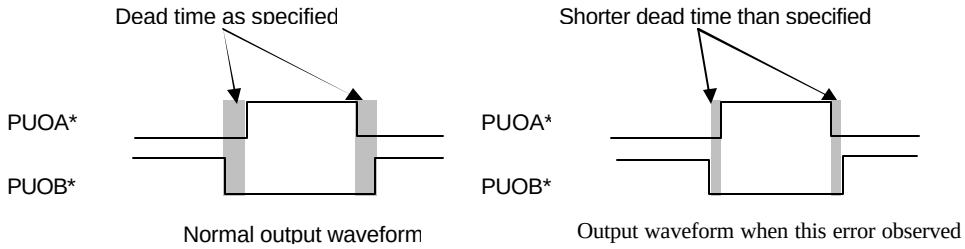
Product Category	MPU&MCU		Document No.	TN-SH7-A551A/E	Rev.	1.0
Title	Restrictions on dead time of the motor management timer (MMT) in the SH7046 Series, SH7047 Series, SH7104, SH7105, SH7106, SH7107, SH7108, and SH7109		Information Category	Technical Notification		
Applicable Product	SH7046 Series, SH7047 Series, SH7104, SH7105, SH7106, SH7107, SH7108, and SH7109	Lot No. All lots	Reference Document	SH7046 Series Hardware Manual (ADE-602-237B Rev. 3.0) SH-2 SH7047 Group Hardware Manual (REJ09B0020-0200Z Rev. 2.0)		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of the following restrictions on the dead time of the motor management timer (MMT) in the SH7046 Series, SH7047 Series, SH7104, SH7105, SH7106, SH7107, SH7108, and SH7109.

1. Phenomenon

A PWM waveform output may have a shorter dead time (non-overlap time) than the time specified by the timer dead time register (MMT_TDDR) or may have no dead time (a dead time of 0).



Normal output waveform

Output waveform when this error observed

Note:* The same error is observed for the PVOA and PVOB pins or the PWOA and PWOB pins.

2. Conditions

This error occurs when the counter is restarted (setting the CST bit in TCNR to 1) after the counter is stopped by clearing the CST bit in TCNR to 0 while the MMT repeats count up and count down.

3. Measures to Handle Error

The following three measures can be used to handle this error.

3.1 Measure A

The CST bit should not be cleared to 0 when the counter is restarted by setting the CST bit to 1. If the CST bit needs to be cleared, the CST bit should not be set to 1 after clearing.

3.2 Measure B

To set the CST bit again after clearing, follow the following procedure.

1. Specify the PWM output pin as a general input port by the pin function controller (PFC).
2. Write H'0000 to free-operation addresses of all buffer registers (TBRU, TBRV, and TBRW).
3. After the specified dead time has elapsed, write H'00 to TCNR to clear the CST bit to 0.
4. Set the CST bit to 1 to restart the counter.

3.3 Measure C

To set the CST bit again after clearing, follow the following procedure.

1. Stop the counter by clearing the CST bit in TCNR to 0.
2. Specify the PWM output pin as a general input port by the pin function controller (PFC).
3. Clear bit MSTP14 in the module standby control register 2 (MSTCR2) to 0 to enter the module standby mode. The internal states of the MMT is initialized.
4. Immediately, set bit MSTP14 to 1 to leave the module standby mode. Again, initialize the MMT and pin functions.
5. Set the CST bit to 1 to restart the counter.