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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A068A/E	Rev.	1.00
Title	Restriction regarding Watchdog timer		Information Category	Technical Notification		
Applicable Product	RL78/D1A, RL78/F12, RL78/F13, RL78/F14, RL78/F15	Lot No. _	Reference Document	Latest user's Manual of applicable products		

The restriction below applies to watchdog timer in the above mentioned Applicable Products.

1. Description

Wrong WDT-RESET may assert when WDT counter is cleared (writing 0xAC to WDTC register) at just 50% of count-overflow-value and when window open period of watchdog timer is set to 75%.

When all of following conditions is established, the restriction applies.

(1) “Operation of watchdog timer” is ”enabled” (WDTON = “1”)

(2) “Operation of watchdog timer in the HALT or STOP mode” is “enabled” (WDSTBYON = “1”)

(3) “Setting of window open period of watchdog timer” is “75%” (WINDOW1, WINDOW0 = “10b”)

(4) During watchdog timer operates, counter is cleared at just 50% of count-overflow-value (writing WDTE register to ACh).

Note: Each bit such as WDTON, WDSTBYON, WINDOW1 and WINDOW0 is a part of user option byte (000C0h)

2. Countermeasure

Please correspond with either of the following countermeasures.

1) Set “window open period” to “50%” or “100%”.

Set bit 6 and bit 5 in user option byte (000C0h) to 01b (50%) or 11b (100%)

2) If “window open period” is set to “75%” (WINDOW1, WINDOW0 = “10b”), please perform Counter- clear within the period except for just 50%.

Note

If boot swap function is used, set 020C0h (010C0h in case of RL78/F12) to same value as user option byte (000C0h).