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# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-RL*-A0096A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | Restriction regarding reading data flash memory | | Information Category | Technical Notification | | |
| Applicable Product | RL78/F12<br>RL78/F13、RL78/F14、RL78/F15<br>RL78/D1A | Lot No.<br>– | Reference Document | Latest user's Manual of applicable products | | |

The restriction below applies to above-mentioned applicable products.

**1. Description**

Applicable Usage

RL78/F13, F14, and F15 have restrictions if conditions (1) and (2) are met.

RL78/F12, D1A have restrictions if all conditions (1) to (3) are met.

Conditions:

(1) Reading data flash memory during sub-system clock or low-speed on-chip oscillator is selected as CPU/peripheral hardware clock (CLS note =1).

(2) Switch over CPU/peripheral hardware clock to main system clock after (1), reading data flash memory during main system clock is selected as CPU/peripheral hardware clock frequency (CLS =0).

(3) HS mode is selected.

OR

LS mode is selected, and CPU/peripheral hardware clock frequency is higher than 1MHz.

Note: Bit 7 of System clock control register (CKC)

Remarks: The target clock differs depending on the product.

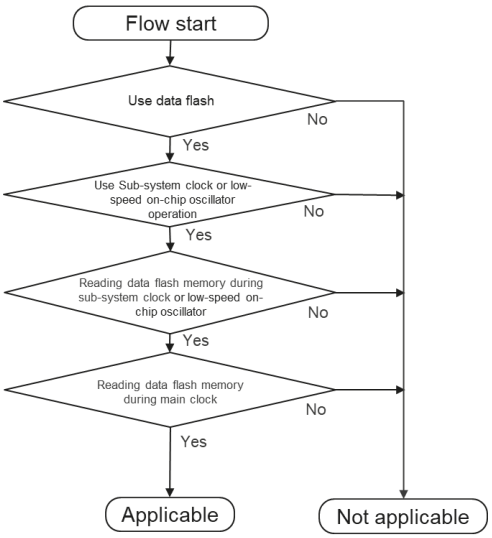
| | |
|---|---|
| RL78/F12 | Subsystem clock |
| RL78/F13, F14, F15 | Subsystem clock or low-speed on-chip oscillator |
| RL78/D1A | Subsystem clock |

Restriction

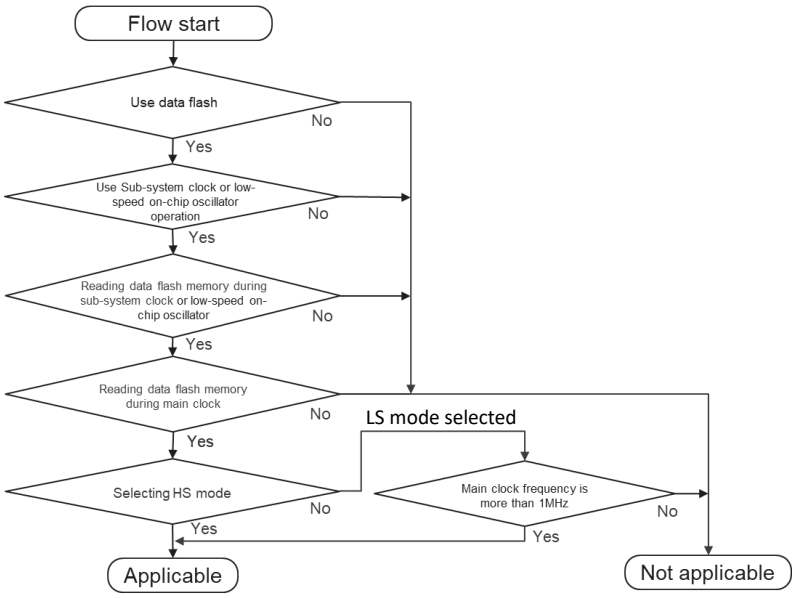
Read out data flash memory during sub-system clock or low-speed on-chip oscillator is selected as CPU/peripheral hardware clock frequency (CLS=1), the read out of the data flash memory during main system clock is selected (CLS=0), may result is wrong data.

**2. Applicable judgement flow**

RL78/F13,F14,F15 :




RL78/F12,D1A :




**3. Countermeasure**

Please apply one of the following procedures.

Countermeasure 1:

In case of switch over CPU/peripheral hardware clock from sub-system clock or low-speed on-chip oscillator to main system clock, please read data flash after executing the following procedures (1) to (3).

(1) Confirming complete switched to main system clock (CLS=0).

(2) Dummy read of any data flash memory address. (Don't use this value.)

(3) Waiting until the following time has been passed:

| | |
|---|---|
| RL78/F13,F14,F15, RL78/F12,D1A | HS (High-speed main) mode: 5 μs |
| RL78/F12,D1A | LS (Low-speed main) mode: 1 μs |

Countermeasure 2:

Please do not read data flash memory during sub-system clock or low-speed on-chip oscillator is selected as CPU/peripheral hardware clock.

If data flash content needs to be accessed during sub-system clock or low-speed on-chip oscillator is selected, please use this workaround:

Copy the required data flash content to RAM before entering sub-system clock or low-speed on-chip oscillator. Use RAM value during sub-system clock or low-speed on-chip oscillator is selected.

**4. Improvement plan**

This matter is a restriction of products.

We will describe this restriction in the next revision of user's manual of applicable products.

**5. Part numbers of applicable products**

Table 1 shows product group and part numbers of applicable products.

Table 1. Product group and part numbers of applicable products

| Product group | Parts number |
|---|---|
| RL78/F12 | R5F109xxx |
| RL78/F13 | R5F10Axxx、R5F10Bxxx |
| RL78/F14 | R5F10Pxxx |
| RL78/F15 | R5F113xxx |
| RL78/D1A | R5F10Cxxx、R5F10Dxxx、R5F10Txxx |