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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0065A/E	Rev.	1.00
Title	RA6T2 Group Correction of Register symbols and R/W attributes		Information Category	Technical Notification		
Applicable Product	RA6T2 Group	Lot No. All	Reference Document	RA6T2 Group User's Manual : Hardware Rev.1.20		

Register symbols and R/W attributes is corrected in following points.

"SVD file will be updated in the FSP version which will be released after the RA6T2 Group User's Manual: Hardware Rev.1.30 is released. (Planned in FSP 4.1.0)

1) Register Symbol

ADC

36.2.2.2 ADSGER, 36.2.2.6 ADINTCR, 36.2.2.8 ADTRGELC, 36.2.2.9 ADTRGGPT,
36.2.2.10 ADTRGENR, 36.2.3.3 ADDOPCRB, 36.2.7.1 ADLIMINTCR
36.2.7.3 ADLIMGRSR, 36.2.7.4 ADLIMCHSR0, 36.2.7.6 ADLIMGRSCR, 36.2.7.7 ADLIMCHSCR0,
36.2.8.1 ADCMPENR, 36.2.8.2 ADCMPINTCR, 36.2.8.3 ADCCMPCR, 36.2.8.7 ADCMPTBSR,
36.2.8.8 ADCMPTBSCR, 36.2.8.9 ADCMPCHSR0, 36.2.8.11 ADCMPCHSCR0,
36.2.9.2 ADSYSTR,
36.2.10.2 ADGRSR, 36.2.10.3 ADSCANENDSR, 36.2.10.4 ADSCANENDSCR, 36.2.10.10 ADOVFCHSR0,
36.2.10.13 ADOVFCHSCR0,
36.2.11.1 ADFIFOCR, 36.2.11.2 ADFIFOINTCR,
36.2.11.13 ADFIFODCR, 36.2.11.14 ADFIFOERSR, 36.2.11.15 ADFIFOERSCR

2) R/W attribute

CANFD

28.2.14 CFDGSTS, 28.2.16 CFDGTINTSTS, 28.2.17 CFDGTSC, 28.2.28 CFDRFPCTR,
28.2.31 CFDCFPCTR, 28.2.33 CFDFFSTS, 28.2.34 CFDFMSTS, 28.2.35 CFDRFISTS,
28.2.37 CFDCDTSTS, 28.2.47 CFDTXQPCTR, 28.2.51 CFDTHLACC1, 28.2.52 CFDTHLPCTR,
28.2.57 CFDGLOCKK,

DOC

40.2.2 DOSR, 40.2.3 DOSCR

[Modified]

36.2.2.2 ADSGER : Scan Group Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x048

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	SGRE8	SGRE7	SGRE6	SGRE5	SGRE4	SGRE3	SGRE2	SGRE1	SGRE0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SGRE0 to SGRE8	Scan Group n Enable The suffix number of each bit symbol corresponds to the scan group number n. 0: Disable the scan group n 1: Enable the scan group n	R/W
31:9	-	These bits are read as 0. The write value should be 0.	R/W

The ADSGER register selects the enable/disable to each scan group.

36.2.2.6 ADINTCR : Scan End Interrupt Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x05C

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	ADIE8	ADIE7	ADIE6	ADIE5	ADIE4	ADIE3	ADIE2	ADIE1	ADIE0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	ADIE0 to ADIE8	Scan Group n Scan End Interrupt Enable The suffix number of each bit symbol corresponds to the scan group number n. 0: Disable scan end interrupt 1: Enable scan end interrupt	R/W
31:9	-	These bits are read as 0. The write value should be 0.	R/W

The ADINTCR register enables/disables the scan end interrupt.

36.2.2.8 ADTRGELCn : ELC Trigger Enable Register n (n = 0 to 8)

Base address: ADC_B = 0x4017_0000

Offset address: 0x0C4 + 0x10 × n

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	TRGELC5	TRGELC4	TRGELC3	TRGELC2	TRGELC1	TRGELC0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	TRGELC0 to TRGELC5	ELC Trigger m Enable The suffix number of each bit symbol corresponds to the ELC trigger number m. 0: Disable ELC Trigger m 1: Enable ELC Trigger m	R/W
31:6	-	These bits are read as 0. The write value should be 0.	R/W

The ADTRGELCn register enables/disables the ELC Trigger m as the starting conditions for A/D conversion of scan group n.

36.2.2.9 ADTRGGPTn : GPT Trigger Enable Register n (n = 0 to 8)

Base address: ADC_B = 0x4017_0000

Offset address: 0x0C8 + 0x10 × n

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	TRGGPTB9	TRGGPTB8	TRGGPTB7	TRGGPTB6	TRGGPTB5	TRGGPTB4	TRGGPTB3	TRGGPTB2	TRGGPTB1	TRGGPTB0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	TRGGPTA9	TRGGPTA8	TRGGPTA7	TRGGPTA6	TRGGPTA5	TRGGPTA4	TRGGPTA3	TRGGPTA2	TRGGPTA1	TRGGPTA0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	TRGGPTA0 to TRGGPTA9	GPT channel m A/D Conversion Starting Request A Enable The suffix number of each bit symbol corresponds to the GPT channel number m. 0: Disable the A/D conversion stating request A from GPT channel m 1: Enable the A/D conversion stating request A from GPT channel m	R/W
15:10	-	These bits are read as 0. The write value should be 0.	R/W
25:16	TRGGPTB0 to TRGGPTB9	GPT channel m A/D Conversion Starting Request B Enable The suffix number of each bit symbol corresponds to the GPT channel number m. 0: Disable the A/D conversion stating request B from GPT channel m 1: Enable the A/D conversion stating request B from GPT channel m	R/W
31:26	-	These bits are read as 0. The write value should be 0.	R/W

The ADTRGGPTn register enables/disables the A/D conversion starting request A/B from GPT channel m as the starting conditions for A/D conversion of scan group n.

36.2.2.10 ADTRGENR : A/D Conversion Start Trigger Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xC08

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	STTRGEN8	STTRGEN7	STTRGEN6	STTRGEN5	STTRGEN4	STTRGEN3	STTRGEN2	STTRGEN1	STTRGEN0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	STTRGEN0 to STTRGEN8	Scan Group n A/D Conversion Start Trigger Enable The suffix number of each bit symbol corresponds to the scan group number n. 0: Disable the A/D conversion start trigger 1: Enable the A/D conversion start trigger	R/W
31:9	-	These bits are read as 0. The write value should be 0.	R/W

The ADTRGENR register enables/disables the trigger from the peripheral modules for starting the A/D conversion of Scan group n. The triggers for each scan group are selected in the ADTRGEXTn, ADTRGELCn, and ADTRGGPTn registers.

36.2.3.3 ADDOPCRBn : A/D Conversion Data Operation Control B Register n (n = 0 to 36)

Base address: ADC_B = 0x4017_0000

Offset address: 0x608 + 0x10 × n

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	CMPTBLE7	CMPTBLE6	CMPTBLE5	CMPTBLE4	CMPTBLE3	CMPTBLE2	CMPTBLE1	CMPTBLE0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	ADC[3:0]				-	-	-	-	-	-	AVEMD[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

bit	Symbol	Function	R/W
1:0	AVEMD[1:0]	Addition/Averaging Mode Selection 0 0: Not use Addition/Averaging mode 0 1: Addition mode 1 0: Averaging mode 1 1: Setting prohibited	R/W
7:2	-	These bits are read as 0. The write value should be 0.	R/W
11:8	ADC[3:0]	Addition/Averaging Times Selection 0x0: 1-time conversion (no addition, same as normal conversion) 0x1: 2-time conversion (1 addition) 0x3: 4-time conversion (3 additions) 0x4: 8-time conversion (7 additions) 0x5: 16-time conversion (15 additions) 0x6: 32-time conversion (31 additions) 0x7: 64-time conversion (63 additions) 0x8: 128-time conversion (127 additions) 0x9: 256-time conversion (255 additions) 0xA: 512-time conversion (511 additions) 0xB: 1024-time conversion (1023 additions) Others: Setting prohibited	R/W
15:12	-	These bits are read as 0. The write value should be 0.	R/W
23:16	CMPTBLE0 to CMPTBLE7	Compare Match Enable The suffix number of each bit symbol corresponds to the compare match table number m. 0: Disable the compare match with the compare match table m 1: Enable the compare match with the compare match table m	R/W
31:24	-	These bits are read as 0. The write value should be 0.	R/W

The ADDOPCRBn register is one of the registers that selects the data calculation function for the A/D conversion data of virtual channel n.

36.2.7.1 ADLIMINTCR : Limiter Clip Interrupt Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x3A0

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	LIMIE8	LIMIE7	LIMIE6	LIMIE5	LIMIE4	LIMIE3	LIMIE2	LIMIE1	LIMIE0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LIMIE0 to LIMIE8	Limiter Clip Interrupt n Enable bit The suffix number of each bit symbol corresponds to the limiter clip interrupt number n. 0: Disable the limiter clip interrupt n 1: Enable the limiter clip interrupt n	R/W
31:9	-	These bits are read as 0. The write value should be 0.	R/W

The ADLIMINTCR register enables/disables the limiter clip interrupt n.

36.2.7.3 ADLIMGRSR : Limiter Clip Scan Group Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD28

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	LIMGRF8	LIMGRF7	LIMGRF6	LIMGRF5	LIMGRF4	LIMGRF3	LIMGRF2	LIMGRF1	LIMGRF0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LIMGRF0 to LIMGRF8	Scan Group n Limiter Clip Flag The suffix number of each bit symbol corresponds to the scan group number n. 0: Limiter clip for scan group n is not detected 1: Limiter clip for scan group n is detected	R
31:9	-	These bits are read as 0.	R

The ADLIMGRSR register indicates whether the limiter clip occurred in the scanning operation for scan group n. Each flag can be cleared in the ADLIMGRSCR.

36.2.7.4 ADLIMCHSR0 : Limiter Clip Channel Status Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xD2C

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	LIMCHF28	LIMCHF27	LIMCHF26	LIMCHF25	LIMCHF24	LIMCHF23	LIMCHF22	LIMCHF21	LIMCHF20	LIMCHF19	LIMCHF18	LIMCHF17	LIMCHF16
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LIMCHF15	LIMCHF14	LIMCHF13	LIMCHF12	LIMCHF11	LIMCHF10	LIMCHF9	LIMCHF8	LIMCHF7	LIMCHF6	LIMCHF5	LIMCHF4	LIMCHF3	LIMCHF2	LIMCHF1	LIMCHF0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	LIMCHF0 to LIMCHF28	Analog Channel n: Limiter Clip Flag The suffix number of each bit symbol corresponds to the analog channel number n. 0: Limiter clip is not detected 1: Limiter clip is detected	R
31:29	-	These bits are read as 0.	R

The ADLIMCHSR0 register indicates whether the limiter clip occurred when the A/D conversion for the analog channel n is performed. Each flag can be cleared in ADLIMCHSCR0.

36.2.7.6 ADLIMGRSCR : Limiter Clip Scan Group Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD3C

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	LIMGRC8	LIMGRC7	LIMGRC6	LIMGRC5	LIMGRC4	LIMGRC3	LIMGRC2	LIMGRC1	LIMGRC0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LIMGRC0 to LIMGRC8	Scan Group n Limiter Clip Flag Clear The suffix number of each bit symbol corresponds to the scan group number n. 0: No effect 1: ADLIMGRSR.LIMGRFn is cleared	W
31:9	-	The write value should be 0.	W

The ADLIMGRSCR register clears the limiter clip flag for scan group n (ADLIMGRSR.LIMGRFn).

36.2.7.7 ADLIMCHSCR0 : Limiter Clip Channel Status Clear Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xD40

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	LIMCHC28	LIMCHC27	LIMCHC26	LIMCHC25	LIMCHC24	LIMCHC23	LIMCHC22	LIMCHC21	LIMCHC20	LIMCHC19	LIMCHC18	LIMCHC17	LIMCHC16
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LIMCHC15	LIMCHC14	LIMCHC13	LIMCHC12	LIMCHC11	LIMCHC10	LIMCHC9	LIMCHC8	LIMCHC7	LIMCHC6	LIMCHC5	LIMCHC4	LIMCHC3	LIMCHC2	LIMCHC1	LIMCHC0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	LIMCHC0 to LIMCHC28	Analog Channel n Limiter Clip Flag Clear bit The suffix number of each bit symbol corresponds to the analog channel number n. 0: No effect 1: ADLIMCHSR0.LIMCHFn is cleared	W
31:29	-	The write value should be 0.	W

The ADLIMCHSCR0 register clears the limiter clip flag for the analog channel n (ADLIMCHSR0.LIMCHFn).

36.2.8.1 ADCMPENR : Compare Match Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x400

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	CMPEN7	CMPEN6	CMPEN5	CMPEN4	CMPEN3	CMPEN2	CMPEN1	CMPEN0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CMPEN0 to CMPEN7	Compare Match n Enable The suffix number of each bit symbol corresponds to the compare match number n. 0: Disable the compare match n 1: Enable the compare match n	R/W
31:8	-	These bits are read as 0. The write value should be 0.	R/W

The ADCMPENR register enables/disables the compare match n.

36.2.8.2 ADCMPINTCR : Compare Match Interrupt Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x404

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	CMPIE3	CMPIE2	CMPIE1	CMPIE0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CMPIE0 to CMPIE3	Compare Match Interrupt n Enable The suffix number of each bit symbol corresponds to the compare match interrupt number n. 0: Disable the compare match interrupt n 1: Enable the compare match interrupt n	R/W
31:4	-	These bits are read as 0. The write value should be 0.	R/W

The ADCMPINTCR register enables/disables the compare match interrupt n.

36.2.8.3 ADCCMPCRn : Composite Compare Match Configuration Register n (n = 0, 1)

Base address: ADC_B = 0x4017_0000

Offset address: 0x408 + 0x04 × n

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	CCMPTBL7	CCMPTBL6	CCMPTBL5	CCMPTBL4	CCMPTBL3	CCMPTBL2	CCMPTBL1	CCMPTBL0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CCMPCND[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CCMPCND[1:0]	Composite Compare Match Condition Selection 0 0: Logical disjunction (OR) conditions 0 1: Logical conjunction (AND) conditions 1 0: Logical exclusive disjunction (EXOR) conditions 1 1: Setting prohibited	R/W
15:2	-	These bits are read as 0. The write value should be 0.	R/W
23:16	CCMPTBL0 to CCMPTBL7	Composite Compare Match Condition Table Selection 0: Not use the compare match table m 1: Use the compare match table m	R/W
31:24	-	These bits are read as 0. The write value should be 0.	R/W

The ADCCMPCRn register configures the conditions for the composite compare match interrupt n

36.2.8.7 ADCMPTBSR : Compare Match Table Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD00

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	CMPTBF7	CMPTBF6	CMPTBF5	CMPTBF4	CMPTBF3	CMPTBF2	CMPTBF1	CMPTBF0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CMPTBF0 to CMPTBF7	Compare Match Table n Match Flag The suffix number of each bit symbol corresponds to the compare match table number n. 0: Match event with compare match table n is not detected 1: Match event with compare match table n is detected	R
31:8	-	These bits are read as 0.	R

The ADCMPTBSR register indicates whether the match event with the Compare Match Table n occurred during the A/D conversion. Each flag can be cleared in the ADCMPTBSCR.

36.2.8.8 ADCMPTBSCR : Compare Match Table Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD04

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	CMPTBC7	CMPTBC6	CMPTBC5	CMPTBC4	CMPTBC3	CMPTBC2	CMPTBC1	CMPTBC0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CMPTBC0 to CMPTBC7	Compare Match Table n: Match Flag Clear The suffix number of each bit symbol corresponds to the compare match table number n. 0: No effect 1: ADCMPTBSR.CMPTBFn is cleared	W
31:8	-	The write value should be 0.	W

The ADCMPTBSCR register clears the match flag for the compare match n (ADCMPTBSR.CMPTBFn).

36.2.8.9 ADCMPCHSR0 : Compare Match Channel Status Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xD08

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	CMPCHF28	CMPCHF27	CMPCHF26	CMPCHF25	CMPCHF24	CMPCHF23	CMPCHF22	CMPCHF21	CMPCHF20	CMPCHF19	CMPCHF18	CMPCHF17	CMPCHF16
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMPCHF15	CMPCHF14	CMPCHF13	CMPCHF12	CMPCHF11	CMPCHF10	CMPCHF9	CMPCHF8	CMPCHF7	CMPCHF6	CMPCHF5	CMPCHF4	CMPCHF3	CMPCHF2	CMPCHF1	CMPCHF0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	CMPCHF0 to CMPCHF28	Analog Channel n: Compare Match Flag The suffix number of each bit symbol corresponds to the analog channel number n. 0: Compare match is not detected 1: Compare match is detected	R
31:29	-	These bits are read as 0.	R

The ADCMPCHSR0 register indicates whether the compare match event for the Analog Channel n is detected. Each flag can be cleared in ADCMPCHSCR0.

36.2.8.11 ADCMPCHSCR0 : Compare Match Channel Status Clear Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xD18

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	CMPCHC28	CMPCHC27	CMPCHC26	CMPCHC25	CMPCHC24	CMPCHC23	CMPCHC22	CMPCHC21	CMPCHC20	CMPCHC19	CMPCHC18	CMPCHC17	CMPCHC16
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMPCHC15	CMPCHC14	CMPCHC13	CMPCHC12	CMPCHC11	CMPCHC10	CMPCHC9	CMPCHC8	CMPCHC7	CMPCHC6	CMPCHC5	CMPCHC4	CMPCHC3	CMPCHC2	CMPCHC1	CMPCHC0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	CMPCHC0 to CMPCHC28	Analog Channel n: Compare Match Flag Clear bit The suffix number of each bit symbol corresponds to the analog channel number n. 0: No effect 1: ADCMPCHSR0.CMPCHFn is cleared	W
31:29	-	The write value should be 0.	W

The ADCMPCHSCR0 register clears the compare match flag for the Analog Channel n (ADCMPCHSR0.CMPCHFn).

36.2.9.2 ADSYSTR : A/D Conversion Synchronous Software Start Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xC10

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	ADSYST8	ADSYST7	ADSYST6	ADSYST5	ADSYST4	ADSYST3	ADSYST2	ADSYST1	ADSYST0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	ADSYST0 to ADSYST8	Scan Group n: A/D Conversion start The suffix number of each bit symbol corresponds to the scan group number n. 0: No effect 1: Start the A/D conversion of scan group n	W
31:9	-	The write value should be 0.	W

The ADSYSTR register controls the start of the A/D conversion of scan group n. This register is used to start the A/D conversions of several scan groups simultaneously by software..

36.2.10.2 ADGRSR : Scan Group Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xC84

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	ACTGR8	ACTGR7	ACTGR6	ACTGR5	ACTGR4	ACTGR3	ACTGR2	ACTGR1	ACTGR0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	ACTGR0 to ACTGR8*1	Scan Group n Status The suffix number of each bit symbol corresponds to the scan group number n. 0: Scan group n is idle 1: Scan group n is in the scanning operation	R
31:9	-	These bits are read as 0.	R

Note 1. In the group priority operation, if the scanning operation of a low priority group is interrupted, the ACTGRn bit of the corresponding scan group is set to 1.

The ADGRSR register indicates the operating status for each scan group

36.2.10.3 ADSCANENDSR : Scan End Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD50

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	SCENDF8	SCENDF7	SCENDF6	SCENDF5	SCENDF4	SCENDF3	SCENDF2	SCENDF1	SCENDF0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SCENDF0 to SCENDF8[*1]	Scan Group n Scan End Flag The suffix number of each bit symbol corresponds to the scan group number n. 0: Scan group n has not been scanned 1: End of scan for scan group n is detected	R
31:9	-	These bits are read as 0.	R

Note 1. If the A/D conversion operation is stopped with the ADSTOPR register, the SCENDFn bit of the scan group in which the scan operation was stopped is not changed. (It is not set to 1)

The ADSCANENDSR register indicates whether the scanning operation for each scan group has been done. Each flag can be cleared in ADSCANENDSCR register.

36.2.10.4 ADSCANENDSCR : Scan End Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD54

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	SCENDC8	SCENDC7	SCENDC6	SCENDC5	SCENDC4	SCENDC3	SCENDC2	SCENDC1	SCENDC0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SCENDC0 to SCENDC8	Scan Group n Scan End Flag Clear The suffix number of each bit symbol corresponds to the scan group number n. 0: No effect 1: ADSCANENDSR.SCENDFn is cleared	W
31:9	-	The write value should be 0.	W

The ADSCANENDSCR register clears the scan end flag for the scan group n.

36.2.10.10 ADOVFCHSR0 : A/D Conversion Overflow Channel Status Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xCA4

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	OVFCHF28	OVFCHF27	OVFCHF26	OVFCHF25	OVFCHF24	OVFCHF23	OVFCHF22	OVFCHF21	OVFCHF20	OVFCHF19	OVFCHF18	OVFCHF17	OVFCHF16
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OVFCHF15	OVFCHF14	OVFCHF13	OVFCHF12	OVFCHF11	OVFCHF10	OVFCHF9	OVFCHF8	OVFCHF7	OVFCHF6	OVFCHF5	OVFCHF4	OVFCHF3	OVFCHF2	OVFCHF1	OVFCHF0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	OVFCHF0 to OVFCHF28	Analog Channel n: Overflow Flag The suffix number of each bit symbol corresponds to the analog channel number n. 0: Overflow is not detected 1: Overflow is detected	R
31:29	-	These bits are read as 0.	R

The ADOVFCHSR0 register indicates whether the overflow has occurred in the A/D conversion of the analog channel n.
Each flag can be cleared in ADOVFCHSCR0 register.

36.2.10.13 ADOVFCHSCR0 : A/D Conversion Overflow Channel Status Clear Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xCB8

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	OVFCHC28	OVFCHC27	OVFCHC26	OVFCHC25	OVFCHC24	OVFCHC23	OVFCHC22	OVFCHC21	OVFCHC20	OVFCHC19	OVFCHC18	OVFCHC17	OVFCHC16
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OVFCHC15	OVFCHC14	OVFCHC13	OVFCHC12	OVFCHC11	OVFCHC10	OVFCHC9	OVFCHC8	OVFCHC7	OVFCHC6	OVFCHC5	OVFCHC4	OVFCHC3	OVFCHC2	OVFCHC1	OVFCHC0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	OVFCHC0 to OVFCHC28	Analog Channel n: Overflow Flag Clear The suffix number of each bit symbol corresponds to the analog channel number n. 0: No effect 1: ADOVFCHSR0.OVFCHFn is cleared	W
31:29	-	The write value should be 0.	W

The ADOVFCHSCR0 register clears the Overflow flag for the analog channel n.

36.2.11.1 ADFIFOCR : FIFO Control Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x4C0

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	FIFOEN8	FIFOEN7	FIFOEN6	FIFOEN5	FIFOEN4	FIFOEN3	FIFOEN2	FIFOEN1	FIFOEN0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFOEN0 to FIFOEN8	Scan Group n FIFO Enable The suffix number of each bit symbol corresponds to the scan group number n. 0: Disable scan group n FIFO function 1: Enable scan group n FIFO function	R/W
31:9	-	These bits are read as 0. The write value should be 0.	R/W

The ADFIFOCR register enables/disables the FIFO function of scan group n.

36.2.11.2 ADFIFOINTCR : FIFO Interrupt Control Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x4C4

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	FIFOIE8	FIFOIE7	FIFOIE6	FIFOIE5	FIFOIE4	FIFOIE3	FIFOIE2	FIFOIE1	FIFOIE0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFOIE0 to FIFOIE8	Scan Group n FIFO Interrupt Enable The suffix number of each bit symbol corresponds to the scan group number n. 0: Disable scan group n FIFO interrupt 1: Enable scan group n FIFO interrupt	R/W
31:9	-	These bits are read as 0. The write value should be 0.	R/W

The ADFIFOINTCR register enables/disables the FIFO data read request interrupt and FIFO overflow interrupt for scan group n.

36.2.11.13 ADFIFODCR : FIFO Data Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xCF0

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	FIFODC8	FIFODC7	FIFODC6	FIFODC5	FIFODC4	FIFODC3	FIFODC2	FIFODC1	FIFODC0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFODC0 to FIFODC8	Scan Group n FIFO Data Clear The suffix number of each bit symbol corresponds to the scan group number n. 0: No effect 1: Clear the data of scan group n FIFO	W
31:9	-	The write value should be 0.	W

The ADFIFODCR register clears the data in FIFO for each scan group.

36.2.11.14 ADFIFOERSR : FIFO Error Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xCF4

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	FIFOFLF8	FIFOFLF7	FIFOFLF6	FIFOFLF5	FIFOFLF4	FIFOFLF3	FIFOFLF2	FIFOFLF1	FIFOFLF0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	FIFOOVF8	FIFOOVF7	FIFOOVF6	FIFOOVF5	FIFOOVF4	FIFOOVF3	FIFOOVF2	FIFOOVF1	FIFOOVF0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFOOVF0 to FIFOOVF8	Scan Group n FIFO Overflow Flag The suffix number of each bit symbol corresponds to the scan group number n. 0: No overflow 1: FIFO overflow is detected	R
15:9	-	These bits are read as 0.	R
24:16	FIFOFLF0 to FIFOFLF8	Scan Group n FIFO Data Read Request Flag The suffix number of each bit symbol corresponds to the scan group number n. 0: FIFO Data Read Request is not detected. 1: FIFO Data Read Request is detected.	R
31:25	-	These bits are read as 0.	R

The ADFIFOERSR register indicates the status of the FIFO. Each flag can be cleared in ADFIFOERSCR.

36.2.11.15 ADFIFOERSCR : FIFO Error Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xCF8

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	FIFOFLC8	FIFOFLC7	FIFOFLC6	FIFOFLC5	FIFOFLC4	FIFOFLC3	FIFOFLC2	FIFOFLC1	FIFOFLC0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	FIFOOVFC8	FIFOOVFC7	FIFOOVFC6	FIFOOVFC5	FIFOOVFC4	FIFOOVFC3	FIFOOVFC2	FIFOOVFC1	FIFOOVFC0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFOOVFC0 to FIFOOVFC8	Scan Group n FIFO Overflow Flag Clear The suffix number of each bit symbol corresponds to the scan group number n. 0: No effect 1: ADFIFOERSR.FIFOOVFn is cleared	W
15:9	-	The write value should be 0.	W
24:16	FIFOFLC0 to FIFOFLC8	Scan Group n FIFO Data Read Request Flag Clear The suffix number of each bit symbol corresponds to the scan group number n. 0: No effect 1: ADFIFOERSR.FIFOFLFn is cleared	W
31:25	-	The write value should be 0.	W

ADFIFOERSCR clears the FIFO overflow flags and the FIFO data read request flags for scan group n.

28.2.14 CFDGSTS : Global Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x001C

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	GRAMINIT	GSLPSTS	GHLTSTS	GRSTSTS
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	GRSTSTS	Global Reset Status 0: Not in Reset mode 1: In Reset mode	R
1	GHLTSTS	Global Halt Status 0: Not in Halt mode 1: In Halt mode	R
2	GSLPSTS	Global Sleep Status 0: Not in Sleep mode 1: In Sleep mode	R
3	GRAMINIT	Global RAM Initialization 0: RAM initialization is complete 1: RAM initialization is ongoing	R
31:4	-	These bits are read as 0.	R

The Global Status Register indicates the global status of the CANFD module.

28.2.16 CFDGTINTSTS : Global TX Interrupt Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00A4

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	THIF0	CFTIF0	TQIF0	TAI0	TSIF0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

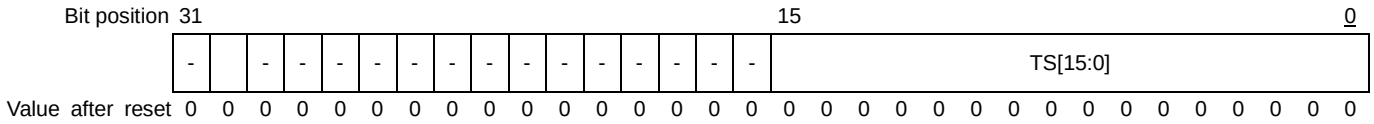
Bit	Symbol	Function	R/W
0	TSIF0	TX Successful Interrupt Flag 0: Channel n TX Successful Interrupt flag not set 1: Channel n TX Successful Interrupt flag set	R
1	TAI0	TX Abort Interrupt Flag 0: Channel n TX Abort Interrupt flag not set 1: Channel n TX Abort Interrupt flag set	R
2	TQIF0	TX Queue Interrupt Flag 0: Channel n TX Queue Interrupt flag not set 1: Channel n TX Queue Interrupt flag set	R
3	CFTIF0	COM FIFO TX Mode Interrupt Flag 0: Channel n COM FIFO TX Mode Interrupt flag not set 1: Channel n COM FIFO TX Mode Interrupt flag set	R
4	THIF0	TX History List Interrupt 0: Channel n TX History List Interrupt flag not set 1: Channel n TX History List Interrupt flag set	R
31:5	-	These bits are read as 0.	R

The Global TX Interrupt Status register indicates the detection of transmit specific interrupts.

28.2.17 CFDGTSC : Global Timestamp Counter Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0024



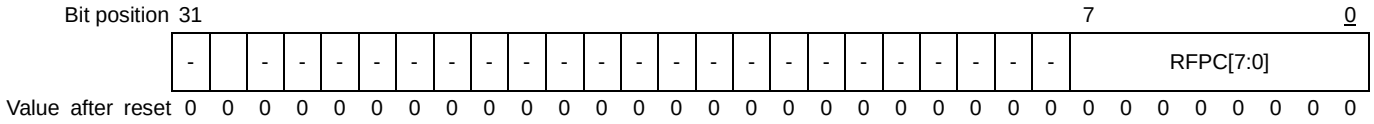
Bit	Symbol	Function	R/W
15:0	TS[15:0]	Timestamp value	R
31:16	-	These bits are read as 0.	R

The Global Timestamp Counter register stores the timestamp based on the selected configuration

28.2.28 CFDRFPCTRa : RX FIFO Pointer Control Registers a (a = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x004C + 0x04 × a



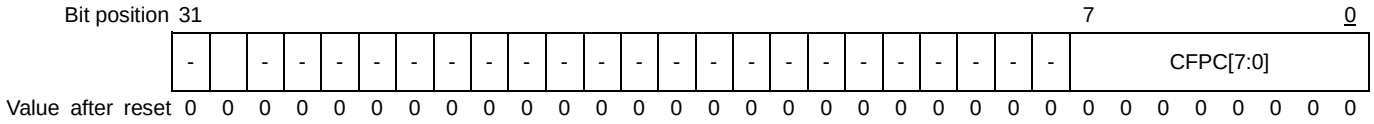
Bit	Symbol	Function	R/W
7:0	RFPC[7:0]	RX FIFO Pointer Control Increments read pointer of the corresponding RX FIFO buffers	W
31:8	-	The write value should be 0.	W

The RX FIFO Pointer Control Registers can be used to increment the read pointer of the corresponding RX FIFO buffers.

28.2.31 CFDCFPCTR : Common FIFO Pointer Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x005C



Bit	Symbol	Function	R/W
7:0	CFPC[7:0]	Common FIFO Pointer Control Increments read or write pointer of the corresponding Common FIFO buffers depending on the mode configuration.	W
31:8	-	The write value should be 0.	W

The Common FIFO Pointer Control Registers can be used to increment the read or write pointer of the corresponding Common FIFO buffer.

28.2.33 CFDFFSTS : FIFO Full Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0064

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	CFFLL	-	-	-	-	-	-	RFXFLL[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	RFXFLL[1:0]	RX FIF0 Full Status 0: Corresponding FIFO not full 1: Corresponding FIFO full	R
7:2	-	These bits are read as 0.	R
8	CFFLL	Common FIF0 Full Status 0: Corresponding FIFO not full 1: Corresponding FIFO full	R
31:9	-	These bits are read as 0.	R

The FIFO Full Status Register shows status of the full bits of the FIFO buffers.

28.2.34 CFDFMSTS : FIFO Message Lost Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0068

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	CFMLT	-	-	-	-	-	-	RFXMLT[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	RFXMLT[1:0]	RX FIFO Message Lost Status 0: Corresponding FIFO Message Lost flag not set 1: Corresponding FIFO Message Lost flag set	R
7:2	-	These bits are read as 0.	R
8	CFMLT	Common FIFO Message Lost Status 0: Corresponding FIFO Message Lost flag not set 1: Corresponding FIFO Message Lost flag set	R
31:9	-	These bits are read as 0.	R

The FIFO Message Lost Status Register shows status of the Msg Lost bits of the FIFO buffers.

28.2.35 CFDRFISTS : RX FIFO Interrupt Flag Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x006C

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RFXIF[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	RFXIF[1:0]	RX FIFO[x] Interrupt Flag Status 0: Corresponding RX FIFO Interrupt flag not set 1: Corresponding RX FIFO Interrupt flag set	R
31:2	-	These bits are read as 0.	R

The FIFO Interrupt Flag Status Register shows status of the interrupt flag bits of the RX FIFO buffers.

28.2.37 CFDCDTSTS : DMA Transfer Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00CC

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	CFDMASTS	-	-	-	-	-	-	RFDMASTS1	RFDMASTS0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFDMASTS0	DMA Transfer Status for RX FIFO 0 0: DMA transfer stopped 1: DMA transfer on going	R
1	RFDMASTS1	DMA Transfer Status for RX FIFO 1 0: DMA transfer stopped 1: DMA transfer on going	R
7:2	-	These bits are read as 0.	R
8	CFDMASTS	DMA Transfer Status only for Common FIFO 0: DMA transfer stopped 1: DMA transfer on going	R
31:9	-	These bits are read as 0.	R

The DMA Transfer Status Register shows the status of the DMA transfer.

28.2.47 CFDTXQPCTR : TX Queue Pointer Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0094

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TXQPC[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TXQPC[7:0]	TX Queue Pointer Control Increments the write pointer to the TX Queue buffer in the corresponding channel	W
31:8	-	The write value should be 0.	W

The TX Queue Pointer Control Registers are used to confirm storage of a full message in the corresponding TX Queue buffers.

28.2.51 CFDTHLACC1 : TX History List Access Register 1

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0744

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TIFL[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TID[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TID[15:0]	Transmit ID These bits indicate that message buffer reference ID, TX FIFO reference ID, or AFL pointer field is stored for software drivers.	R
17:16	TIFL[1:0]	Transmit Information Label These bits indicate that message buffer information label, TX FIFO information label, or AFL information label is stored for software drivers.	R
31:18	-	These bits are read as 0.	R

The TX History List Access Registers 1 provide access to entry in the TX History List based on the read pointer value.

28.2.52 CFDTHLPCTR : TX History List Pointer Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00A0

Bit position	31																						7							0
	-		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	THLPC[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	THLPC[7:0]	TX History List Pointer Control Increments the write pointer to the TX History List in the corresponding channel	W
31:8	-	The write value should be 0.	W

The TX History List Pointer Control Registers are used to increment the read pointer of the TX History List.

28.2.57 CFDGLOCKK : Global Lock Key Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00B8

Bit position	31																15													0
	-		-	-	-	-	-	-	-	-	-	-	-	-	-	-	LOCK[15:0]													
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	LOCK[15:0]	Lock Key Key bits for unlocking the protection of test modes	W
31:16	-	The write value should be 0.	W

The Global Lock Key register is a write-only register that is used to unlock the protection for special test bits.
See section 28.9.2. Global Test Modes for Lock key specification.

40.2.2 DOSR : DOC Flag Status Register

Base address: DOC_B = 0x4010_9000

Offset address: 0x04

Bit position	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	DOPCF
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DOPCF	Data Operation Circuit Flag Indicates the result of an operation.	R
7:1	-	These bits are read as 0.	R

The DOSR register indicates the status of the data operation.

40.2.3 DOSCR : DOC Flag Status Clear Register

Base address: DOC_B = 0x4010_9000

Offset address: 0x08

Bit position	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	DOPCFCL
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DOPCFCL	DOPCF Clear W 0: Maintains the DOPCF flag state. 1: Clears the DOPCF flag.	W
7:1	-	The write value should be 0.	W

The DOSCR is a register which can clear the status of data operation. This register is read as 0x00.

[Original]

36.2.2.2 ADSGER : Scan Group Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x048

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	SGREn								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SGREn	Scan Group n Enable 0: Disable the scan group n 1: Enable the scan group n	R/W
31:9	-	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 8

The ADSGER register selects the enable/disable to each scan group..

36.2.2.6 ADINTCR : Scan End Interrupt Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x05C

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	ADIEn									
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	ADIEn	Scan Group n Scan End Interrupt Enable 0: Disable scan end interrupt 1: Enable scan end interrupt	R/W
31:10	-	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 8

The ADINTCR register enables/disables the scan end interrupt.

36.2.2.8 ADTRGELCn : ELC Trigger Enable Register n (n = 0 to 8)

Base address: ADC_B = 0x4017_0000

Offset address: 0x0C4 + 0x10 × n

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	TRGELCm					
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	TRGELCm	ELC Trigger m Enable 0: Disable ELC Trigger m 1: Enable ELC Trigger m	R/W
31:6	-	These bits are read as 0. The write value should be 0.	R/W

Note: m = 0 to 5

The ADTRGELCn register enables/disables the ELC Trigger m as the starting conditions for A/D conversion of scan group n.

36.2.2.9 ADTRGGPTn : GPT Trigger Enable Register n (n = 0 to 8)

Base address: ADC_B = 0x4017_0000

Offset address: 0x0C8 + 0x10 × n

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	TRGGPTBm									
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	TRGGPTAm									
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	TRGGPTA0 to TRGGPTA9	GPT channel m A/D Conversion Starting Request A Enable 0: Disable the A/D conversion stating request A from GPT channel m 1: Enable the A/D conversion stating request A from GPT channel m	R/W
15:10	-	These bits are read as 0. The write value should be 0.	R/W
25:16	TRGGPTB0 to TRGGPTB9	GPT channel m A/D Conversion Starting Request B Enable 0: Disable the A/D conversion stating request B from GPT channel m 1: Enable the A/D conversion stating request B from GPT channel m	R/W
31:26	-	These bits are read as 0. The write value should be 0.	R/W

Note: m = 0 to 9

The ADTRGGPTn register enables/disables the A/D conversion starting request A/B from GPT channel m as the starting conditions for A/D conversion of scan group n.

36.2.2.10 ADTRGENR : A/D Conversion Start Trigger Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xC08

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	STTRGENn								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	STTRGENn	Scan Group n A/D Conversion Start Trigger Enable 0: Disable the A/D conversion start trigger 1: Enable the A/D conversion start trigger	R/W
31:9	-	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 8

The ADTRGENR register enables/disables the trigger from the peripheral modules for starting the A/D conversion of Scan group n. The triggers for each scan group are selected in the ADTRGEXTn, ADTRGELCn, and ADTRGGPTn registers.

36.2.3.3 ADDOPCRBn : A/D Conversion Data Operation Control B Register n (n = 0 to 36)

Base address: ADC_B = 0x4017_0000

Offset address: 0x608 + 0x10 × n

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	CMPTBLEm							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	ADC[3:0]				-	-	-	-	-	-	AVEMD[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

bit	Symbol	Function	R/W
1:0	AVEMD[1:0]	Addition/Averaging Mode Selection 0 0: Not use Addition/Averaging mode 0 1: Addition mode 1 0: Averaging mode 1 1: Setting prohibited	R/W
7:2	-	These bits are read as 0. The write value should be 0.	R/W
11:8	ADC[3:0]	Addition/Averaging Times Selection 0x0: 1-time conversion (no addition, same as normal conversion) 0x1: 2-time conversion (1 addition) 0x3: 4-time conversion (3 additions) 0x4: 8-time conversion (7 additions) 0x5: 16-time conversion (15 additions) 0x6: 32-time conversion (31 additions) 0x7: 64-time conversion (63 additions) 0x8: 128-time conversion (127 additions) 0x9: 256-time conversion (255 additions) 0xA: 512-time conversion (511 additions) 0xB: 1024-time conversion (1023 additions) Others: Setting prohibited	R/W
15:12	-	These bits are read as 0. The write value should be 0.	R/W
23:16	CMPTBLEm	Compare Match Enable 0: Disable the compare match with the compare match table m 1: Enable the compare match with the compare match table m	R/W
31:24	-	These bits are read as 0. The write value should be 0.	R/W

Note: m = 0 to 7

The ADDOPCRBn register is one of the registers that selects the data calculation function for the A/D conversion data of virtual channel n.

36.2.7.1 ADLIMINTCR : Limiter Clip Interrupt Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x3A0

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	LIMIEn								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LIMIEn	Limiter Clip Interrupt n Enable bit 0: Disable the limiter clip interrupt n 1: Enable the limiter clip interrupt n	R/W
31:9	-	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 8

The ADLIMINTCR register enables/disables the limiter clip interrupt n.

36.2.7.3 ADLIMGRSR : Limiter Clip Scan Group Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD28

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	LIMGRFn								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LIMGRFn	Scan Group n Limiter Clip Flag 0: Limiter clip for scan group n is not detected 1: Limiter clip for scan group n is detected	R
31:9	-	These bits are read as 0.	R

Note: n = 0 to 8

The ADLIMGRSR register indicates whether the limiter clip occurred in the scanning operation for scan group n. Each flag can be cleared in the ADLIMGRSCR.

36.2.7.4 ADLIMCHSR0 : Limiter Clip Channel Status Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xD2C

Bit position	31		28																										0
	-		-	LIMCHFn																									
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	LIMCHFn	Analog Channel n: Limiter Clip Flag 0: Limiter clip is not detected 1: Limiter clip is detected	R
31:29	-	These bits are read as 0.	R

Note: n = 0 to 28

The ADLIMCHSR0 register indicates whether the limiter clip occurred when the A/D conversion for the analog channel n is performed. Each flag can be cleared in ADLIMCHSCR0.

36.2.7.6 ADLIMGRSCR : Limiter Clip Scan Group Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD3C

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	LIMGRCn								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LIMGRCn	Scan Group n Limiter Clip Flag Clear 0: No effect 1: ADLIMGRSR.LIMGRFn is cleared	W
31:9	-	The write value should be 0.	W

Note: n = 0 to 8

The ADLIMGRSCR register clears the limiter clip flag for scan group n (ADLIMGRSR.LIMGRFn).

36.2.7.7 ADLIMCHSCR0 : Limiter Clip Channel Status Clear Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xD40

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-		-	LIMCHCn																												
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	LIMCHCn	Analog Channel n Limiter Clip Flag Clear bit 0: No effect 1: ADLIMCHSR0.LIMCHFn is cleared	W
31:29	-	The write value should be 0.	W

Note: n = 0 to 28

The ADLIMCHSCR0 register clears the limiter clip flag for the analog channel n (ADLIMCHSR0.LIMCHFn).

36.2.8.1 ADCMPENR : Compare Match Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x400

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	CMPENn							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CMPENn	Compare Match n Enable 0: Disable the compare match n 1: Enable the compare match n	R/W
31:8	-	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 7

The ADCMPENR register enables/disables the compare match n.

36.2.8.2 ADCMPINTCR : Compare Match Interrupt Enable Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x404

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	CMPIEn			
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CMPIEn	Compare Match Interrupt n Enable 0: Disable the compare match interrupt n 1: Enable the compare match interrupt n	R/W
31:4	-	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 3

The ADCMPINTCR register enables/disables the compare match interrupt n.

36.2.8.3 ADCCMPCRn : Composite Compare Match Configuration Register n (n = 0, 1)

Base address: ADC_B = 0x4017_0000

Offset address: 0x408 + 0x04 × n

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	CCMPTBLm							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CCMPCND [1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CCMPCND[1:0]	Composite Compare Match Condition Selection 0 0: Logical disjunction (OR) conditions 0 1: Logical conjunction (AND) conditions 1 0: Logical exclusive disjunction (EXOR) conditions 1 1: Setting prohibited	R/W
15:2	-	These bits are read as 0. The write value should be 0.	R/W
23:16	CCMPTBLm	Composite Compare Match Condition Table Selection 0: Not use the compare match table m 1: Use the compare match table m	R/W
31:24	-	These bits are read as 0. The write value should be 0.	R/W

Note: m = 0 to 7

The ADCCMPCRn register configures the conditions for the composite compare match interrupt n

36.2.8.7 ADCMPTBSR : Compare Match Table Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD00

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	CMPTBFn							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CMPTBFn	Compare Match Table n Match Flag 0: Match event with compare match table n is not detected 1: Match event with compare match table n is detected	R
31:8	-	These bits are read as 0.	R

Note: n = 0 to 7

The ADCMPTBSR register indicates whether the match event with the Compare Match Table n occurred during the A/D conversion. Each flag can be cleared in the ADCMPTBSCR.

36.2.8.8 ADCMPTBSCR : Compare Match Table Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD04

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	CMPTBCn							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CMPTBCn	Compare Match Table n: Match Flag Clear 0: No effect 1: ADCMPTBSR.CMPTBFn is cleared	W
31:8	-	The write value should be 0.	W

Note: n = 0 to 7

The ADCMPTBSCR register clears the match flag for the compare match n (ADCMPTBSR.CMPTBFn).

36.2.8.9 ADCMPCHSR0 : Compare Match Channel Status Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xD08

Bit position	31			28																										0
	-		-	CMPCHFn																										
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	CMPCHFn	Analog Channel n: Compare Match Flag 0: Compare match is not detected 1: Compare match is detected	R
31:29	-	These bits are read as 0.	R

Note: n = 0 to 28

The ADCMPCHSR0 register indicates whether the compare match event for the Analog Channel n is detected. Each flag can be cleared in ADCMPCHSCR0.

36.2.8.11 ADCMPCHSCR0 : Compare Match Channel Status Clear Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xD18

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	CMPCHCn												
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMPCHCn															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	CMPCHCn	Analog Channel n: Compare Match Flag Clear bit 0: No effect 1: ADCMPCHSR0.CMPCHFn is cleared	W
31:29	-	The write value should be 0.	W

Note: n = 0 to 28

The ADCMPCHSCR0 register clears the compare match flag for the Analog Channel n (ADCMPCHSR0.CMPCHFn).

36.2.9.2 ADSYSTR : A/D Conversion Synchronous Software Start Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xC10

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	ADSYSTn								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	ADSYSTn	Scan Group n: A/D Conversion start 0: No effect 1: Start the A/D conversion of scan group n	W
31:9	-	The write value should be 0.	W

Note: n = 0 to 8

The ADSYSTR register controls the start of the A/D conversion of scan group n. This register is used to start the A/D conversions of several scan groups simultaneously by software..

36.2.10.2 ADGRSR : Scan Group Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xC84

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	ACTGRn								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	ACTGRn*1	Scan Group n Status 0: Scan group n is idle 1: Scan group n is in the scanning operation	R
31:9	-	These bits are read as 0.	R

Note: n = 0 to 8

Note 1. In the group priority operation, if the scanning operation of a low priority group is interrupted, the ACTGRn bit of the corresponding scan group is set to 1.

The ADGRSR register indicates the operating status for each scan group

36.2.10.3 ADSCANENDSR : Scan End Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD50

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	SCENDFn								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SCENDFn*1	Scan Group n Scan End Flag 0: Scan group n has not been scanned 1: End of scan for scan group n is detected	R
31:9	-	These bits are read as 0.	R

Note: n = 0 to 8

Note 1. If the A/D conversion operation is stopped with the ADSTOPR register, the SCENDFn bit of the scan group in which the scan operation was stopped is not changed. (It is not set to 1)

The ADSCANENDSR register indicates whether the scanning operation for each scan group has been done. Each flag can be cleared in ADSCANENDSCR register.

36.2.10.4 ADSCANENDSCR : Scan End Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xD54

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	SCENDCn								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SCENDCn	Scan Group n Scan End Flag Clear 0: No effect 1: ADSCANENDSR.SCENDFn is cleared	W
31:9	-	The write value should be 0.	W

Note: n = 0 to 8

The ADSCANENDSCR register clears the scan end flag for the scan group n.

36.2.10.10 ADOVFCHSR0 : A/D Conversion Overflow Channel Status Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xCA4

Bit position	31			28																										0
	-		-	OFVCHFn																										
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	OFVCHFn	Analog Channel n: Overflow Flag 0: Overflow is not detected 1: Overflow is detected	R
31:29	-	These bits are read as 0.	R

Note: n = 0 to 28

The ADOVFCHSR0 register indicates whether the overflow has occurred in the A/D conversion of the analog channel n. Each flag can be cleared in ADOVFCHSCR0 register.

36.2.10.13 ADOVFCHSCR0 : A/D Conversion Overflow Channel Status Clear Register 0

Base address: ADC_B = 0x4017_0000

Offset address: 0xCB8

Bit position	31			28																										0
	-		-	OVFCHCn																										
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	OVFCHCn	Analog Channel n: Overflow Flag Clear 0: No effect 1: ADOVFCHSR0.OVFCHFn is cleared	W
31:29	-	The write value should be 0.	W

Note: n = 0 to 28

The ADOVFCHSCR0 register clears the Overflow flag for the analog channel n.

36.2.11.1 ADFIFOCR : FIFO Control Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x4C0

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	FIFOENn								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFOENn	Scan Group n FIFO Enable 0: Disable scan group n FIFO function 1: Enable scan group n FIFO function	R/W
31:9	-	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 8

The ADFIFOCR register enables/disables the FIFO function of scan group n.

36.2.11.2 ADFIFOINTCR : FIFO Interrupt Control Register

Base address: ADC_B = 0x4017_0000

Offset address: 0x4C4

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	FIFOIEn								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFOIEn	Scan Group n FIFO Interrupt Enable 0: Disable scan group n FIFO interrupt 1: Enable scan group n FIFO interrupt	R/W
31:9	-	These bits are read as 0. The write value should be 0.	R/W

Note: n = 0 to 8

The ADFIFOINTCR register enables/disables the FIFO data read request interrupt and FIFO overflow interrupt for scan group n.

36.2.11.13 ADFIFODCR : FIFO Data Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xCF0

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	FIFODCn								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFODCn	Scan Group n FIFO Data Clear 0: No effect 1: Clear the data of scan group n FIFO	W
31:9	-	The write value should be 0.	W

Note: n = 0 to 8

The ADFIFODCR register clears the data in FIFO for each scan group.

36.2.11.14 ADFIFOERSR : FIFO Error Status Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xCF4

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	FIFOFLFn								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	FIFOOVFn								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFOOVFn	Scan Group n FIFO Overflow Flag 0: No overflow 1: FIFO overflow is detected	R
15:9	-	These bits are read as 0.	R
24:16	FIFOFLFn	Scan Group n FIFO Data Read Request Flag 0: FIFO Data Read Request is not detected. 1: FIFO Data Read Request is detected.	R
31:25	-	These bits are read as 0.	R

Note: n = 0 to 8

The ADFIFOERSR register indicates the status of the FIFO. Each flag can be cleared in ADFIFOERSCR.

36.2.11.15 ADFIFOERSCR : FIFO Error Status Clear Register

Base address: ADC_B = 0x4017_0000

Offset address: 0xCF8

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	FIFOFLCn								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	FIFOOVFCn								
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	FIFOOVFCn	Scan Group n FIFO Overflow Flag Clear 0: No effect 1: ADFIFOERSR.FIFOOVFn is cleared	W
15:9	-	The write value should be 0.	W
24:16	FIFOFLCn	Scan Group n FIFO Data Read Request Flag Clear 0: No effect 1: ADFIFOERSR.FIFOFLFn is cleared	W
31:25	-	The write value should be 0.	W

Note: n = 0 to 8

ADFIFOERSCR clears the FIFO overflow flags and the FIFO data read request flags for scan group n.

28.2.14 CFDGSTS : Global Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x001C

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	GRAMINIT	GSLPSTS	GHLTSTS	GRSTSTS
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	GRSTSTS	Global Reset Status 0: Not in Reset mode 1: In Reset mode	R
1	GHLTSTS	Global Halt Status 0: Not in Halt mode 1: In Halt mode	R
2	GSLPSTS	Global Sleep Status 0: Not in Sleep mode 1: In Sleep mode	R
3	GRAMINIT	Global RAM Initialization 0: RAM initialization is complete 1: RAM initialization is ongoing	R
31:4	-	These bits are read as 0. The write value should be 0.	R/W

The Global Status Register indicates the global status of the CANFD module.

28.2.16 CFDGTINTSTS : Global TX Interrupt Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00A4

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	THIF0	CFTIF0	TQIF0	TAI0	TSIF0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

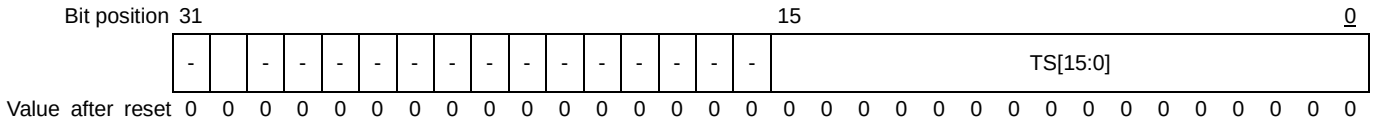
Bit	Symbol	Function	R/W
0	TSIF0	TX Successful Interrupt Flag 0: Channel n TX Successful Interrupt flag not set 1: Channel n TX Successful Interrupt flag set	R
1	TAI0	TX Abort Interrupt Flag 0: Channel n TX Abort Interrupt flag not set 1: Channel n TX Abort Interrupt flag set	R
2	TQIF0	TX Queue Interrupt Flag 0: Channel n TX Queue Interrupt flag not set 1: Channel n TX Queue Interrupt flag set	R
3	CFTIF0	COM FIFO TX Mode Interrupt Flag 0: Channel n COM FIFO TX Mode Interrupt flag not set 1: Channel n COM FIFO TX Mode Interrupt flag set	R
4	THIF0	TX History List Interrupt 0: Channel n TX History List Interrupt flag not set 1: Channel n TX History List Interrupt flag set	R
31:5	-	These bits are read as 0. The write value should be 0.	R/W

The Global TX Interrupt Status register indicates the detection of transmit specific interrupts.

28.2.17 CFDGTSC : Global Timestamp Counter Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0024



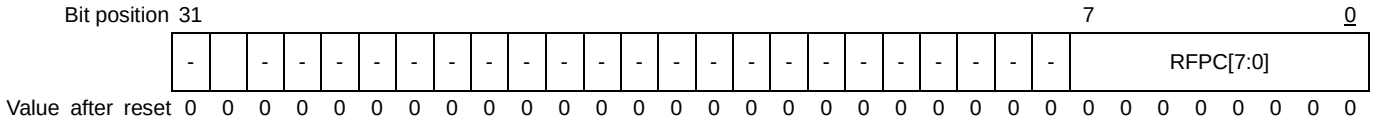
Bit	Symbol	Function	R/W
15:0	TS[15:0]	Timestamp value	R
31:16	-	These bits are read as 0. The write value should be 0..	R/W

The Global Timestamp Counter register stores the timestamp based on the selected configuration

28.2.28 CFDRFPCTRa : RX FIFO Pointer Control Registers a (a = 0 to 1)

Base address: CANFD_B = 0x400B_0000

Offset address: 0x004C + 0x04 × a



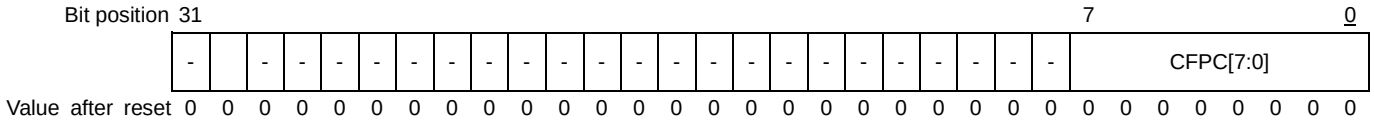
Bit	Symbol	Function	R/W
7:0	RFPC[7:0]	RX FIFO Pointer Control Increments read pointer of the corresponding RX FIFO buffers	W
31:8	-	These bits are read as 0. The write value should be 0.	R/W

The RX FIFO Pointer Control Registers can be used to increment the read pointer of the corresponding RX FIFO buffers.

28.2.31 CFDCFPCTR : Common FIFO Pointer Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x005C



Bit	Symbol	Function	R/W
7:0	CFPC[7:0]	Common FIFO Pointer Control Increments read or write pointer of the corresponding Common FIFO buffers depending on the mode configuration.	W
31:8	-	These bits are read as 0. The write value should be 0.	R/W

The Common FIFO Pointer Control Registers can be used to increment the read or write pointer of the corresponding Common FIFO buffer.

28.2.33 CFDFFSTS : FIFO Full Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0064

Bit position	31																							8							1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CFFLL	-	-	-	-	-	-	RFXFLL[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	RFXFLL[1:0]	RX FIF0 Full Status 0: Corresponding FIFO not full 1: Corresponding FIFO full	R
7:2	-	These bits are read as 0. The write value should be 0.	R/W
8	CFFLL	Common FIF0 Full Status 0: Corresponding FIFO not full 1: Corresponding FIFO full	R
31:9	-	These bits are read as 0. The write value should be 0.	R/W

The FIFO Full Status Register shows status of the full bits of the FIFO buffers.

28.2.34 CFDFMSTS : FIFO Message Lost Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0068

Bit position	31																							8							1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CFMLT	-	-	-	-	-	-	RFXMLT[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	RFXMLT[1:0]	RX FIFO Message Lost Status 0: Corresponding FIFO Message Lost flag not set 1: Corresponding FIFO Message Lost flag set	R
7:2	-	These bits are read as 0. The write value should be 0.	R/W
8	CFMLT	Common FIFO Message Lost Status 0: Corresponding FIFO Message Lost flag not set 1: Corresponding FIFO Message Lost flag set	R
31:9	-	These bits are read as 0. The write value should be 0.	R/W

The FIFO Message Lost Status Register shows status of the Msg Lost bits of the FIFO buffers.

28.2.35 CFDRFISTS : RX FIFO Interrupt Flag Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x006C

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RFXIF[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	RFXIF[1:0]	RX FIFO[x] Interrupt Flag Status 0: Corresponding RX FIFO Interrupt flag not set 1: Corresponding RX FIFO Interrupt flag set	R
31:2	-	These bits are read as 0. The write value should be 0.	R/W

The FIFO Interrupt Flag Status Register shows status of the interrupt flag bits of the RX FIFO buffers.

28.2.37 CFDCDTSTS : DMA Transfer Status Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00CC

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	CFDMASTS	-	-	-	-	-	-	RFDMASTS1	RFDMASTS0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFDMASTS0	DMA Transfer Status for RX FIFO 0 0: DMA transfer stopped 1: DMA transfer on going	R
1	RFDMASTS1	DMA Transfer Status for RX FIFO 1 0: DMA transfer stopped 1: DMA transfer on going	R
7:2	-	These bits are read as 0. The write value should be 0.	R/W
8	CFDMASTS	DMA Transfer Status only for Common FIFO 0: DMA transfer stopped 1: DMA transfer on going	R
31:9	-	These bits are read as 0.	R

The DMA Transfer Status Register shows the status of the DMA transfer.

28.2.47 CFDTXQPCTR : TX Queue Pointer Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0094

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TXQPC[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

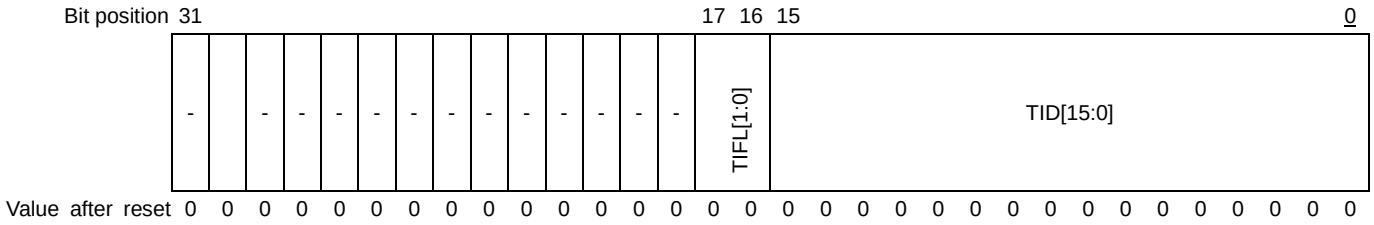
Bit	Symbol	Function	R/W
7:0	TXQPC[7:0]	TX Queue Pointer Control Increments the write pointer to the TX Queue buffer in the corresponding channel	W
31:8	-	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Pointer Control Registers are used to confirm storage of a full message in the corresponding TX Queue buffers.

28.2.51 CFDTHLACC1 : TX History List Access Register 1

Base address: CANFD_B = 0x400B_0000

Offset address: 0x0744



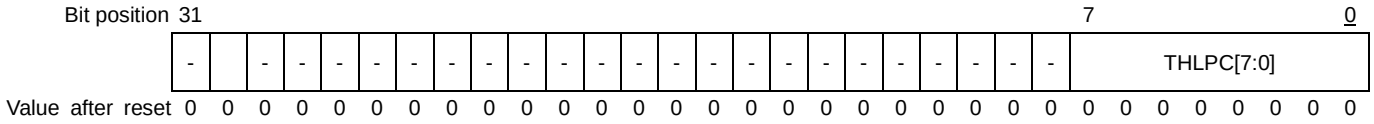
Bit	Symbol	Function	R/W
15:0	TID[15:0]	Transmit ID These bits indicate that message buffer reference ID, TX FIFO reference ID, or AFL pointer field is stored for software drivers.	R
17:16	TIFL[1:0]	Transmit Information Label These bits indicate that message buffer information label, TX FIFO information label, or AFL information label is stored for software drivers.	R
31:18	-	These bits are read as 0. The write value should be 0.	R/W

The TX History List Access Registers 1 provide access to entry in the TX History List based on the read pointer value.

28.2.52 CFDTHLPCTR : TX History List Pointer Control Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00A0



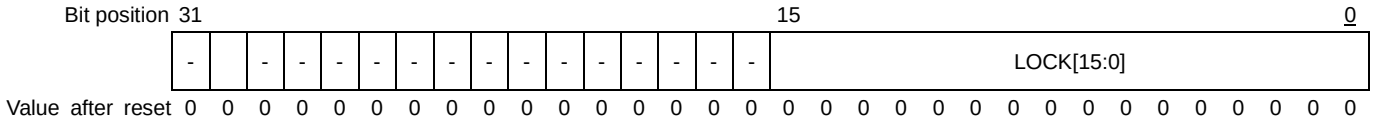
Bit	Symbol	Function	R/W
7:0	THLPC[7:0]	TX History List Pointer Control Increments the write pointer to the TX History List in the corresponding channel	W
31:8	-	These bits are read as 0. The write value should be 0.	R/W

The TX History List Pointer Control Registers are used to increment the read pointer of the TX History List.

28.2.57 CFDGLOCKK : Global Lock Key Register

Base address: CANFD_B = 0x400B_0000

Offset address: 0x00B8



Bit	Symbol	Function	R/W
15:0	LOCK[15:0]	Lock Key Key bits for unlocking the protection of test modes	W
31:16	-	These bits are read as 0. The write value should be 0.	R/W

The Global Lock Key register is a write-only register that is used to unlock the protection for special test bits.
See section 28.9.2. Global Test Modes for Lock key specification.

40.2.2 DOSR : DOC Flag Status Register

Base address: DOC_B = 0x4010_9000

Offset address: 0x04

Bit position	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	DOPCF
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DOPCF	Data Operation Circuit Flag Indicates the result of an operation.	R
7:1	-	These bits are read as 0. The write value should be 0.	R/W

The DOSR register indicates the status of the data operation.

40.2.3 DOSCR : DOC Flag Status Clear Register

Base address: DOC_B = 0x4010_9000

Offset address: 0x08

Bit position	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	DOPCFCL
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DOPCFCL	DOPCF Clear W 0: Maintains the DOPCF flag state. 1: Clears the DOPCF flag.	W
7:1	-	These bits are read as 0. The write value should be 0.	R/W

The DOSCR is a register which can clear the status of data operation. This register is read as 0x00.