Date: Sep. 29, 2022

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RA*-A0063A/E	Rev.	1.00
Title	RA6T2 Group Correction of the condition for ADC Self-calibration		Information Category	Technical Notification		
Applicable Product	RA6T2 Group	Lot No. All	Reference Document	RA6T2 Group User's Manual : Hardware Rev.1.20		

ADC Self-calibration condition when sample and hold setting is changed had been modified.

[Modified]

Table 36.7 List of conditions under which Self-calibration should be performed

Conditions under which self-calibration is required	Internal-circuit Calibration	Gain/Offset Calibration	Channel dedicated sample-and-hold circuit Gain and Offset Calibration *1
After reset release	✓	✓	✓
After releasing the module stop	✓	✓	✓
When returning from Software Standby mode or Deep Software Standby mode	✓	✓	✓
When changed the ADCLK setting (When clock source or frequency is changed)	✓	✓	✓
When changed the operation mode or the scan mode of the A/D converter (When changed ADMDR.ADMDm bit (m = 0, 1))	✓	✓	✓
When changed A/D successive approximation time (When changed ADCNVSTR.CSTm bit (m = 0, 1))	✓	✓	✓
When changed the operation setting of the channel-dedicated sample-and-hold circuit *1	—	—	✓

Note: ✓: Self-calibration should be performed.
—: Self-calibration is not required.
Note 1. When any of ADSHCRm.SHENn bits are set to 1, or any of ADSHCRm.SHENn bits are changed, perform the channel-dedicated sample-and-hold circuits self-calibration (m = 0, 1. n = 0 to 2, 4 to 6). Not required if the channel-dedicated sample-and-hold circuits are not used.

[Original]

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When changed the operation mode or the scan mode of the A/D converter (When changed ADMDR.ADMDm bit (m = 0, 1))	✓	✓	—
When changed A/D successive approximation time (When changed ADCNVSTR.CSTm bit (m = 0, 1))	✓	✓	—
When changed the operation setting of the channel-dedicated sample-and-hold circuit *1	—	—	✓

Note: ✓: Self-calibration should be performed.
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