Date: Dec. 21, 2021

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RA*-A0051A/E	Rev.	1.00
Title	RA6M4 Group, RA6M5 Group, correction of CSn Control Register (CSnCR) bit		Information Category	Technical Notification		
Applicable Product	RA6M4 Group RA6M5 Group	Lot No. All	Reference Document	RA6M4 Group User's Manual Hardware Rev.1.10 RA6M5 Group User's Manual Hardware Rev.1.10		

The description of CSnCR.EMODE bit is corrected.

[Before]

14. Buses

14.3 Register Descriptions

14.3.3 CSnCR : CSn Control Register (n = 0 to 7)

EMODE bit (Endian Mode)

This bit specifies the endian of each area. As core endian is fixed little, When the endian setting for each area is different from that for the MCU, no instruction code can be allocated in the area. The instruction code should be allocated to the external space of little-endian setting.

[After]

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Only CPU, DMAC, and DTC can access to big-endian area.

Memory type of big-endian area must be "Device-Memory".

For changing the memory type, refer to ARMv8-M Architecture Reference Manual.