To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPD

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Product Category	MPU&MCU		Document No.	TN-SH7-482A/EA	Rev.	1.0
Title	POE-Usage Notes for the SH7046 Series, SH7047 Series, and SH7144 Series		Information Category	Usage Limitation		
Applicable Product	HD64F7046, HD6437049, HD64F7047, HD6437144, HD64F7144, HD6437145, HD64F7145, HD6437148, HD6437048, HD6437101	Lot No. All	Reference Document	SH7046 Series Hardware Manual (ADE-602-237B) SH7047 Series Hardware Manual (REJ09B0020-0100Z) SH7144 Series Hardware Manual (REJ09B0108-0300Z) SH7101 Series Hardware Manual (ADE-602-272)		

We greatly appreciate your purchasing our semiconductor products. We would like to inform you of some notes on usage of the POE function of the SH7046-Series, SH7047-Series, and SH7144-Series products. Please include these notes in your hardware manual of the relevant product.

1. Symptom

1.1 Regarding the POEnF*[1] bits

If setting of the POEnF bits in the input level control/status registers (ICSR1 and ICSR2) by the hardware*[2] and reading from these bits occur simultaneously, “0” will be read, where “1” should be read.

Furthermore, if clearing of these bits is attempted subsequent to the above condition, the clearing should be ignored*[3] but it will be carried out.

*[1]: For the SH7046-Series and SH7047-Series, n = 0 to 6; for the SH7144-Series, n = 0 to 3.

*[2]: The POEnF bits are set when the signals input to the respective POEn pins satisfy the conditions that are specified by the POEnM1 and POEnM0 of the ICSR1 and ICSR2.

*[3]: The correct operation is that clearing of the POEnF bits is only possible after “1” is read from them in order to prevent accidental clearing.

1.2 Regarding the OSF bit

The same symptom applies to the OSF bits of the output level control/status register (OCSR).

2. To Avoid This Problem

Please clear the POEnF bits or the OSF bit in these steps: first execute a read for ICSR1, ICSR2, or OCSR, then write “0” to the bits that had a read value of “1” to clear them while writing “1” to other bits. If this procedure is not followed, the POEnF bits and the OSF bit may be cleared unexpectedly if their setting by hardware and reading occur simultaneously.