## Old Company Name in Catalogs and Other Documents

On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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## **RENESAS TECHNICAL UPDATE**

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Product Category	MPU&MCU			Document No.	TN-SH7-A644A/E	Rev.	1.00	
Title	Notice and error correction about deep standby control register (DSCTR) and power-on reset exception handling.			Information Category	Technical Notification			
Applicable Product	R5S72650P200BG,		Lot No.		• SH7265 Group Hardware Manual			
Troduct	R5S72651P200BG, R5S72652P200BG, R5S72653P200BG, R5S72050W200BG		ALL	Reference Document	Rev.1.00 (REJ09B0351-0100) • SH7205 Group Hardware Manual Rev.1.00 (REJ09B0372-0100)			
We would lik	te to inform you of the fol	lowing notice and e	error correcti	ion about deep	standby control registe	r (DSCTI	R) and	
power-on reset exception handling in the above-mentioned applicable products.								
1. Error correction								
[Error] 35	[Error] 35.3 (SH7265) / 32.3(SH7205) Register States in Each Operating Mode							
	Module Name	Register Abbreviation		Deep	Deep Standby			
	Power-Down Modes	DSCIR		Retained				
Correction	1 25 2 (SUZ265) / 22 2(S	UZ205) Degister Sta	taa in Each	Operating Mode				
[Correction] 35.3 (SH7265) / 32.3 (SH7205) Register States in Each Operating Mode								
	Power-Down Modes DSCTR			Initialized				
2. Notice								
<ul> <li>The read value of bits 7 and 6 of deep standby control register (DSCTR) are undefined.</li> </ul>								
• After (1) power-on reset by /RES pin is released. (2) the LSI transit to deep standby mode in case that bit 6								
(RAMBOOT) of deep standby control register (DSCTR) is set to "1". (3) the deep standby mode is cancelled, and (4)								
power-on reset by WDT or H-UDI reset is occurred before power-on reset by /RES pin is executed again then the								
behavior of the power-on reset exception handling is as follows.								
Address where the program Address where the stack								
	vior of the power-on reset e	JDI reset is occurre exception handling is ess where the progra	d before po s as follows. am Add	wer-on reset by Iress where the	/RES pin is executed	again, th	en the	
	vior of the power-on reset e	JDI reset is occurre exception handling is ess where the progra unter (PC) is fetched H'FE800000	d before po s as follows. am Add I po	wer-on reset by Iress where the inter (SP) is fetc H'EE800004	r /RES pin is executed	again, th	en the	
So if	vior of the power-on reset e	JDI reset is occurre exception handling is ess where the progra unter (PC) is fetched H'FF800000 PC and SP are nec	d before po s as follows. am Add b po essary to be	wer-on reset by Iress where the inter (SP) is feto H'FF800004 retained in the a	r /RES pin is executed stack hed	again, th data rete	en the	
So if	vior of the power-on reset e	JDI reset is occurre exception handling is ess where the progra unter (PC) is fetched H'FF800000 PC and SP are nec	d before po s as follows. am Add l po essary to be	wer-on reset by Iress where the inter (SP) is feto H'FF800004 retained in the a	r /RES pin is executed stack hed area of on-chip RAM for	again, th data rete	en the	
So if • After (1	vior of the power-on reset e Addre applicable as above case,	JDI reset is occurre exception handling is ess where the progra unter (PC) is fetched H'FF800000 PC and SP are nect pin is released, (2)	d before po s as follows. am Add d po essary to be the LSI tra	wer-on reset by Iress where the inter (SP) is feto H'FF800004 retained in the a nsit to deep sta	r /RES pin is executed stack hed area of on-chip RAM for	again, th data rete e deep s	en the ention. tandby	
So if After (1 mode is	vior of the power-on reset e Addre applicable as above case, ) power-on reset by /RES	JDI reset is occurre exception handling is ess where the progra unter (PC) is fetched H'FF800000 PC and SP are nect pin is released, (2) ossibility that power	d before po s as follows. am Add b po essary to be the LSI tra -on reset by	wer-on reset by Iress where the inter (SP) is feto H'FF800004 retained in the a nsit to deep sta WDT or H-UDI	r /RES pin is executed stack hed area of on-chip RAM for ndby mode, and (3) the	again, th data rete e deep si power-oi	en the ention. tandby	
So if After (1 mode is by /RES	vior of the power-on reset e Addre applicable as above case, ) power-on reset by /RES cancelled, if there is a p	JDI reset is occurre exception handling is ess where the progra unter (PC) is fetched H'FF800000 PC and SP are nect pin is released, (2) ossibility that power-	d before po s as follows. am Add b po essary to be the LSI tra on reset by or H-UDI sho	wer-on reset by Iress where the inter (SP) is feto H'FF800004 retained in the a nsit to deep sta WDT or H-UDI puld be done in	r /RES pin is executed stack hed area of on-chip RAM for ndby mode, and (3) the reset is occurred before the condition that bit 15	again, th data rete e deep si power-oi 5 (IOKEE	en the ention. tandby n reset P) and	
So if After (1 mode is by /RES bits 9~(	vior of the power-on reset e Addre applicable as above case, ) power-on reset by /RES cancelled, if there is a p S pin is executed again, th	JDI reset is occurre exception handling is ess where the progra unter (PC) is fetched H'FF800000 PC and SP are nect pin is released, (2) ossibility that power e settings of WDT co	d before po s as follows. am Add b po essary to be the LSI tra on reset by or H-UDI sho DSER) are a	wer-on reset by Iress where the inter (SP) is feto H'FF800004 retained in the a nsit to deep sta WDT or H-UDI ould be done in all cleared after	r /RES pin is executed stack hed area of on-chip RAM for ndby mode, and (3) the reset is occurred before the condition that bit 15 canceling deep standby	again, th data rete e deep si power-oi 5 (IOKEE	en the ention. tandby n reset P) and	
So if After (1 mode is by /RES bits 9~0 bits are	vior of the power-on reset e Addre applicable as above case, ) power-on reset by /RES cancelled, if there is a p S pin is executed again, th of deep standby cancel s 1, please write these as "0	JDI reset is occurre exception handling is ess where the progra- unter (PC) is fetched H'FF800000 PC and SP are neck pin is released, (2) ossibility that power- e settings of WDT of ource flag register ( " after reading these	d before po s as follows. am Add b po essary to be the LSI tra on reset by or H-UDI sho DSFR) are a	wer-on reset by Iress where the inter (SP) is feto H'FF800004 retained in the nsit to deep sta WDT or H-UDI ould be done in all cleared after	r /RES pin is executed stack hed area of on-chip RAM for andby mode, and (3) the reset is occurred before the condition that bit 15 canceling deep standby	again, th data rete e deep si power-ou 5 (IOKEE v mode (if	en the ention. tandby n reset P) and f some	
So if After (1 mode is by /RES bits 9~0 bits are If (1) th	<ul> <li>vior of the power-on reset experience of the power-on reset of Address</li> <li>applicable as above case,</li> <li>applicable as above case,</li> <li>power-on reset by /RES</li> <li>cancelled, if there is a p</li> <li>cancelled, if there is a p</li> <li>of deep standby cancel s</li> <li>please write these as "0</li> <li>e setting of WDT or H-UD</li> </ul>	JDI reset is occurre exception handling is ess where the progra- unter (PC) is fetched H'FF800000 PC and SP are neck pin is released, (2) ossibility that power e settings of WDT c ource flag register ( " after reading these I is done in the con-	d before po s as follows. am Add b po essary to be the LSI tra on reset by or H-UDI sho DSFR) are a e as "1"). dition that IC	wer-on reset by Iress where the inter (SP) is feto H'FF800004 retained in the a nsit to deep sta WDT or H-UDI build be done in all cleared after DKEEP bit is no	ARES pin is executed stack hed area of on-chip RAM for andby mode, and (3) the reset is occurred before the condition that bit 15 canceling deep standby t 0, and (2) power-on re	again, th data rete e deep si power-oi 5 (IOKEE v mode (if	en the ention. tandby n reset P) and f some	



are retained in deep standby mode and which are not in table 33.4 (SH7265) / table 30.4 (SH7205), are kept retained. Additionally, in the case that bit 7 (CS0KEEPE) of deep standby control register (DSCTR) are set to "1", the pin status of the pins in table 33.4 (SH7265) / table 30.4 (SH7205) are also keep retained.

If (1) the settings of WDT or H-UDI is done in the condition that bits 9~0 are not all 0, and (2) power-on reset by WDT or H-UDI reset is occurred before power-on reset by /RES pin is executed again, the internal information about the deep standby canceling source is not cleared, and deep standby mode are cancelled by the wrong canceling source when the LSI attempt to transit to deep standby mode since then.

