To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

Classification of Production	MPU&MCU		No	TN-SH7-492A/E	Rev	1
THEME	Notice about The MMCIF transfer data block size in multiblock read command.	Classification of Information	1. Spec change 2. Supplement of Documents (3.) Limitation of Use 4. Change of Mask 5. Change of Production Line			
PRODUCT NAME	SH7760	Lot No.: All	Reference Documents	SH7760 hardware manual (ADE-602-291)	Effective Date: Eternity	

There are the following notes about the problem of the MMCIF data block size in the multiblock read command.

1. Summary

The MMCIF may not receive the command response correctly, when it finishes receiving the end bit of the first data block before receiving the end bit of the command response. It may occur after MMCIF sends CMD18 to the receive device.

2. Condition in which the problem occurs

When all of the following operations consist, the problem occurs.

(1) The multiblock read command (CMD18) is sent.

(2) The transfer data block size is setting to 1,2,4 or 8 byte(s).

(3) The end bit of the command response is received after the end bit of the first data block is received.

3. Workaround for this problem

(1) The transfer data block size in Transfer Byte Number Count Register (TBCR) must be more than 16 bytes when CMD18 is transmitted.

(2) Confirm that the end bit of the command response is received before the end bit of the first data block is received, if the transfer data block size is 1,2,4 or 8 bytes when CMD18 is transmitted.

Keep the below formula in order to confirm that the end bit of the command response is received before the end bit of the first data block is received.

N_{AC} cycles + Read Data cycles > (N_{CR} Cycles + Response cycles)

Please confirm the N_{AC} and N_{CR} in the spec of target devices to communicate.

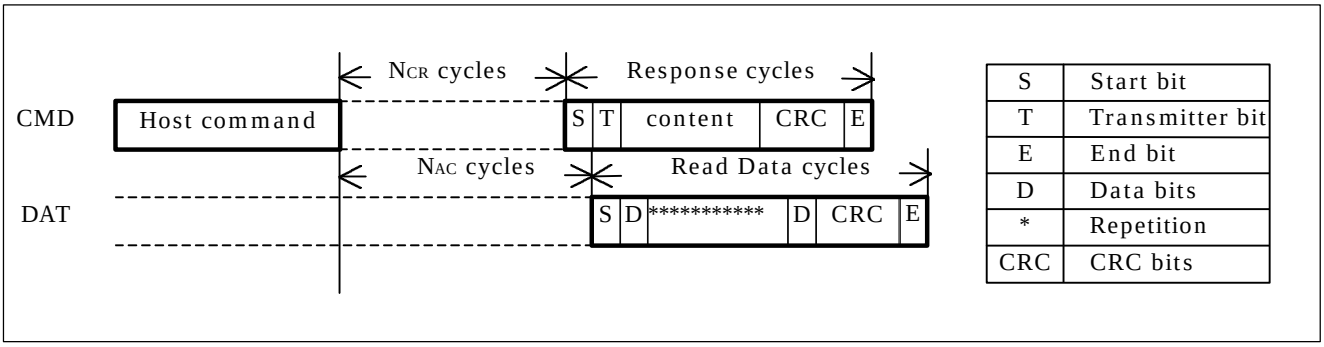

figure.1 Timing of receiving the command response and data