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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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RENEASAS TECHNICAL UPD

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Product Category	MPU&MCU		Document No.	TN-SH7-517A/EA	Rev.	1.0
Title	Notice about double precision FADD and FSUB instructions for SH-4		Information Category	Usage Limitation		
Applicable Product	SH7750,SH7750S,SH7750R	Lot No.	Reference Document	SH7750 series hardware manual (ADE-602-124) SH7751 series hardware manual (ADE-602-201) SH7760 hardware manual (ADE-602-291)		
	SH7751,SH7751R SH7760 SH-4 core use product	All				

There are the following notes about double precision FADD and FSUB instruction for SH-4.

1. Contents

This document reports the analysis on problem about double precision FADD and FSUB instruction for SH-4. All SH-4 products and SH-4 core has the same problem. This document explains the problem.

2. Condition in which the problem occurs

When all the following conditions are satisfied, the Problem may occur.

1. Double precision FADD instruction or Double precision FSUB instruction is executed.
2. Difference of exponents of two inputs (DRm,DRn) is 43 to 50.
3. Bit 24 to 31 of the input with the smaller absolute value of DRn and DRm is NOT all 0.
4. Bit 0 to 23 of the input with the smaller absolute value of DRn and DRm is all 0.
5. Bit 32 to 40 of the input with the smaller absolute value of DRn and DRm is all 0.

What happens by the Problem is

The operation is inexact but FPSCR.Flag.I or FPSCR.Cause.I may not be set to 1.

The operation has incorrect rounding.

In detail, SH-4 selects the smallest expressible value of larger side of the pre-rounding one instead of the largest expressible value of smaller side of the pre-rounding one, or vice versa.

3. Examples

The result of double precision FSUB DR0,DR2 is # h' C4B250D2 0CC1F974 as against the expected value #h' C4B250D2 0CC1F973, and FPSCR.Flag.I or FPSCR.Cause.I is not set to 1, though the operation is inexact.

(input data)	fpscr = #h' 000C0001
	DR0 = #h' c1f00000 80000000, DR2 = #h' c4b250d2 0cc1fb74
(correct result)	DR2 = h'C4B250D2 0CC1F973
(result of this LSI)	DR2 = h'C4B250D2 0CC1F974

4. Effect of the problem

In addition to the above explanation, the effect of the numeric value of this problem can be limited within the boundary that can be described by the small arithmetic error, 1/256 of LSB in the significant, and the rounding mechanism. Strictly speaking, it is explained as follows.

- a : The computing result of infinite accuracy
- b : The largest expressible value of smaller side of a
- c : The smallest expressible value of larger side of a
- d : The right rounded value of a
- e : This LSI's rounded value of a

(1) Round to Nearest

When the rounding is correctly performed, the value of the rounding error is

$$0 \leq |d - a| \leq (1/2) * (c - b)$$

But the result of this LSI is

$$0 \leq |e - a| < (129/256) * (c - b)$$

The range of the rounding error is 1/256 * (c - b) larger than that of correct error.

(2) Round to Zero

When the rounding is correctly performed, the value of the rounding error is

$$(-1) * (c - b) < |d| - |a| \leq 0$$

But the result of this LSI is

$$(-1) * (c - b) < |e| - |a| < (1/256) * (c - b)$$

The range of the rounding error is 1/256 * (c - b) larger than that of correct error.